Kazuo Kondo · Morihiro Kada
Kenji Takahashi *Editors*

Three-Dimensional Integration of Semiconductors

Processing, Materials, and Applications

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Preface

The concept of three-dimensional integration of semiconductors originated with the US patent by IBM in 1969. The patent is titled "Hourglass-shaped conductive connection through semiconductor structures" (http://www.google.com.mx/patents/US3648131). The original interconnect looks like an hourglass. Since 1969, the three-dimensional integration concept has spread out to semiconductor industries all over the world and more than 40 consortia and companies have been involved in this development. Forty-five years after its invention, three-dimensional integration of semiconductors is becoming very popular, and is about to be industrialized in advanced electronics in the very near future.

This book reviews the state of the art of three-dimensional semiconductor integration. Chapter 1 gives an overview of three-dimensional integration research and development history. Chapter 2 summarizes recent three-dimensional integration research and development activities and applications. Chapter 3 gives an explanation of through-silicon via (TSV) formation processes. Chapters 4 and 5 cover wafer handling, wafer thinning, and bonding of wafers and dies. Chapter 6 explains metrology and inspection. Chapter 7 discusses reliability and characterization issues. Chapter 8 covers trends in technology development of three-dimensional integration circuits testing. Finally, Chapter 9 summarizes research and development project results conducted by New Energy and Industrial Technology Development Organization (NEDO)/Association of Super-Advanced Electronics Technologies (ASET): Japan in 2008 to 2012.

We really hope that this book will help not only beginners in three-dimensional integration technology of semiconductors but also engineers who are already involved in this field, both in industry and academia. I was very much astonished when, in 2000, ASET members visited my university and asked for support to fill an interconnect via that was huge compared to the contact via created by the damascene process of copper electrodeposition. This introduction gave me the initial motivation to start my research on three-dimensional integration. Two editors,

Morihiro Kada and Kenji Takahasi, are former ASET leaders. The opportunity given by K. Howell of Springer to publish this book is very much appreciated.

Kazuo Kondo Osaka
Morihiro Kada Osaka
Kenji Takahasi Oita

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Dr. Kazuo Kondo is a professor in the Department of Chemical Engineering, Osaka Prefecture University. He received his Ph.D. in chemical engineering from the University of Illinois in 1981. He has worked for Sumitomo Metal Industries, Hokkaido University, and Okayama University. He has 200 research publications and 100 patents. His major research is Copper Electrodeposition for TSV. His research extends to various fields, not only in electrodeposition but also in battery science and CVD. He is a member of the Electrochemical Society, IEEE, the Society of Chemical Engineering, Japan, the Japanese Institute of Electronics Packaging, the Surface Finishing Society of Japan, Material Japan, Electrochemistry Japan and the Japanese Society of Applied Physics.

Morihiro Kada is an invited researcher of the National Institute of Advanced Industrial Science and Technology (AIST) and a part-time researcher at Osaka Prefecture University. Prior to joining AIST and the university, he headed the Japanese national research and development project on semiconductor 3D-Integration technology in the Association of Super-Advanced Electronics Technologies (ASET). He has also been the general manager of the Advanced Packaging Development Department in Sharp Corporation. He received his B.E. in applied physics from Fukui University, Japan in 1970. He has more than 40 years of experience in semiconductor packaging engineering, with major emphasis on developing chip scale, chip stack package, and three-dimensional-system-in-package (3D-SiP), and is the global pioneer of 3D-Integration technology in the world.

Dr. Kenji Takahashi is a chief specialist at Memory Packaging Development Department, Memory Division, Semiconductor and Storage Company, Toshiba Corporation. He received an M.E. in chemical engineering from the University of Tokyo in 1984 and a Ph.D. in information science and electrical engineering from Kyushu University in 2010. His major research and development focuses on semiconductor packaging and chip package interaction, especially through-silicon via technology. He was the research manager of the Electronic System Integration Technology Research Department at the Association of Super-Advanced Electronics Technologies (ASET). He is a senior member of IEEE, and a member of the Society for Chemical Engineers, Japan; the Institute of Electronics, Information and Communication Engineers; and the Japanese Institute of Electronics Packaging.

Chapter 1
Research and Development History of Three-Dimensional Integration Technology

Morihiro Kada

1.1 Introduction

Semiconductor integrated circuits have been developed according to Moore's law; the conjecture made in 1965 was that the number of transistors in a dense integrated circuit (IC) will double every 2 years, and the industry has developed according to this trend [1]. Two different concepts have been proposed for future advancements. One is "More Moore," which suggests that technological progress will continue to follow scaling theory, and the other is termed "More than Moore," which emphasizes the evolution and diversification of function [2].

1.1.1 The International Technology Roadmap for Semiconductors

The international semiconductor research community gathered in 2005, at the abovementioned meeting (the International Technology Roadmap for Semiconductors**,** ITRS), which led to the concept of "More than Moore." Two years later, at ITRS 2007, a number of such ideas were formally defined. We elaborate on two of these: scaling and functional diversification with reference to Fig. 1.1.

1. Scaling: Fig. 1.1, vertical axis of "More Moore"
   a. *Geometrical scaling:* Also referred to as constant field scaling, this design methodology involves reducing the horizontal and vertical dimensions of physical features of the on-chip logic and memory storage components to

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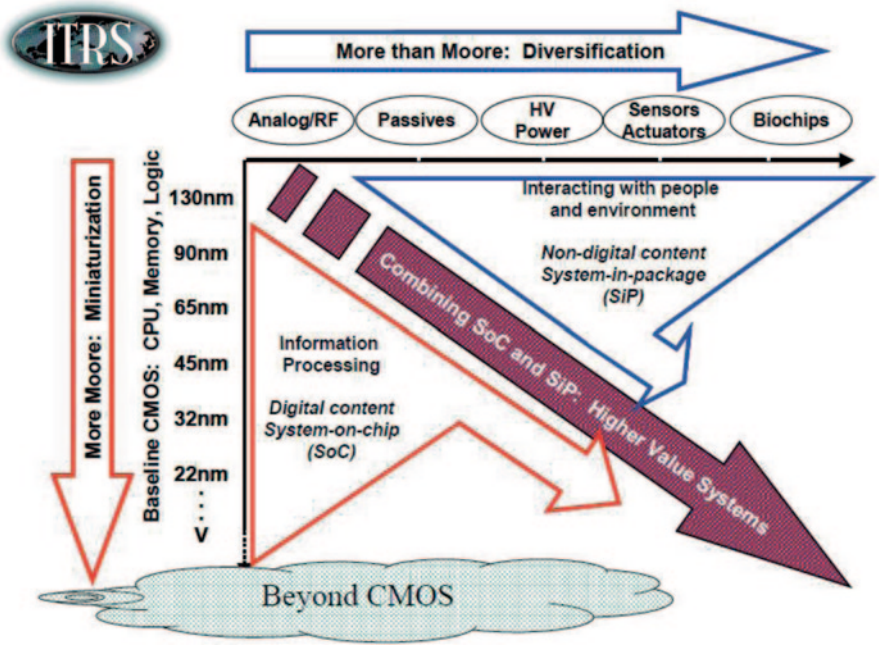

Fig. 1.1 A diagrammatic representation of the concepts of "Moore's law" and "More than Moore". (Reproduced with permission from Ref. [3], Fig. 4). *RF* radio frequency, *CPU* central processing unit, *CMOS* complementary metal–oxide–semiconductor

improve density (cost per function reduction), performance (speed, power), and reliability (Fig. 1.1).

b. *Equivalent scaling:* This approach refers to (a) three-dimensional (3D) device structure ("design factor") improvements as well as other nongeometric processing techniques and the use of new materials that affect the performance of the chip; (b) novel design techniques and technologies, such as multi-core design. Equivalent scaling occurs in conjunction with geometric scaling and aims for the continuation of "Moore's law."

2. Functional Diversification: Fig. 1.1, horizontal axis of "More than Moore."

Moore's law is not the only way to provide additional value to the end user. A complementary approach is that of functional diversification, which refers to the incorporation of new functionalities into devices that are not necessarily scalings of existing hardware or software. Typical of this "More than Moore" approach is the migration of non-digital functionalities (e.g., radio frequency (RF) communication, power control, passive components, sensors, and actuators) from the system board level into a particular chip-level (system on a chip; SoC) or package-level (system in package; SiP) implementation. As the need increases for evermore complex software to be embedded into SoCs and SiPs, the role of the software itself in performance scaling may also need to be considered. The objective of the "More than Moore" design methodology is to incorporate digital and non-digital functionalities into compact systems.

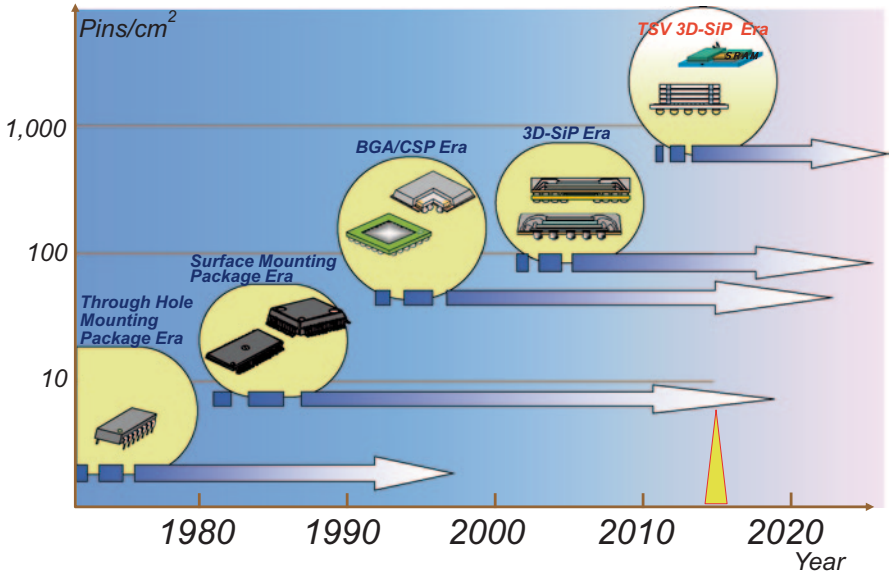

Fig. 1.2 Toward the new TSV 3D-SiP Era. *3D-SiP* three-dimensional system in package, *TSV* through-Si via, *BGA/CSP* ball grid array/chip-scale package

1.1.2 3D Integration Technology

Although 3D integration technology is not explicit in the definition of "More than Moore," it is generally considered to be one of the most important technology development strategies. The transistor scaling that has continued for more than 40 years is approaching the atomic level of silicon, and this physical limit will likely be reached in 10–15 years.

Entirely new device structures, such as carbon nanotubes, spintronics, and molecular switches are being developed to replace transistor technology. However, they will not be ready for 10–15 years. In the interim, 3D integration technology offers a viable solution for continued performance and economic advancement [4].

"More than Moore" is not just a solution to the limitation of "More Moore," it also recognizes the evolution and potential for improvements of packaging technology. Figure 1.2 illustrates the history of IC packaging technology. Every 10 years since the 1970s, packaging technology has undergone a technological revolution. The first decade of this century is the era of the 3D system in package (3D-SiP), and work has begun to develop new 3D technology termed through-Si via (TSV) that will define the present decade [5]. In TSV, the electrode passes completely through the silicon wafer (or chip). It represents the fusion of silicon wafer process technology (front end of line, FEOL) and semiconductor packaging technology (assembly/packaging).

3D integration using conventional technologies, such as with the wire bonding (WB) as shown in Fig. 1.3 (left), is referred to as 3D integration packaging technologies. In this book, we focus our attention on systems in which semiconductor chips are stacked and connected by TSV, as shown in Fig. 1.3 (right), which

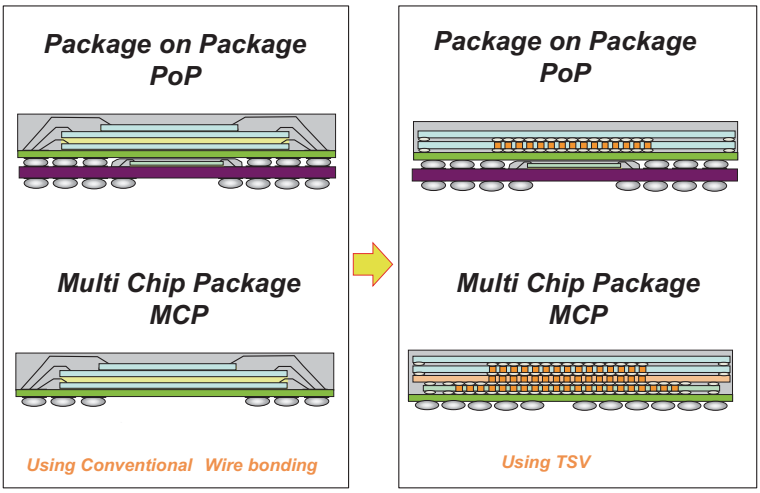

Fig. 1.3 3D integration packaging technology and 3D integration technology [6]

define 3D integration technology [6]. We do not discuss 3D integrated circuits (3D-IC) that use FEOL, such as 3D NAND in which transistors are stacked, nor the Intel tri-gate transistors that were introduced in the 22-nm generation ivy bridge CPU.

1.2 Motivation for 3D Integration Technology

The development impetus is accounted for in the following two points.

1. If semiconductor integrated circuit chips are connected using TSV, the interconnected distance is approximately 1/1000 of that using conventional WB (micrometers compared with millimeters). This results in dramatic reductions in electric resistance and capacitance, making possible high-speed operation and low power consumption.
2. It is difficult to make (wire) connections between the conventional packages on the mounting board on the order of thousands, but this task is straightforward, and on even grander scales, between Si chips using TSV. Thus, TSV-based systems that have several 1000 input/output (I/O) circuits are realizable, which also benefit from being lower power consumption devices with higher data transmission speeds.

3D integration need not be confined to like technologies. By combining semiconductor integrated circuits with, for example, micro-electro-mechanical systems (MEMS) devices, unique functionalities can be developed in what is termed heterogeneous 3D integration technology.

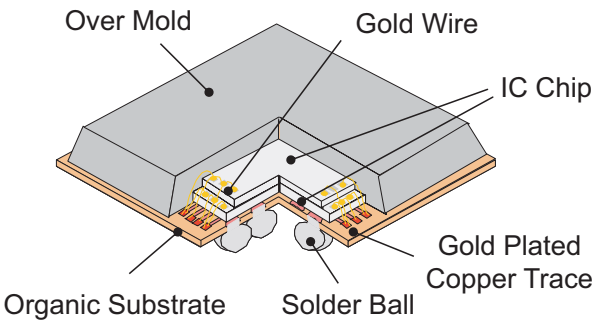

Fig. 1.4 Typical construction of S-CSP (MCP). *IC* integrated circuit

1.3 Research and Development History of 3D Integration Technology

1.3.1 3D Packaging Technology

Even as of 2015, the use of 3D-IC (TSV) is uncommon, with the exception of complementary metal–oxide–semiconductor imaging sensors (CIS). However, high-volume manufacturing of 3D integration packaging technology using WB continues.

In 1998, Sharp Corporation developed the world's first stacked two-chip chip-scale package (CSP) using WB [7]. Before that time, there was no notion of chip stacking in CSP. This led to its development for use in mobile phones, mostly by Japanese chip makers, such as Sharp, Mitsubishi, Hitachi, NEC, Toshiba, and Fujitsu. This technology was called stacked chip-scale (size) package (S-CSP) or multi-chip package (MCP). Figure 1.4 shows the typical construction of S-CSP (MCP).

S-CSP/MCP was first used to make combinations of NOR flash memory and of static random-access memory (SRAM), which are at the heart of all mobile phones. Consumer demand fuelled the development of smaller sizes and higher performance [8]. When Sharp developed the world's first stacked CSP, the combination memory development race was called the "East versus West War" over standardization by the Joint Electron Device Engineering Council. It became a demonstration of the strength of Japanese packaging technology.

Although, in the beginning, the interconnect technology was only WB, CSP stacking has given rise to the package on package (PoP) model, which also uses flip chip (FC) technology. Today, this approach is integral to modern smart phones and tablets; dynamic random access memory (DRAM) and application and/or baseband processors are stacked together using this technology. Upon these foundations, newer technologies continue to drive advances in telecommunications, such as through mold via (TMV) [9, 10]; see Fig. 1.5.

In the present-day flash memory, there are more than eight chips stacked into a single package [11]; see, for example, Fig. 1.6. This technology will likely continue being a mainstay of 3D integration packaging technology for some time yet. On the horizon are wireless interconnect technologies, such as capacitive and inductive 3D coupling [12].

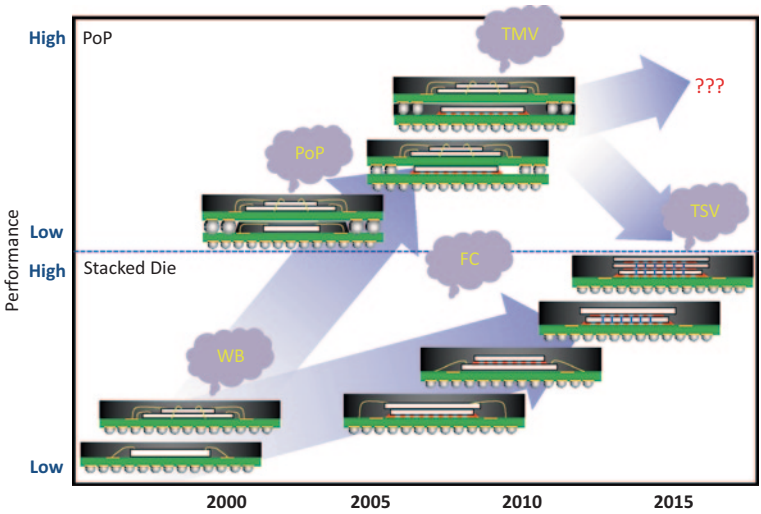

Fig. 1.5 3D integration packaging technology transition [10]. (With permission from Amkor Technology, Inc., Chandler AZ). *WB* wire bonding, *PoP* package on package, *FC* flip chip, *TMV* through-mold via, *TSV* through-Si via

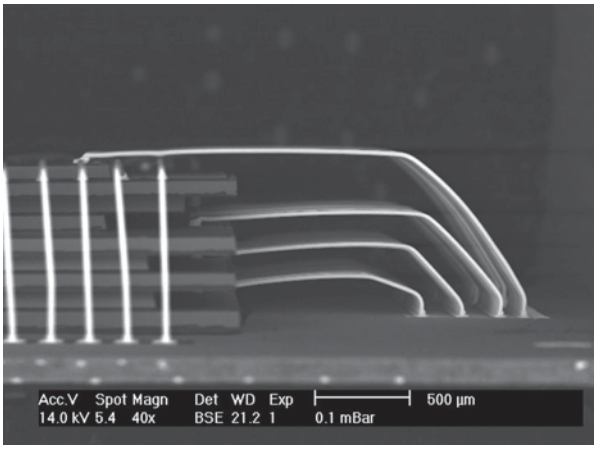

Fig. 1.6 World's first nine-chip stacked memory. (With permission from Toshiba Corporation)

1.3.2 Origin of the TSV Concept

The underlying concept of TSV technology is not new. International Business Machines Corporation filed the patent USP3,648,131 entitled, "Hourglass-shaped conductive connection through semiconductor structures" in November 1969, with the following abstract [13]:

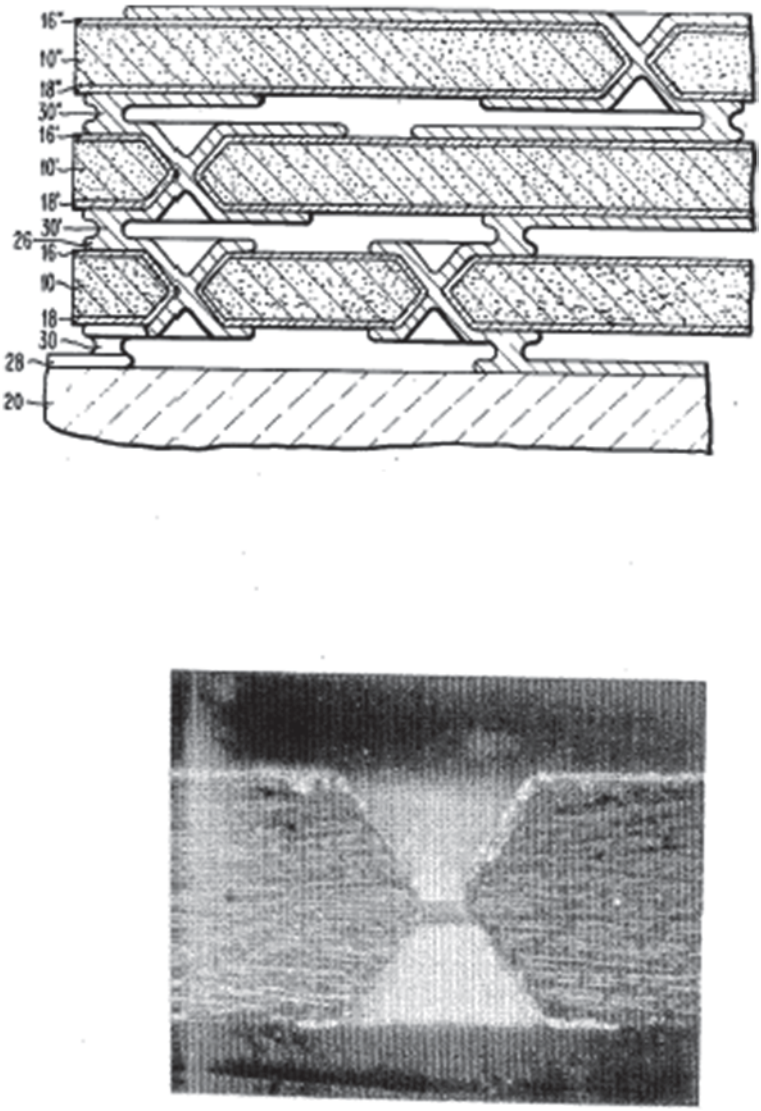

Fig. 1.7 US Patent 3,648,131 A [13]

"An integrated semiconductor structure including the fabrication thereof, and more particularly, an improved means for interconnecting the two planar surfaces of a semiconductor wafer. To provide the electrically conductive interconnections through the wafer, a hole is etched, insulated, and metallized. Active or passive devices may be formed on either or both sides of the wafer and connected to a substrate by solder pads without the use of beam leads or flying lead bonding." The drawings are shown in Fig. 1.7.

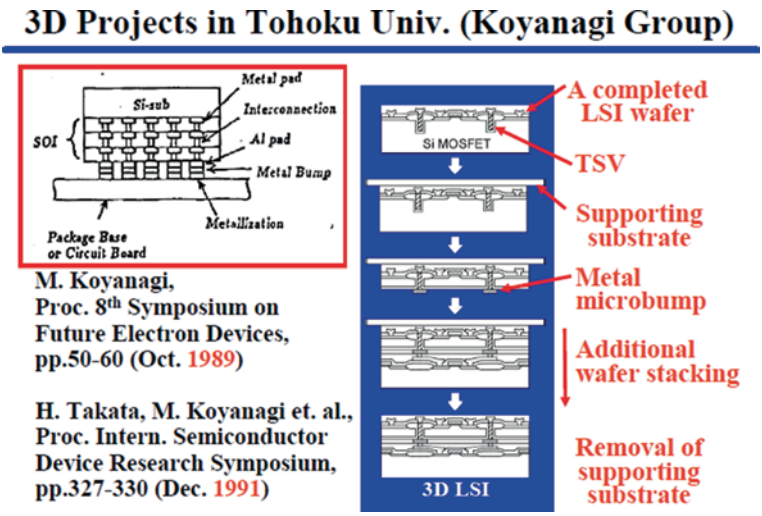

Fig. 1.8 Extracts from presentations by Tohoku University researchers in 1989 [14] and 1991 [15]. (With permission from Tohoku University, Japan). *TSV* through-Si via, *LSI wafer* large-scale integration wafer

Later on, patents JP (S59)1984-22954 (June 1, 1983) and patent JP (S61)1986–88546 (October 5, 1984) were filed by Hitachi Ltd. and Fujitsu Ltd, respectively. The patent JP (S63)1988–156348 (December 19, 1986), by Fujitsu, describes a stacked chip structure. Figure 1.8 shows key schematics of chip stacking techniques sourced from 1989 and 1991 conference presentations by Tohoku University, Japan [14, 15].

1.3.3 Research and Development History of 3D Technology in Organizations

Research and development of 3D integration technologies has been carried out through global efforts [16]. Some of the major contributions by region are summarized in Fig. 1.9 [17].

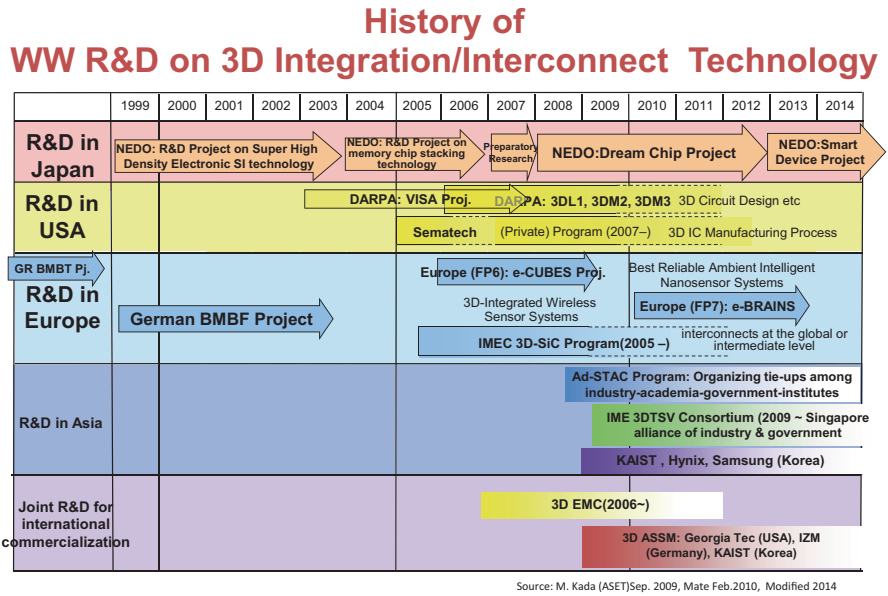

Fig. 1.9 History of global research and development on 3D integration technology. (Adapted from Ref. [16]). *NEDO* New Energy and Industrial Technology Development Organization, *DARPA* Defense Advanced Research Projects Agency, VISA vertically interconnected sensor arrays, *AD-STAC* Advanced Stacked-System Technology and Application Consortium, *TSV* through-silicon via, *ASSM* All Silicon System Module, *EMC* Equipment and Materials Consortium, *SiC* stacked integrated circuit, *German BMFT* German Ministry of Research, *BMBF* Federal Ministry of Education and Research, *FP7* Seventh Framework Programme

1.3.3.1 Japan

In Japan, research and development of the "Three-Dimensional Circuit Element R&D Project" by the Research and Development Association for Future (New) Electron Devices was conducted from 1981 to 1990, and the technology developed was termed "Cumulatively Bonded IC" (CUBIC): (in Japanese); TSV was not integral to the design. A thin film (approximately 2-μm thick) of electron channel metal–oxide–semiconductor field-effect transistor (nMOSFET) was laminated onto the bulk silicon device. The electrical interconnection of 1600 wiring contact arrays was checked, and the contact volume resistance of $5 \times 10^{-6}\ \Omega \cdot \mathrm{cm}^2$ did not adversely affect the operation [18].

In Japan, the Association of Super-Advanced Electronics Technologies (ASET) carried out a research and development project of 3D integration technology using TSV during the 5-year period 1999–2003. The project was entitled, "R&D on High Density Electronic System Integration Technology" (in Japanese). Its execution was entrusted to the New Energy and Industrial Technology Development Organization (NEDO) organization of the Japanese government's Ministry of Economy, Trade, and Industry (METI) [19]. Following on were the "Stacked Memory Chip

Technology Development Project" (in Japanese), 2004–2006 [20] and the "Development on Functionally Innovative 3D-Integrated Circuit (Dream Chip) Technology Project" (in Japanese), 2008–2012. In 2010, research was conducted with a focus on "Design Environmental Technology, Interposer Technology, Chip-Testing Technology, Three-dimensional Integration Basic Technology, Flex chip (FPGA) Technology, and RF MEMS."

The majority of the semiconductor-related businesses in Japan were involved in these projects. These included semiconductor companies Elpida, Toshiba, Renesas, and Rohm; electronic companies NEC, Sharp, Nac Image Tech., IBM, Panasonic, Hitachi, and Fujitsu; and material/equipment companies Advantest, DNP, Ibiden, Shinko, TEL, Toppan, Yamaichi, and Zycube. Furthermore, The University of Tokyo, Tohoku University, and the National Institute of Advanced Industrial Science and Technology represented the academic participation [21–23].

In 2010, an interim assessment led to a focus shift to thermal management/chip stacking technology, thin wafer technology, 3D integration technology, ultra-wide bus 3D-SiP, mixed signal (digital–analog) 3D integration technology, and heterogeneous 3D integration technology. The research outcomes are described in later sections of this book [24, 25].

However, despite the sizeable investment by the Japanese government over these long periods of time, the national semiconductor industry is presently in decline and future research and development remains uncertain.

The WOW alliance based at the Tokyo Institute of Technology (based at The University of Tokyo until 2014) was founded in 2008 [26], and the "Three-Dimensional Semiconductor Investigation Center" (translated from the Japanese) in Kyushu commenced operations in 2011 [27].

1.3.3.2 Japanese 3D Integration Technology Research and Development Project (Dream Chip)

The second full-scale national research and development (R&D) initiative of 3D integration technology using through-silicon via (TSV) was implemented over the 5-year period from 2008 to 2012. Super-Advanced Electronics Technologies (ASET) conducted the project "Development on Functionally Innovative 3D-Integrated Circuit (Dream Chip) Technology Project," and it was managed by the NEDO Organization that is based on "IT Innovation Program" of Japanese government's Ministry of Economy, Trade and Industry (METI). After the 2010 interim assessment, the two focus areas became 3D integration process basic technologies and application technologies using TSV. The former consisted of thermal management/chip-stacking technology, thin wafer technology, and 3D integration technology, while the latter focus area comprised ultra-wide bus 3D-SiP, mixed signal (digital–analog) 3D, and heterogeneous 3D; see Fig. 1.10. For details beyond research and development subjects and results, the reader is referred to Chapter 9 [17, 28].

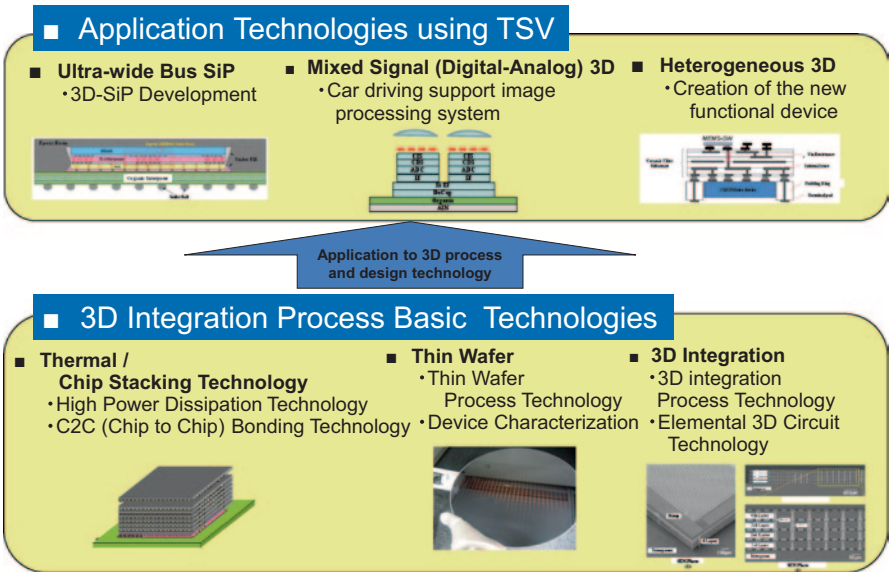

Fig. 1.10 Research and development subject of the Dream Chip Project. (With permission from the Electrochemical Society: ECS) [17]. *TSV* through-Si via

1.3.3.3 The USA

The US Defense Advanced Research Projects Agency (DARPA)'s work in microsystems technology has a long history. 3D-related research and development projects are controlled by the "Microsystems Technology Office (MTO)." These projects are:

1. Enhanced Digital (3D-IC Program)
   - Large amounts of cache memory
   - High memory bandwidth
2. Enhanced Analog (COSMOS Program)
   - Heterogeneous integration
   - Disparate process technologies (e.g., SiGe/Si, C.S./Si, SOI/Bulk)
3. Smart Focal Planes (Vertically Interconnected Sensor Arrays, VISA Program)
   - Processing at each pixel
   - High fill factors
4. Photonics (EPIC Program)
   - Optical and electronic tiers

DARPA funding and the Microelectronics Center of North Carolina Research and Development Institute (MCNC-RDI) supported a project that was started in 2003. The research and development device comprised VISA that implemented highly