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Suresh Chandra Satapathy
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Editors

Microelectronics, Electromagnetics and Telecommunications

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Preface

This LNEE volume contains the papers presented at the ICMEET 2015: International Conference on Microelectronics, Electromagnetics and Telecommunications. The conference was held during 18–19 December, 2015 at Department of Electronics and Communication Engineering, GITAM Institute of Technology, GITAM University, Visakhapatnam, India. The objective of this international conference was to provide an opportunity for researchers, academicians, industry persons and students to interact and exchange ideas, experience and expertise in the current trend and strategies in the field of Microelectronics, Electromagnetics and Communication Technologies. Besides this, participants were also enlightened about vast avenues and current and emerging technological developments in the field of Antennas, Electromagnetics, Telecommunication Engineering, and Low Power VLSI Design. The conference attracted a large number of high-quality submissions and stimulated cutting-edge research discussions among many academic pioneering researchers, scientists, industrial engineers, and students from all around the world and provided a forum to researchers. Research submissions in various advanced technology areas were received and after a rigorous peer-review process with the help of programme committee members and external reviewers, 73 papers were accepted with an acceptance ratio of 0.33.

The conference featured distinguished personalities that include Dr. Lipo Wang (Nanyang Technological University, Singapore), Dr. V. Bhujanga Rao (Distinguished Scientist and Director General, Naval Systems and Materials), Prof. G.S.N. Raju (Vice Chancellor, Andhra University), Dr. Aditya K. Jagannadham (IIT Kanpur), Dr. Sanjay Malhotra (BARC, Trombay), Dr. Samir Iqbal (University of Texas, Arlington, USA), Dr. D. Sriram Kumar (NIT Trichy), Dr. P.V. Ananda Mohan (ECIL, Bangalore), Dr. G. Radha Krishna (IIT Madras), Mr. Rajan A. Beera (Global Director of Engineering, Cortland, NY), and Mr. G.S. Rao (Managing Director—Technology, Accenture). Separate invited talks were organized in industrial and academia tracks on both days. The conference also hosted a few tutorials and workshops for the benefit of participants. We are indebted to the management of Springer Publishers, GITAM University, for their immense support

to make this conference possible at such a grand scale. A total of 13 sessions were organized as a part of ICMEET 2015 including ten technical, two plenary and one inaugural session. The Session Chairs for the technical sessions were Mrs. D.R. Rajeswari (Scientist-F, NSTL), Dr. V.S.S.N.S. Baba (Prutvi Electronics, Hyderabad), Dr. B. Prabhakar Rao (JNTU, Kakinada), Dr. S Srinivasa Kumar (JNTU, Kakinada), Dr. G. Sasibhushana Rao (Andhra University), Dr. P. Mallikarjuna Rao (Andhra University), Dr. P. Rajesh Kumar (Andhra University), Dr. P.V. Sridevi (Andhra University), Dr. A. Mallikarjuna Prasad (JNTU, Kakinada), Dr. N. Balaji (JNTU, Vizianagaram), Dr. Ch. Srinivasa Rao (JNTU, Vizianagaram), Dr. B. Tirumala Krishna (JNTU, Vizianagaram), Dr. Ibrahim Varghese (NSTL, Visakhapatnam), Dr. N. Bala Subrahmanyam (GVPCE, Visakhapatnam), Dr. M. Sai Ram (GVPCE, Visakhapatnam), and Dr. P. Ramana Reddy (MVGR College of Engineering, Vizianagaram).

We express our sincere thanks to members of the technical review committee and the faculty of Department of ECE, for their valuable support in doing critical reviews to enhance the quality of all accepted papers. Our heartfelt thanks are due to the National and International Advisory Committee for their support in making this a grand success. Our authors deserve a big thank you as it is due to them that the conference was such a huge success.

Our sincere thanks to all sponsors, press, print, and electronic media for their excellent coverage of this convention.

December 2015

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Subthreshold Operation of Energy Recovery Circuits

D. Jennifer Judy and V.S. Kanchana Bhaaskaran

Abstract This paper introduces a novel design methodology i.e. adiabatic subthreshold mode which inherits the features of both the subthreshold logic and the adiabatic (or the energy recovery) circuits. In this paper, analysis of essential digital gates is done for the three modes of operation namely, (1) subthreshold (2) adiabatic and (3) adiabatic subthreshold operation. The simulation results validate the benefits obtained in terms of the reduced energy consumption in the adiabatic subthreshold mode, making it suitable for ultra low power and medium throughput (10 kHz–1 MHz) applications. Specifically, it has been emphasized that the non-adiabatic dissipation that is prevalent in adiabatic circuits is almost discarded in the proposed mode. And, the challenges faced by the methodology are mitigated by the circuit level technique of upsizing the channel. Berkeley Predictive Technology Model (BPTM) 45 nm technology node has been used in the simulation studies on industry standard Spice tools.

Keywords Subthreshold · Device sizing · Adiabatic subthreshold · Nonadiabatic dissipation

1 Introduction

Generally, in a CMOS inverter, if $IN = 0$ and V is the supply voltage, only $½CV^2$ is delivered to the load capacitance for $OUT = 1$. The remaining $½CV^2$ is dissipated in the circuit transistors. Here, C represents the nodal capacitance. Then, when input signal IN becomes 1, the $½CV^2$ stored in the load capacitor is dissipated to the ground [1]. On the other hand, in the adiabatic logic, a time varying supply clock,

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called as *power-clock* is used, that reduces the voltage drop across the device at any time. The majority of the energy spent on charging the nodal capacitance is recycled back to the supply clock every time and is not dissipated to the ground as it occurs in CMOS. Hence, these circuits are called as *Adiabatic circuits.* This energy recovery property greatly reduces the switching power of the digital circuits. However, in the quasi-adiabatic circuits that consists of cross coupled PMOS transistors or cross coupled inverters at the outputs there is significant amount of non-adiabatic dissipation. This is due to the fact that the transistor helping in energy recovery remains *ON* only till the gate voltage is below its threshold voltage. When the output voltage reaches the threshold value of V_T, the recovery path transistor becomes *off* and no further energy recovery takes place. This contributes for the $½CV_{th}^2$ power dissipation, which happens every time when the input signal switches. This non adiabatic energy dissipation is a major setback in the Quasi adiabatic structures.

On the other hand, in the subthreshold logic, device sizing is done in such a way that they are operated with $V_{DD} < V_{th}$. In this weak inversion region, the leakage current or the subthreshold current is considered the computation current. It helps in surmounting the $½CV_{th}^2$ power dissipation drawback of the adiabatic circuits. Moreover, the exponential I-V relationship in the subthreshold region of operation increases the current gain. However, it is to be pointed out that, although the switching power is greatly reduced, subthreshold circuit operations are intended mainly for medium throughput applications. Additionally, due to the exponentially increasing current gain, the sensitivity of the circuit to the process and temperature variations increases. Nevertheless, the robustness of the circuit has been improved by different circuit level and device level techniques.

In this paper, it is proposed to utilize the advantages of both the subthreshold logic operation and the energy recovering adiabatic logic and launch a new mode of operation called *adiabatic subthreshold mode*. In adiabatic subthreshold mode of operation, the adiabatic circuit is device-sized to operate with the supply clock below the threshold value, i.e., in the weak inversion region. Here, the non-adiabatic dissipation discussed above is reduced to a bare minimum. Moreover, in this mode the process of near complete energy recovery property enhances the lower power operation capability even better than the conventional CMOS subthreshold operation. Further, the multi phase power-clocking in the adiabatic circuits assist in efficient pipelining due to their inherent nature of each clock lagging behind the other by 90^o, with the successive power-clocks operating the cascade of circuits. The pipelining adopted in the adiabatic structures, may improve the throughput of the novel mode far better than the subthreshold circuits.

In this paper, the basic digital logic gates such as inverter, NAND, NOR, XOR, AND and OR shown in Fig. 1 are analysed for all the above three modes of operations to validate the claims. Each of the claim and the simulation outcomes are substantiated with necessary analytical support and conceptual clarification. Further, the proposed adiabatic subthreshold mode is illustrated with a 4 stage, 8 stage and 16 stage cascaded inverter chain to prove the operation of the adiabatic subthreshold operation with increased logical depth or higher latency.

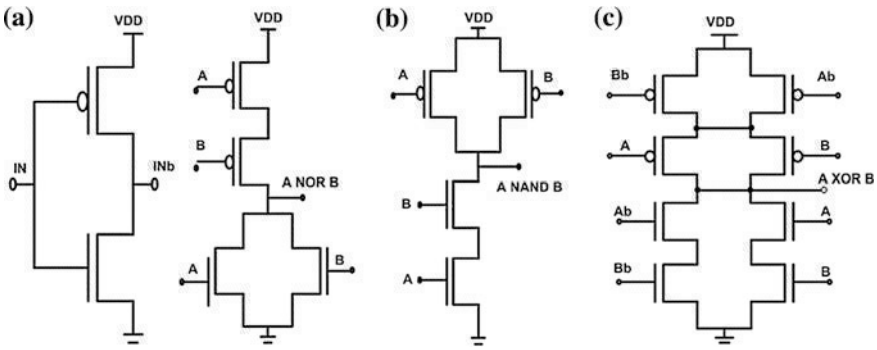

Fig. 1 Basic CMOS digital logic gates device sized for subthreshold operation **a** NOT, **b** NOR, **c** NAND

Section 2 discusses the device sizing and the impacts of subthreshold operation of the above mentioned basic digital logic gate circuits. Section 3 explains the circuit counterparts operated in adiabatic mode and detail out the features and benefits. Section 4 elaborates the adiabatic subthreshold mode of operation of the circuits listed in Sect. 3. Section 4 exemplifies a 4 stage, 8 stage and 16 stage cascaded inverter chain operated in all the three modes. Section 5 presents the simulation results, discussions and the analysis depicting the justification and validation. Section 6 concludes and the scope for the future work is also discussed.

2 Subthreshold Operation

2.1 Device Sizing

Scaling down of V_{dd} below the value of threshold voltage, for ultra low power designs require optimal sizing of transistors for accurate functionality, minimum delay, minimum power consumption and also symmetrical noise margin [2]. Thus, there is a need to obtain an optimal size ratio $\rho = (W/L)_P/(W/L)_N$. Changing ρ is done by changing the width of the transistors maintaining the length constant ($\rho = (W_p + \Delta W_p)/L_p/(W_n + \Delta W_n/L_n)$. PMOS transistor is made larger with respect to the NMOS device, maintaining the total size of the logic gate constant. Hence, in effect, C_L is maintained constant, to maintain the power dissipation of the gate also constant. Since the gate oxide capacitances contributing to the C_L is the same per unit area for both the PMOS and NMOS transistors, the energy does not vary so much. However ρ affects the delay, power and noise margin as follows.

- Increased width of the transistor will reduce the propagation delay due to the increased current. i.e., larger PMOS and smaller NMOS will give low t_{pLH}. However, it will increase t_{pHL}. Weaker PMOS and larger NMOS will result in reduced t_{pHL} and increased t_{pLH}.

- Changing ρ further changes the miller parasitic capacitance and hence the load capacitance C_L. This affects the total power consumption.
- Smaller PMOS and larger NMOS give reasonable noise margin low level *NML* and reduce t_{pHL} and the static power. However, larger PMOS and smaller NMOS improve *NMH* and reduce the t_{pLH}, however, at the cost of increased static power. Here, $NML = V_{IL} - V_{OL}$ and $NMH = V_{OH} - V_{IH}$.

Hence, in the presented work, an optimal size ratio ρ is designed for realizing minimum delay, minimum power consumption and reasonable noise margin characteristics. Thus, the device sizing is fixed as $\rho = (W_P = 135\ nm/L_P = 45\ nm)/(W_N = 65\ nm/L_N = 45\ nm)$ after analysing with various aspect ratios in the process corner models Fast PMOS/Slow NMOS and Slow NMOS/Fast PMOS for wide range of supply voltages below the threshold value $V_T = 0.61$ V.

2.2 Subthreshold Circuits

Subthreshold operation employs the leakage current as the operation current by maintaining the supply voltage $V_{dd} < V_{TH}$. The I-V characteristics of the devices in the weak inversion region are entirely different from the strong inversion region as shown in Fig. 2.

The weak inversion current has an exponential behaviour in contrast to the linear behaviour of the strong inversion region operation. The subthreshold current is given by the equation

$$I_{sub} = I_o \times e^{((VGS-VTH/nvt))} \times (1 - e^{(-VDS/vt))} \times e^{\eta VDS/nvt} \quad (1)$$

$$I_o = \mu_o C_{ox} \times W/L(n-1)vt^2 \quad (2)$$

Here, V_{GS} is the transistor gate to source voltage, V_{DS} is the drain to source voltage, V_{TH} is the threshold voltage, v_T is the thermal voltage, η is the DIBL

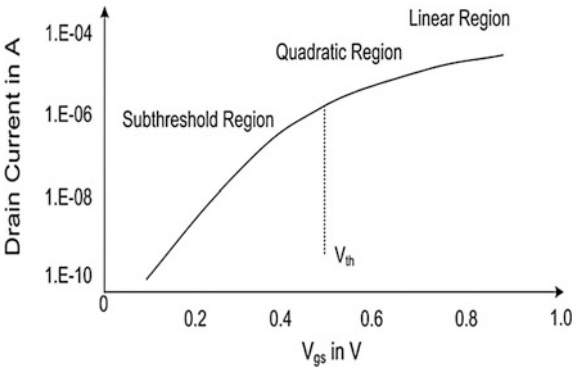

Fig. 2 Exponential behaviour of the drain current in the subthreshold region

coefficient, n is the subthreshold swing coefficient of the transistor, μ_o is the zero bias mobility, C_{ox} is the gate oxide capacitance, W and L are the width and length of the transistor respectively [3]. The equation signifies the exponential dependence of the subthreshold current on V_{DS}. This is the reason for the high transconductance gain of the circuit and the ideal VTC characteristics of the gate.

In the super-threshold region, a transistor enters the saturation region only when $V_{DS} > V_{GS} - V_T$ which gives a much narrower saturation region and thus an undesirable voltage transfer characteristic (VTC). However, the devices in the subthreshold region, the drain current saturates and becomes independent of V_{DS} for $V_{DS} > 3kT/q$ ($\sim$78 mV at 300 K). Hence, the devices are good current sources in the subthreshold region in the operating voltage range of $3kT/q$ to V_{dd} [4, 5].

Furthermore, the exponential dependence of the drain current on the V_{GS} voltage increases the sensitivity of the circuit to the process and temperature variations and hence, the robustness of the device is declining which is one of the challenges faced in the subthreshold circuits. An added consequence of the subthreshold region is the decrease in the input gate capacitance, where the gate capacitance is given by

$$Ci = series(C_{ox}, C_d)||C_{if}||C_{of}||C_{do} \tag{3}$$

Here, C_{ox}, C_d are the oxide and depletion capacitances, C_{if} and C_{of} are the fringe capacitances and C_{do} is the overlap capacitance. The second order effects of the MOS devices are also less pronounced in the subthreshold region. The subthreshold currents are weaker and hence, the time taken for charging and discharging the nodal capacitance is longer, as given by

$$T_d = C_L V_{DD}/I_{on} \tag{4}$$

Thus, operating the devices in the weak inversion region exhibits several benefits such as 1. High current gain 2. Lower power dissipation 3. High noise margin 4. Low input gate capacitance 5. Reduced gate tunnelling current, Gate induced drain leakage and reverse biased diode leakage. However, the sensitivity of the subthreshold circuits to the PVT variations and the low throughput of the devices operating in the subthreshold regime are major obstacles that need to be eradicated to acquire the benefits [6, 7]. The robustness of the circuits can be enhanced by various circuit level and device level techniques such as channel upsizing and body biasing [8].

Extending the subthreshold logic to adiabatic circuits can improve power efficiency of the energy recovery circuits for ultra low power operation besides deriving several benefits from each of the low power schemes. In order to illustrate the claims on the proposed adiabatic subthreshold mode, CMOS basic digital logic gates (AND, NAND, OR, NOR, NOT, XOR) are device sized to operate in subthreshold region. And also, the adiabatic designs of logic gates are evaluated in the strong inversion and weak inversion region of operation (adiabatic subthreshold mode) as discussed in the subsequent sections.

3 Adiabatic Circuits

Figure 3a–c show the (Efficient Charge recovery Logic) ECRL adiabatic structures of the digital logic gates. In these adiabatic circuits, it is noted that the constant power supply V_{DD} of the conventional CMOS circuits is replaced with a power-clock, which is trapezoidal in shape with four phases, as shown in Fig. 4. The cascaded successive stages of the ECRL adiabatic gates are driven by the four phases of the power clock PCLK1, PCLK2, PCLK3 and PCLK4. This pipelining feature of the ECRL adiabatic architecture lessens the energy dissipated per stage and enhances the throughput [9, 10].

The time varying power clock reduces the potential across the switching devices at any time, and this minimizes the dissipation in the pull-up and pull-down transistor networks. The energy delivered to the circuit nodes during *Evaluate* phase is recycled back to the supply during the *Recovery* phase. The output nodal value is cascaded to the subsequent stage in the adiabatic pipeline during the Hold phase [11]. This adiabatic dissipation of the power-clocked circuit during the evaluating/recovery phase is given by

$$E_{adia} = R_{on} C_L / T C_L V_{DD}^2 \tag{5}$$

$$R_{on} = [\mu_{effpC_{ox}} W_{effp} / L_{effp} (V_{DD} - |Vthp|)]^{-1}. \tag{6}$$

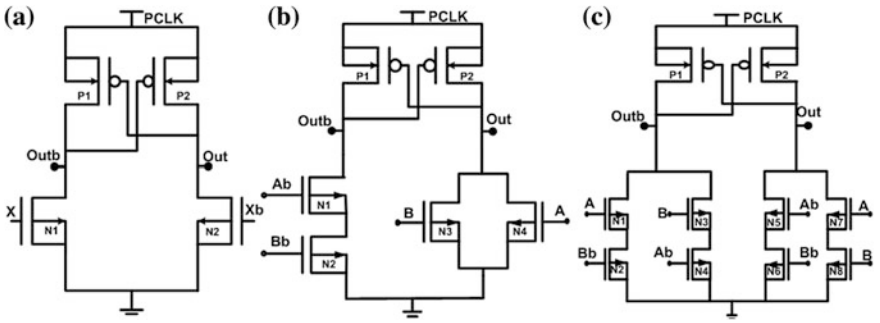

Fig. 3 ECRL **a** INV/BUF, **b** AND/NAND, **c** XOR/XNOR

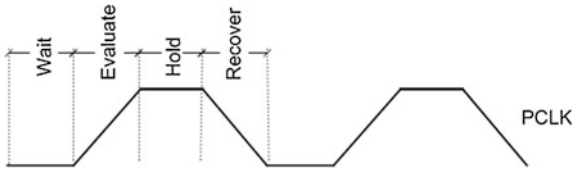

Fig. 4 Four phase power clock

where R_{on} is the ON resistance in the charging path, C_L is the load capacitance and T is the power clock period. However, there prevails a non-adiabatic component of power that is irrecoverable [12]. This is due to the fact that the PMOS transistors are maintained *on* only as long as its source voltage is more than the threshold voltage V_T [13]. The non adiabatic dissipation is the sum of energy components due to the V_{thp} and the leakage. i.e., $E_{nad} = E_{vthp} + E_{leakage.}$

It can be expressed by the equation as depicted below,

$$E_{nad} = 1/2C_L V_{thp}^2 + V_{DD}\mathrm{I_{leak}kT} \tag{7}$$

Then, the total energy loss E_{diss} per switching event of the adiabatic circuits is given by,

$$E_{diss} = 2\left(\frac{R_{on}C_L}{T}\right)C_L V_{DD}^2 + 1/2C_L V_{thp}^2 + V_{DD}I_{leak}kT \tag{8}$$

Expanding,

$$E_{diss} = 2C_L^2 V_{DD}^2\left[T\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{DD}|Vthp|)\right] + 1/2C_L V_{thp}^2 + V_{DD}I_{leak}kT \tag{9}$$

where n, V_T, μ, is subthreshold slope factor, thermal voltage and mobility of the leaking transistors respectively [14]. It is inferred from the Eqs. (7) and (9), the adiabatic power dissipation component decreases with reducing frequency, while the nonadiabatic dissipation is independent on frequency. This detrimental feature of the adiabatic circuits is subsisting at all frequencies and hence is a design constraint and need to be sorted out. Thus, there come into view the novel approach i.e. adiabatic subthreshold mode that inherits the features of the subthreshold and the adiabatic styles of operation. Consequently, this proposed mode also exhibits most of the benefits of both the techniques as detailed out in the next section.

4 Adiabatic Subthreshold Logic

This section presents the adiabatic subthreshold mode of operation, i.e., the adiabatic structures are operated in the weak inversion region. The adiabatic structures are device sized for subthreshold operation and power clock *PCLK* voltage is held below the threshold value V_T for operation in the weak inversion region. This novel methodology acquires most of the merits of both the low power schemes which is listed as below.

- The dynamic power dissipation $P_d = \alpha C_L V_{dd}^2 f$ is minimized as the nodal capacitance C_L is reduced by device sizing due to the reduction in the gate capacitances, V_{DD} being less than the threshold voltage and the power-clock period T being longer. (meaning lower power-clock frequency)
- Besides, absolute energy recovery made possible through the use of time varying power clock improves the power efficiency to a greater extent.
- And, most crucially it is also justified that the non-adiabatic power dissipation is also brought down to an utmost low value in the proposed mode as given by the Eq. (10).

$$E_{nad} = \frac{1}{2} C_L V_{thp}^2 + V_{DD} \mu C_{ox} \left(\frac{W}{L}\right) V_T^2 \exp^{Vgs - Vth/\eta V_T} kT \tag{10}$$

The non-adiabatic dissipation is dependent on 1. The power supply voltage PCLK that is now scaled down to a value below the threshold voltage 2. The nodal capacitance that is lessened by the reduction in the gate capacitance and 3. The value of threshold voltage that is come down to 3kT/q = 78 mV in the subthreshold region.

- Moreover, the gate tunneling current, reverse biased current DIBL, GIDL leakage currents are minimized due to their dependence on the supply voltage which is now below the threshold value.
- The weaker currents may increase the delay in the subthreshold mode and decrease the frequency of operation. However, the pipelining adopted in the adiabatic subthreshold circuits improves the throughput.
- Device optimization of the adiabatic circuits for subthreshold operation also improves the power delay product.
- Moreover, the current source property (drain current saturates at $V_{DS} > 3kT/q$) in the subthreshold region enables better pass gate logic or in other words reduces the voltage degradation in series connected devices. This is owing to the fact that the voltage drop across the devices is just the *3kT/q* drop ($\sim$78 mV) as against the full V_{th} value of around 700 mV.

The claims are exemplified with the basic digital gates and a 4 stage, 8 stage and 16 stage cascaded inverter chain in all the above three modes of operation analysed for power efficiency. A 4 stage inverter chain is depicted in Fig. 5 for better

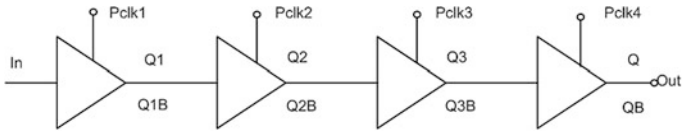

Fig. 5 Cascaded inverter chain

understanding in which the successive stages are driven by the four phases of the power clock. However, in the subthreshold mode, power clock will be replaced by a constant supply voltage V_{DD}.

5 Simulation Results and Analysis

The circuits are designed using the BPTM 45 nm process technology models and are simulated using TSPICE. The basic CMOS digital logic gate circuits shown in Fig. 2 are device sized (W_P = 135 nm; L_P = 45 nm) (W_N = 65 nm; L_N = 45 nm) to operate with a constant V_{DD} set at value 0.4 V for subthreshold operation. And, four-phase trapezoidal power-clocks with peak-to-peak voltage of 1.1 v (V_T = 0.61 v) are used to power up the ECRL circuits for the adiabatic mode of operation. Also, the ECRL circuits are device sized to operate with the time varying power clocks PCLK1, PCLK2, PCLK3 and PCLK4 fixed at peak to peak value of 0.4 V. Thus the power dissipation results so obtained in all the three modes of operation, i.e., subthreshold logic, adiabatic logic and adiabatic subthreshold logic for the basic logic gates have been depicted in Fig. 6.

The graph in Fig. 6 portrays the reduced dynamic power dissipation in the proposed mode due to smaller operating voltage, less nodal capacitance and reduced operating frequency.

Further, it has already been stated that the voltage degradation of series connected devices is reduced in subthreshold operation due to the current source property in the weak inversion region. Thus the logical depth that can be attained in the adiabatic subthreshold mode can defensed with simulation of the 4 stage, 8 stage and 16 stage inverter chains. The power results are plotted in Fig. 7. On comparison, the 16 stage inverter in the subthreshold operation consumes 570 nW, while the dynamic power dissipation incurred by the proposed subthreshold adiabatic counterpart decreases to 27 nW. Thus, a power efficiency of 95 % is realized in the novel mode of operation.

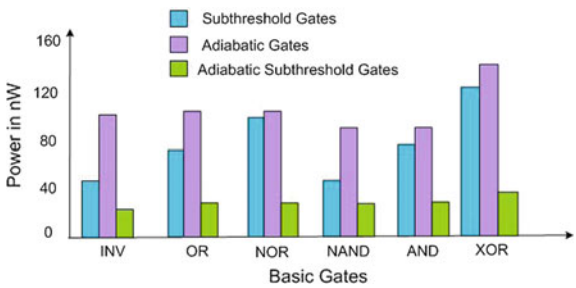

Fig. 6 Simulation results of the gates in the subthreshold, adiabatic, adiabatic subthreshold modes of operation

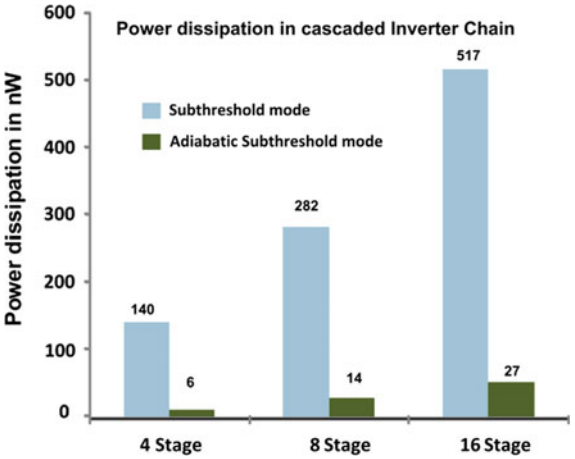

Fig. 7 Simulation results of the power dissipation of the cascaded inverters

The frequency range of operation of adiabatic subthreshold circuits is held at 10 kHz–1 MHz and this improved throughput is mainly by the pipelining feature adopted in the ECRL architecture. This makes the subthreshold circuits suitable for medium throughput applications.

And also, it is clear that in the adiabatic mode when the power-clock reaches the threshold voltage during its negative ramping (or recovery phase); the recovery transistor is cut-off, leaving $1/2C_L V_{thp}^2$ of power dissipation unrecovered. This non adiabatic dissipation is narrowed to the least in the proposed mode. As inferred from Eq. (10), it is explicit that the scaled supply voltage, the threshold voltage which is now reduced to 3kT/q (=78 mV) instead of V_T (0.61 V) and the decreased leakage currents diminishes non-adiabatic component in the total power dissipation. The above analytical argument is proven with the simulation results of the 16 stage cascaded inverter chain shown in Fig. 8. It is validated that the inherent non adiabatic dissipation is 1600 nW in the adiabatic logic and reduced to 25 nW in the

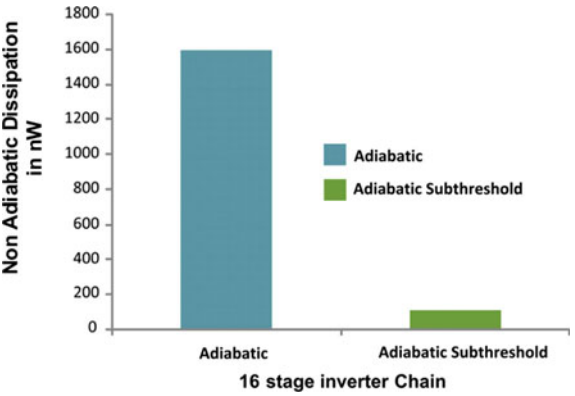

Fig. 8 Non adiabatic power dissipation of a 16 stage inverter chain