Chi-Wah Kok | Wing-Shan Tam

CMOS Voltage References

An Analytical and Practical Perspective

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AN ANALYTICAL AND PRACTICAL PERSPECTIVE

Chi-Wah Kok and Wing-Shan Tam

Canaan Microelectronics Corporation Ltd, Hong Kong

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CONTENTS

About the Authors ix

Preface xi

Acknowledgements xiii

Nomenclature xv

1 Warm Up 1

1.1 Bipolar Junction Transistors 2
1.1.1 Differential V_{BE} 5
1.2 Metal-Oxide Semiconductor Field-Effect Transistor 7
1.2.1 Cutoff Region 11
1.2.2 Subthreshold Conduction 11
1.2.3 Triode Region 14
1.2.4 Saturation Region 16
1.2.5 Thermal Properties 19
1.2.6 Channel Length Modulation Effect 23
1.3 Diode 23
1.4 Resistor 25
1.4.1 Dummy Element 27
1.4.2 Guard Ring 27
1.4.3 Sheet Resistance 27
1.5 Device Matching 28
1.5.1 Application of Statistics to Circuit Design 28
1.5.2 Systematic Variation 30
1.6 Simulation Models for Circuit Design 31
1.6.1 Process Variation and Typical Design 32
1.6.2 Process Corners 34
1.7 Noise 36
1.7.1 Types of Noises 36
1.7.2 Sums and Multiplications of Noises 38
1.8 Fabrication Technology 39
1.9 Book Organization 40
1.10 Exercises 42
References 46

2 Voltage Reference **49**
2.1 Performance Measures 49
2.1.1 Line Regulation 51
2.1.2 Temperature Coefficient 54
2.1.3 Power Supply Rejection Ratio 56
2.1.4 Quiescent Current 59
2.1.5 Output Noise 60
2.2 Other Design Considerations 62
2.3 Summary 63
2.4 Exercises 65
References 70

3 Bandgap Voltage Reference **71**
3.1 Widlar Bandgap Voltage Reference Circuit 71
3.2 Drain Voltage Equalization Current Mirror 74
3.2.1 Opamp Based β-Multiplier Bandgap Voltage Reference Circuit 76
3.2.2 Bandgap Voltage Reference Circuit 77
3.3 Major Circuit Elements 81
3.3.1 Operational Amplifier 81
3.3.2 Current Mirror 86
3.3.3 Startup Circuit 88
3.3.4 Resistor Network 93
3.3.5 Bipolar Transistor 94
3.4 Complete Layout 95
3.5 Summary 95
3.6 Exercises 96
References 101

4 Error Sources in Bandgap Voltage Reference Circuit **103**
4.1 Non-Ideal Opamp 103
4.1.1 Input Offset Voltage 104
4.1.2 Limited Gain and Power Supply Rejection Ratio 112
4.1.3 Noise 113
4.2 Current Mirror Mismatch 114
4.2.1 Channel Length Modulation Effect Compensation 116
4.2.2 Cascode Current Mirror 117
4.3 Bipolar Transistor 122
4.3.1 Size Variation 122
4.3.2 Series Base Resistance 122
4.3.3 β Variation 125
4.4 Resistor Variation 126
4.5 Power Supply Variation 127
4.5.1 Pre-Regulation 132
4.6 Output Loading 135
4.7 Output Noise 138
4.8 Voltage Reference Circuit Trimming 140

4.8.1 Linked Fuse Resistor Trimming 141
4.8.2 Resistor Trimming Circuit Analysis 142
4.8.3 Modulated Trimming 146
4.8.4 Voltage Domain Trimming 148
4.8.5 Current Domain Trimming 149
4.9 Summary 149
4.10 Exercises 151
References 161

ADVANCED VOLTAGE REFERENCE CIRCUITS

5 Temperature Compensation Techniques 165
5.1 $V_{BE} - \Delta V_{BE}$ Compensation 166
5.1.1 Brokaw Bandgap Voltage Reference 168
5.1.2 β-Multiplier $V_{BE} - \Delta V_{BE}$ Compensation 170
5.2 Widlar PTAT Current Source and V_{BE} Compensation 175
5.3 V_{GS} Based Temperature Compensation 177
5.3.1 V_{GS} Current Source 178
5.4 Summary 182
5.5 Exercises 183
References 189

6 Sub-1V Voltage Reference Circuit 191
6.1 Sub-1V Output Stage 193
6.2 Voltage Headroom in Opamp based β-multiplier Voltage Reference Circuit 195
6.2.1 Opamp with NMOS Input Stage 197
6.2.2 Local Voltage Boosting 198
6.2.3 Low V_{th} Transistor 198
6.2.4 Bulk-Driven Transistors 199
6.3 Sub-1V Bandgap Voltage Reference by Resistive Division 199
6.3.1 Resistive Divided V_{BE} 202
6.3.2 Independent Biased Resistive Divided V_{BE} 206
6.4 Peaking Current Source and V_{BE} Compensation 209
6.5 Weighted ΔV_{GS} Compensation 211
6.6 Summary 214
6.7 Exercises 215
References 222

7 High Order Curvature Correction 223
7.1 Compensation Order 224
7.2 Second Order Temperature Compensation 228
7.2.1 Second Order Current Source 229
7.2.2 Current Subtraction 232
7.2.3 Current Addition 236
7.3 BJT Current Subtraction 238
7.4 Piecewise Linear Compensation 240

7.5 Sum and Difference of Sources with Similar Temperature Dependence 243
7.5.1 Difference of Voltages with Similar Temperature Dependence 244
7.5.2 Sum of Voltages with Inverted Temperature Dependence 245
7.5.3 Multi-threshold Voltages Curvature Compensated Voltage Reference 247
7.6 Summary 252
7.7 Exercises 253
References 257

8 CMOS Voltage Reference without Resistors 259
8.1 Generation of Weighted PTAT Source By Inverse Functions 260
8.1.1 Weighted Differential Circuit 260
8.1.2 Negative Impedance Converter 262
8.2 Resistorless Voltage and Current Sources 265
8.2.1 Resistorless Voltage Source 265
8.2.2 Resistorless Current Source 266
8.3 First Order Compensated Resistorless Bandgap Voltage Reference Circuit 268
8.3.1 Voltage Summation Based Resistorless Reference Circuit 269
8.3.2 Current Summation Based Resistorless Reference Circuit 270
8.4 Resistorless Sub-Bandgap Reference Circuit 270
8.4.1 The Voltage Summation Approach 271
8.4.2 CTAT Voltage Reduction 273
8.5 Summary 279
8.6 Exercises 280
References 281

A SPICE Model File 283

B SPICE Netlist of Voltage Reference Circuit 287

Index 289

ABOUT THE AUTHORS

Chi-Wah Kok was born in Hong Kong. He was granted a PhD degree from the University of Wisconsin Madison. Since 1992, he has been working with various semiconductor companies, research institutions, and universities, which include AT&T Labs Research, Holmdel, SONY U.S. Research Labs, Stanford University, Hong Kong University of Science and Technology, Hong Kong Polytechnic University, City University of Hong Kong, Lattice Semiconductor, etc. In 2006, he founded Canaan Microelectronics Corp Ltd., a fabless IC company with products in mixed signal IC for consumer electronics. Dr. Kok embraces new technologies to meet the fast changing market requirements. He has extensively applied signal processing techniques to improve the circuit topologies, designs, and fabrication technologies within Canaan. This includes the application of semidefinite programming to circuit design optimization, abstract algebra in switched capacitor circuit topologies improvement, and nonlinear optimization methods to optimize high voltage MOSFET layout and fabrication.

Wing-Shan Tam was born in Hong Kong. She received her BEng degree in electronic engineering from The Chinese University of Hong Kong, MSc degree in electronic and information engineering from The Hong Kong Polytechnic University, and PhD degree in electronic engineering from the City University of Hong Kong in 2004, 2007, and 2011, respectively. Currently, she is the Engineering Manager of Canaan Microelectronics Corp Ltd. Her research interests include mixed-signal integrated circuit design for data conversion and power-management.

PREFACE

This book has a genesis: It started as internal training material for engineers working in Canaan Microelectronics Corp. Ltd. It is also a monograph because it presents the outcome of our research and teaching activities in the field of temperature independent circuit design at both the Canaan Microelectronics Corp. Ltd. and the City University of Hong Kong. Many unpublished works are included in this book. Numerous design examples are also presented together with detailed discussions on design principles, performance analysis, and the potential problems of each circuit topology. This book is intended to be course material for senior and graduate level courses, training material for engineers, and also a reference text for readers who are working in the field of temperature independent circuit design.

The book is divided into eight chapters. The first chapter offers an introduction of device physics focusing on the temperature properties of individual devices, which introduces just enough material for voltage reference circuit design and analysis. Details of general device physics may be gathered from existing literature, such as the textbooks by Chenming C. Hu, (*Modern Semiconductor Devices for Integrated Circuits*, Prentice Hall, 2010), and S.M. Sze, (*Physics of Semiconductor Devices*, Wiley, 1969) that offer detailed discussions on the device physics for bipolar transistors, MOS transistors, and other passive components manufactured in the CMOS process. Besides the physics, towards the end of Chapter 1, we also discuss practical issues in CMOS circuit design. The device matching problem is introduced. Computer simulation for circuit design with process variations is discussed. Finally, the device noise models that describe the noises associated with CMOS devices are presented. Chapter 2 presents the performance characterization of voltage reference circuits. The presented characterization will be used throughout the book in the analytical discussions and performance comparisons of individual voltage reference circuits. A general voltage reference circuit framework of opamp based β-multiplier bandgap voltage reference is presented in Chapter 3. The presented voltage reference circuit is silicon proven, and has been applied to a power management IC of Canaan Microelectronics Corp. Ltd.: the micrograph of the die is shown on the front page of this book. Every building block within the voltage reference circuit is discussed analytically together with layout details. Various error sources of the circuit are identified, and analyzed in Chapter 4. Methods to remedy each problem together with their pros and cons are discussed in detail in Chapter 4. The basic PTAT-CTAT temperature compensation technique discussed in Chapter 4 will be extended to voltage reference circuits using various temperature dependent devices and topologies in Chapter 5. Analytical derivation to determine the component values of each device within the voltage reference circuit, together with the important design considerations of each circuit and topology will be discussed. Chapter 6 discusses the design of voltage

reference circuits with sub-1V supply, and voltage reference circuits with sub-1V reference voltage. Notice that the design of the voltage reference circuit with a sub-1V reference voltage is different from that of the voltage reference circuit with a sub-1V supply voltage. A voltage reference circuit with a sub-1V supply voltage is also a voltage reference circuit with a sub-1V reference voltage. The voltage reference circuit with sub-1V reference voltage being able to operate with a sub-1V supply voltage is important in modern CMOS circuit design where the supply voltage keeps reducing for power reduction and silicon size shrinkage. A number of sub-1V voltage reference circuits will be discussed in this chapter.

High order curvature compensated voltage reference circuits are presented in Chapter 7, which are important to applications that require a reference voltage with low temperature sensitivity. A number of high accuracy voltage reference circuit topologies, including high order curvature compensation, inverted temperature compensation, and piecewise temperature compensation etc. are discussed. This book concludes in Chapter 8 with a discussion on a type of special voltage reference circuit that does not require resistors. Such a voltage reference circuit has the advantage of compact layout. The performance of a resistor free voltage reference circuit can be further optimized with applications of piecewise temperature compensation technique to lower the temperature sensitivity of the circuit. Post-fabrication trimming circuits are discussed to reduce the reference voltage variation.

A detailed summary of the state of the art development with respect to the topic of each chapter is presented in the "*Summary*" section of each chapter. Homework problems are presented in the "*Exercise*" section in individual chapter. The homework includes both analytic problems, and SPICE based computer simulation exercises. While the process parameters used in this book and also in developing the exercises may not be the same as those in your institution, it is our hope that the exercises will provide you with general guidelines, analysis, design and layout experience for the design of the voltage reference circuits with the help of SPICE. The experience will further address the performance evaluation of the voltage reference circuit which will help you to achieve a thorough consideration of the voltage reference circuit before the actual design.

The development of voltage reference circuits is still continuing and therefore a book, such as this one, cannot be definitive or complete. It is hoped, however, that this book will fill an important gap; students embarking upon mixed-signal circuit design should be able to learn sufficient basics before tackling journal papers, researchers and engineers in the field of temperature independent/dependent circuit design should be able to use it as reference to assist their circuit design tasks, and current researchers in the field should be able to get a broad perspective on what has been achieved. The subject area is introduced, some major developments are recorded, and enough successes as well as challenges are noted here for readers to look into other voltage independent/dependent circuit design problems and generate solutions for their own problems.

Chi-Wah Kok and Wing-Shan Tam
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We are in debt to many people, too numerous to mention. To all the scholars who have influenced us, both in person or through their works, we acknowledge our indebtedness and express our great appreciation. Perhaps the most noteworthy was Prof. Hei Wong of the City University of Hong Kong whose knowledge, enthusiasm in advanced microelectronics research and development, and generous support in the course of the development of this book has surely inspired and greatly assisted us. We are proud to say that Prof. Wong is one of our greatest role models.

Dr. Kok would like to take this chance to claim victory in the competition with his wife Dr. Annie Ko on who will be the first to complete his/her second textbook. It was this competition that provided Dr. Kok with the extra boost to get this book finished with his best effort. Dr. Kok is also very happy to collaborate with Dr. Tam on this book project, who has always been his best collaborator in both the academic and business spheres. Dr. Tam is truly indebted and grateful to her parents, Simon Tam and Gloria Lee, for their love, encouragement, and their constant support in all her pursuits, including her PhD study and the completion of this book. Dr. Tam would also like to thank her beloved family, especially her sister and grandmother, who are always willing to share her stress and happiness. Finally, Dr. Tam would like to express her sincere gratitude to Dr. Kok, who introduced her into the world of IC design. Dr. Tam is very grateful for the opportunity to coauthor this book and treasures other aspects of her partnership with Dr. Kok too. Coauthoring a book is never easy. In the course of the development of this book, the authors have learned a lot from each other, and adapted to each others' working and learning styles. We are looking forward to seeing our excellent partnership extend to future book and other research and development projects.

Despite the assistance, review, overseeing, and editing of so many people, we have no doubt that errors still lurk undetected. These are ours alone, and it is our hope that the reader of this book will discover them and bring them to our attention, so that they all may be eradicated.

Chi-Wah Kok and Wing-Shan Tam

NOMENCLATURE

SoC	System-On-Chip
ATE	Automatic test equipment
J	Joule
Col	Coulomb
K	Kelvin
°**C**	degree Celsius
V_T	Thermal voltage, kT/q
V_{DD}	Positive supply voltage
V_{SS}	Negative supply voltage
BJT	Bipolar Junction Transistor
I_B	Base Current of Bipolar Transistor
I_C	Collector Current of Bipolar Transistor
I_E	Emitter Current of Bipolar Transistor
I_S	Saturation Current of Bipolar Transistor
J_C	Collector Current Density of Bipolar Transistor
J_S	Saturation Current Density of Bipolar Transistor
V_{BE}	Base-Emitter Voltage of a BJT
V_{CE}	Collector-Emitter Voltage of a BJT
R_B	Zero-bias base ohmic resistance
R_E	Emitter resistance
R_C	Collector resistance
V_{G0}	Silicon Bandgap Voltage Extrapolated at 0 K
A_E	Emitter Area of Bipolar Transistor
W_B	BJT base width
β	Forward current gain
V_D	Forward-bias diode voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-Channel MOSFET
PMOS	P-Channel MOSFET
CMOS	Complementary Metal Oxide Semiconductor
W	MOSFET Gate Width
L	MOSFET Gate Length
S	Channel Width to Length Ratio (W/L) of a MOSFET
I_{DS}	Drain to Source Current of a MOSFET

$I_{D,sub}$	Drain to Source Current of a MOSFET biased in subthreshold mode
$I_{D,lin}$	Drain to Source Current of a MOSFET biased in triode mode
$I_{D,sat}$	Drain to Source Current of a MOSFET biased in saturation mode
$I_{D,leak}$	Drain to Source Leakage Current or Off Current of a MOSFET in cutoff mode
$\hat{I}_{leak}$	Unit Drain to Source Current Normalized by S
ζ	Subthreshold Slope
ζ_n	Subthreshold Slope of a n-channel MOSFET
ζ_p	Subthreshold Slope p-channel MOSFET
C_D	Depletion capacitance of a MOSFET
C_{ox}	Gate oxide capacitance per unit area of a MOSFET
t_{ox}	Thickness of gate oxide
V_{th}	Threshold voltage of a MOSFET
V_{GS}	Gate source voltage of a MOSFET
V_{DS}	Drain source voltage of a MOSFET
$R_{DS,sub}$	Drain source resistance of a MOSFET in subthreshold mode
$V_{DS,sub}$	Drain source voltage of a MOSFET in subthreshold mode
$V_{DS,lin}$	Drain source voltage of a MOSFET in linear mode
$V_{DS,sat}$	Drain source voltage of a MOSFET in saturation mode
R_{DS}	Drain source resistance of a MOSFET
$R_{DS,lin}$	Drain source resistance of a MOSFET in linear mode
g_m	Transconductance of a MOSFET
$R_{DS,sat}$	Drain source resistance of a MOSFET in saturation mode
μ	Mobility of the charge carrier
CTAT	Complementary to Absolute Temperature
PTAT	Proportional to Absolute Temperature
V_{CTAT}	CTAT Voltage
I_{CTAT}	CTAT Current
V_{PTAT}	PTAT Voltage
I_{PTAT}	PTAT Current
V_{IN}	Input voltage to the voltage reference circuit
$V_{IN(nom)}$	Nominal input voltage to the voltage reference circuit
$V_{IN(min)}$	Minimum input voltage for proper operation of the voltage reference circuit
$V_{IN(max)}$	Maximum input voltage for proper operation of the voltage reference circuit
V_{REF}	Output voltage of the voltage reference circuit
$V_{DD(min)}$	Minimum operating supply voltage
$V_{DD(nom)}$	Nominal supply voltage
$V_{REF(nom),T}$	Output voltage of the voltage reference circuit at specific temperature T with respect to a range of input voltages
$V_{REF(min),T}$	Output voltage of the voltage reference circuit at $V_{IN(min)}$ and temperature T
$V_{REF(max),T}$	Output voltage of the voltage reference circuit at $V_{IN(max)}$ and temperature T
V_{η}	Noise source

$V_{REF_{CONV}}$	Reference voltage generated by conventional $V_{BE} - V_T$ temperature compensation voltage reference circuit
V_{DROP}	Dropout voltage defined as the voltage difference between the input and output voltage
T_{nom}	Nominal temperature
$V_\eta(f)$	Noise voltage at frequency f
T_{min}	Minimum temperature for proper operation of the voltage reference circuit
T_{max}	Maximum temperature for proper operation of the voltage reference circuit
$V_{REF(nom),V_{IN(nom)}}$	Output voltage of the voltage reference circuit at nominal input voltage with respect to a temperature range $[T_{min}, T_{max}]$
$V_{REF(max),V_{IN(nom)}}$	The maximum output voltage of the voltage reference circuit at nominal input voltage in the temperature range $[T_{min}, T_{max}]$
$V_{REF(min),V_{IN(nom)}}$	The maximum output voltage of the voltage reference circuit at nominal input voltage in the temperature range $[T_{min}, T_{max}]$
I_q	The quiescent current of the voltage reference circuit
TC	Temperature Coefficient
$PSRR$	Power supply rejection ratio
BW	System bandwidth of the voltage reference circuit
V_{OS}	Offset voltage
$\mathcal{S}_{PSRR}$	Power-supply rejection ratio that the variation of the reference voltage with a particular frequency in the input voltage
$\mathcal{S}_x^y$	Sensitivity of parameter y with respect to a change in parameter x
$\mathcal{S}_{LR}$	Linear regulation measure of variation of reference voltage with respect to a charge in input voltage to the voltage reference circuit
$\mathcal{S}_{TC}$	Temperature coefficient measure of variation of reference voltage with respect to a change in operation temperature of the voltage reference circuit

Table 1 Physical Constant

Parameter	Description	Typical Values
k	Boltzmann's Constant	1.38×10^2 J/K
q	Electron's Charge	1.62×10^{-19} Col
V_T	Thermal Voltage	$kT/q = 26$ mV at 300 K
B_{G0}	Silicon Bandgap Voltage Extrapolated at 0 K	1.206 V
V_{BE}	Base Emitter Voltage of NPN	0.73 mV at 300 K
V_{BE}	Base Emitter Voltage of PNP	0.76 mV at 300 K

1

Warm Up

The voltage reference circuits discussed in this book require you to work on electron devices by connecting together transistors, resistors, and capacitors. Therefore you need to understand the properties and limitations of each device in some detail. The easiest way to learn about electron devices is to study their physical models, although they are usually very complex. For example, the Gummel and Poon model of a bipolar transistor lists 45 parameters (Gummel and Poon, 1970) and yet still is not accurate enough to simulate the saturation or junction breakdown behaviors. The BSIM 3.3 model of a MOS transistor has more than 50 coefficients (Liu, 2001) not counting noise and gate leakage parameters. Although all of these variables are useful for the design of voltage reference circuits, only very few numbers and equations have to be remembered for creative work, and the shapes of a few dependencies and some qualitative relationships (not how much, but more or less, increasing or decreasing) of these parameters are much more important.

The following sections will present, from the authors' point of view, the most important electron device parameters necessary for voltage reference circuit design. Detailed descriptions of the operations of individual electron device can be found in textbooks on analog circuit design or device modeling (Hu, 2010; Sze, 1969). In particular, a large part of this book presents the design and analysis of a special kind of voltage reference circuit, the bandgap voltage reference. It is useful to know which parameters of the practical model dominate the behavior of each electron devices in the case of bandgap reference circuit design.

The well-known Gummel and Poon model for bipolar transistors, and BSIM 3.3 model for MOSFETs used in SPICE, will form the basis for the design and analysis of bandgap references. In particular HSPICE (*HSPICE® Simulation and Analysis User Guide* 2006), a typical SPICE simulator, will be used to produce all the simulation results presented in this book based on a 0.18 μm mixed signal CMOS process SPICE model. However, instead of going through SPICE, a minimum set of key parameters will be presented in the following sections which allow us to analytically describe the relation between various electron devices behaviors and their application to temperature insensitive circuit design. We shall start our discussions with the active components first, which include the bipolar transistors, MOSFETs, and diode, and then the passive components, which are the resistors made by different CMOS processes.

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1.1 Bipolar Junction Transistors

The bipolar junction transistor (BJT), is a vital component in the voltage reference circuit and is commonly used for the generation of temperature dependent voltage, whereas the generation of controllable temperature dependent voltage is the first step towards obtaining a temperature insensitive reference voltage. The BJTs can be implemented in a standard CMOS process. The simplified cross-view of a vertical NPN transistor and a vertical PNP transistor implemented in CMOS process are shown in Figure 1.1(a) and (b), respectively; while Figure 1.1(c) and (d) are the layouts of the transistors in Figure 1.1(a) and (b), respectively. In general, the NPN transistor is preferred because of its higher collector-current efficiency and the highly doped base region which can achieve a low series base resistance. The awkward effect of the base resistance will be discussed in Section 4.3.2. Besides, there are other limitations on the application of PNP transistor in voltage reference circuit. Consider the vertical PNP transistor illustrated in Figure 1.1(b), where the emitter is formed by a P-type region, the base is formed by a N-well, and the collector is formed by a P-type substrate. There are two limitations imposed on such BJT implementation. First, the collector is formed by the substrate, which is permanently tied to the lowest supply voltage. Second, the current gain of the transistor, β, is very low when compared to its NPN counterpart, which is defined as

$$\beta = \frac{I_C}{I_B}, \tag{1.1}$$

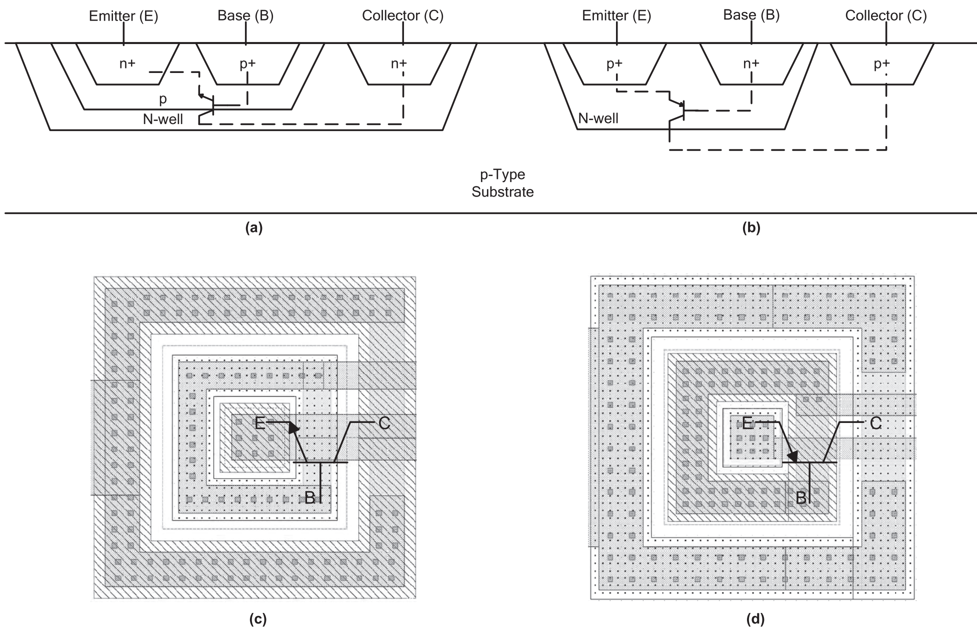

Figure 1.1 Integrated bipolar transistor in N-well CMOS processes: (a) a vertical NPN transistor and (b) a vertical PNP transistor. Layout examples of (c) NPN transistor in (a) and (d) PNP transistor in (b).

with I_C and I_B being the currents flowing into the collector and base of the BJT, respectively. To effectively alleviate the base resistance as a source of error in voltage reference circuit design, a high current gain ($\beta \geq 100$) is desired. As a result, the vertical PNP transistor is only applicable to voltage reference circuit design if we make it large to achieve a small base resistance. The last but not least, problem associated with the vertical PNP BJT is that it cannot be used in cascode structure because the collector is required to connect to the ground, and thus cannot be connected to the emitter of another BJT. Despite the above limitations, both the NPN and the PNP BJTs can be used in the voltage reference circuit.

The BJT applied in a voltage reference circuit is usually configured in a diode-connected structure (i.e., the base terminal and the collector terminal are connected together), such that the base-emitter voltage, V_{BE}, is used to provide a fixed junction voltage. However, the junction voltage is temperature sensitive, and thus cannot be used as reference voltage by itself. The thermal analysis of the BJT, and in particular the V_{BE}, has been widely discussed in the literature (Massobrio and Antognetti, 1993; Tsividis, 1980). The theory and notation of the NPN transistor are applicable to the PNP transistor with a few obvious modifications. Therefore, all the symbols and notations of these two types of BJTs are used interchangeably in our discussions.

If we neglect the Early effect, the collector current of a NPN transistor biased in the forward active region is given by

$$J_C(T)A_E = J_S(T)A_E \exp\left(\frac{V_{BE}}{V_T}\right),$$
$$I_C(T) = I_S(T)\exp\left(\frac{V_{BE}}{V_T}\right), \tag{1.2}$$

where A_E is the base-emitter junction area, T is the absolute temperature in K, $I_C(T)$ is the temperature dependent collector current, $J_S(T)$ is the saturation current density, which relates to the temperature dependent saturation current $I_S(T)$ as $I_S(T) = J_S(T)A_E$. Finally, the thermal voltage V_T is given by

$$V_T = \frac{kT}{q}, \tag{1.3}$$

with $q = 1.6 \times 10^{-19}$ Col being the electron charge, and $k = 1.38 \times 10^{-23}$J/°C being the Boltzmann constant. As an example, at $T = 300$ K, $V_T(300) = 0.0259$ V. Without going into further details of the semiconductor physics of BJT, we shall quote the base-emitter voltage function of the BJT from (Johns and Martin 1997).

$$V_{BE}(T) = V_{G0}\left(1 - \frac{T}{T_r}\right) + V_{BE}(T_r)\frac{T}{T_r} - \frac{\rho kT}{q}\ln\left(\frac{T}{T_r}\right) + \frac{kT}{q}\ln\left(\frac{J_C(T)}{J_C(T_r)}\right), \tag{1.4}$$

where V_{G0} is the bandgap voltage of silicon at 0 K which equals 1.206 V, ρ is a process dependent temperature constant and equals 1.93 in the process concerned, and T_r is a reference temperature. Consider a temperature dependent collector current that can be modeled as

$$I_C(T) = a \times T^{\theta}, \tag{1.5}$$

where a is a constant and θ is the order of temperature dependency, $\theta = 0$ implies the collector current is independent with temperature, and $\theta = 1$ implies the collect current varies linearly with temperature, and so on. The collector current density at temperature T with respect to the collector current density at the reference temperature T_r is given by

$$\frac{J_C(T)}{J_C(T_r)} = \left(\frac{T}{T_r}\right)^{\theta}. \tag{1.6}$$

We can thus simplify $V_{BE}(T)$ as

$$V_{BE}(T) = V_{G0}\left(1 - \frac{T}{T_r}\right) + V_{BE}(T_r)\frac{T}{T_r} - (\rho - \theta)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right). \tag{1.7}$$

It can be observed that $V_{BE}(T)$ is nonlinearly related to temperature. Furthermore, because of the $V_{BE}(T_r)$ term in the above equation, $V_{BE}(T)$ might vary with the biasing condition (which depends on the collector current) as well as the transistor size (which depends on the emitter area). Figure 1.2 shows the SPICE simulation of the temperature dependency of the V_{BE} of a NPN BJT with 25 μm^2 emitter area and biased with $I_C = 6$ μA. The V_{BE} is observed to be 0.73 V at $T = 300$ K, and it decreases with temperature almost linearly at a rate of -1.73 mV/K at 300 K. Such a temperature characteristic is known as *Complementary to Absolute Temperature* (CTAT), where the rate of change of V_{BE} against temperature is negative. When biased with different collector currents, the $V_{BE}(T)$ will vary as shown in the SPICE simulation result in Figure 1.2. To simplify our discussions in subsequent chapters, we shall assume that the BJTs are biased appropriately (with $I_C = 6$ μA), such that the $V_{BE}(T)$ can be approximated as a linear temperature function with high accuracy (unless otherwise

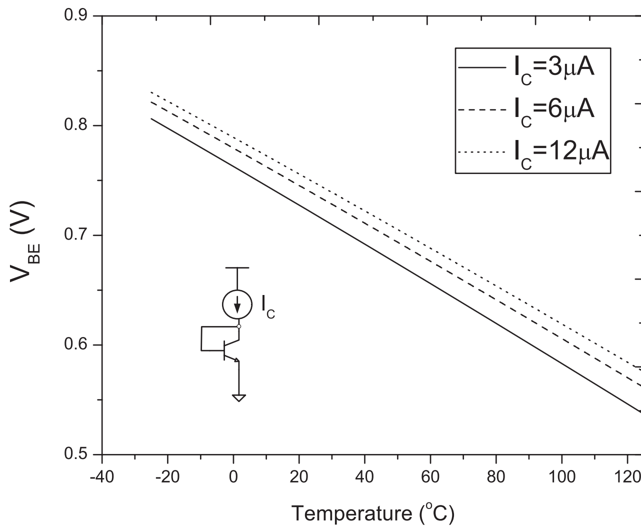

Figure 1.2 V_{BE} vs temperature of a NPN transistor with emitter area 25 μm^2 biased at $I_C = 3, 6, 12$ μA.

specified). In particular, the linear temperature dependency approximation of the V_{BE} for the NPN transistor is given by

$$\frac{\partial V_{BE}(T)}{\partial T} = -1.73 \text{ mV/K}. \tag{1.8}$$

Similarly, the $V_{EB}(T)$ of a PNP transistor has a linear temperature dependency given by

$$\frac{\partial V_{EB}(T)}{\partial T} = -1.39 \text{ mV/K}. \tag{1.9}$$

These two linearly approximated temperature characteristics of the $V_{BE}(T)$ and $V_{EB}(T)$ voltages will be applied in all our discussions unless stated otherwise. In reality, the CTAT characteristic of $V_{BE}(T)$ is not a linear temperature function as depicted in Equation 1.4, and $\partial V_{BE}(T)/\partial T$ is a high order temperature function that will cause curvature error as will be discussed in later chapters. Nevertheless, the $V_{BE}(T)$ is the PN junction voltage, which is a process independent parameter, and is one of the robust parameters in modern CMOS processes that can be used to construct a stable and precise reference voltage.

1.1.1 Differential $\mathbf{V}_{BE}$

As derived in Equation 1.4, $V_{BE}(T)$ is a high order function of temperature T. However, the difference of the $V_{BE}(T)$ between two BJTs biased with different current densities can be well represented by a low order function or even as a linear function of the temperature T. Figure 1.3 illustrates a method to extract the differential V_{BE}, $\Delta V_{BE_{1,2}}$, from two BJTs Q_1 and Q_2 with emitter areas A_{E_1} and A_{E_2}, respectively (readers should note that $V_{BE}(T)$ and V_{BE} will both be used in this book and have exactly the same meaning). Assume $A_{E_1} : A_{E_2} = 1 : N$ and the

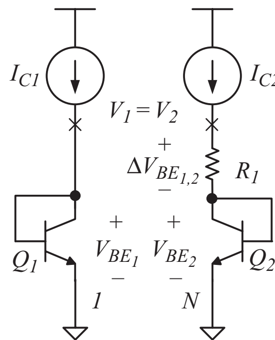

Figure 1.3 Extraction of $\Delta V_{BE_{1,2}}$ from *NPN* transistors.

current sources will provide $I_{C_1} = I_{C_2}$. As a result, the current density J_{C_1} of Q_1 is N times larger than the current density J_{C_2} of Q_2. This yields $\Delta V_{BE_{1,2}}$ as

$$\Delta V_{BE_{1,2}} = V_{BE_1} - V_{BE_2} \tag{1.10}$$

$$= V_T \ln\left(\frac{I_{C_1}}{J_S A_{E_1}}\right) - V_T \ln\left(\frac{I_{C_2}}{J_S A_{E_2}}\right) \tag{1.11}$$

$$= V_T \ln\left(\frac{A_{E_2}}{A_{E_1}}\right) \tag{1.12}$$

$$= V_T \ln(N), \tag{1.13}$$

where V_{BE_1} and V_{BE_2} are the base-emitter voltage of BJTs Q_1 and Q_2, respectively. It can be observed that $\Delta V_{BE_{1,2}}$ is proportional to V_T, which is a linear function of T. If we rewrite Equation 1.13 with respect to V_T, we shall obtain

$$V_T = \frac{\Delta V_{BE_{1,2}}}{\ln(N)}, \tag{1.14}$$

which implies the $\Delta V_{BE_{1,2}}$ extraction circuit is actually a V_T extraction circuit as well. Note that

$$\frac{\partial V_T}{\partial T} = \frac{\partial \frac{kT}{q}}{\partial T} = \frac{k}{q}$$
$$\approx 0.09 \text{ mV/K at } 300 \text{ K}. \tag{1.15}$$

It can be observed from Equation 1.15 that the thermal voltage is an intrinsic linear *Proportional to Absolute Temperature* (PTAT) voltage. Figure 1.4 shows the SPICE simulation result of the

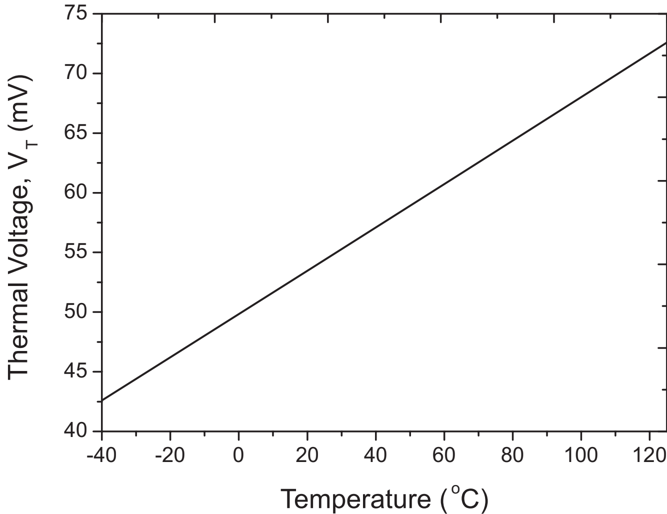

Figure 1.4 Thermal property of V_T extracted from $\Delta V_{BE_{1,2}}$ with emitter area ratio $N = 8$ using the circuit shown in Figure 1.3.

thermal property of V_T extracted from $\Delta V_{BE_{1,2}}$ using the circuit shown in Figure 1.3 with $N = 8$, which demonstrates the PTAT nature of V_T.

The PTAT voltage V_T and the CTAT voltage V_{BE} are commonly used as the thermal elements to generate a temperature insensitive reference voltage. A zero *Temperature Coefficient* (TC) reference voltage can be obtained by compensating the CTAT voltage V_{BE} with a weighted PTAT voltage V_T (The temperature coefficient will be formally defined in Section 2.1.2). The compensation obtained in the form of voltage sum can be easily implemented by the resistor network. However, the resistance of the resistor implemented in the CMOS process is process sensitive, thus imposing another adverse effect on the obtained reference voltage. The derivation of the weighting factor and the methods to compensate the adverse effects from the process variation problem will be discussed in Chapter 4.

1.2 Metal-Oxide Semiconductor Field-Effect Transistor

The metal-oxide semiconductor field-effect transistor, MOSFET, has proved extremely popular compared to the BJT. This is because of the compact layout and simple structure of the MOSFET. In this text, we shall mainly concentrate on the enhancement-mode MOSFET, including both the N-channel MOSFET (NMOS) and P-channel MOSFET (PMOS), since they are the most commonly available MOSFET devices in modern CMOS foundry services. Other types of MOS transistors will be discussed over the course of voltage reference circuit development in later chapters when such devices are applied. Showing in Figure 1.5 are the symbols of the MOSFETs that we shall use in this text. Physically, the MOSFET is a four-terminal device with a source, drain, gate, and substrate terminals. The substrate terminals of the NMOS and PMOS transistors are usually connected to GND and V_{DD}, respectively. We shall use the simplified three-terminal symbols as shown in Figure 1.5 throughout the book. The arrows beside the MOSFET symbols illustrate the direction of the current that is flowing through the drain and source terminals. The silicon layout of an NMOS transistor is shown in Figure 1.5(c). To understand the operation of the MOSFET device, let us consider the physical structure of a NMOS transistor as shown in Figure 1.6, where the NMOS transistor is fabricated directly on the P-type substrate, with N^+ regions forming the drain and source terminals, and with electrons as charge carriers. With the source terminal being grounded, and a positive voltage applied to the gate terminal, the positive voltage at the gate terminal attracts the negative electrons in the P-type substrate to accumulate under the gate terminal and repel the positive holes downwards, thus inverting the substrate surface from P-type to N-type. As a result, this layer is also known as the "*inversion*" layer, which connects the drain and source regions. This layer is also known as the N-channel in the NMOS transistor. The N-channel is completely formed when the NMOS transistor gate-to-source voltage, V_{GS}, is greater than its threshold voltage $V_{th,n}$, where the value of the threshold voltage is determined at device fabrication. Once the channel is created, there will be I_{DS} flows through the channel from the drain to the source terminals, where mobile electrons are the majority charge carriers. As a result, the NMOS transistor can be considered in three modes which depend on the channel condition, and in turn depend on the voltages across different terminals of the transistors. The details of different operation modes will be discussed in the next section. In contrast to the NMOS transistor, the PMOS transistor is fabricated on N-type substrate (in N-well CMOS process, the N-type substrate of a PMOS transistor is usually defined by the N-well), with P^+ regions forming the drain and source terminals, and uses holes as the majority charge carriers.

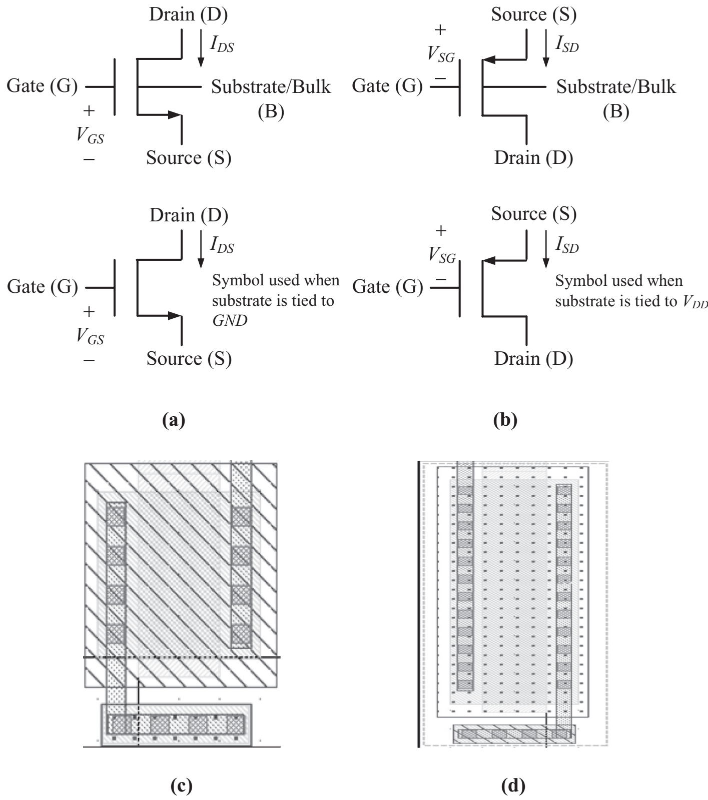

Figure 1.5 Symbols for (a) NMOS transistor and (b) PMOS transistor, and layouts of (c) NMOS transistor and (d) PMOS transistor.

An example layout of the PMOS transistor is shown in Figure 1.5(d). The PMOS transistor operates similarly as its NMOS transistor counterpart, except that V_{GS}, V_{DS}, and the threshold voltage $V_{th,p}$ are negative. Moreover, the current flowing through the channel enters from the source terminal and leaves through the drain terminal, and thus is known as I_{SD}.

As discussed, the threshold voltage V_{th}, particularly $V_{th,n}$ for the NMOS transistor and $V_{th,p}$ for the PMOS transistor, is an important parameter which defines the minimum gate voltage required to accumulate sufficient numbers of charge carriers to form the inversion channel in the MOSFET. Showing in Figure 1.7 is the relationship of I_{DS} and V_{GS} of a NMOS transistor obtained from SPICE simulation with 2 μm channel width and 1 μm channel length at $V_{DS} = 0.1$ V. It can be observed from Figure 1.7 that the positive gate voltage V_{GS} of the NMOS transistor must be larger than $V_{th,n}$ before a conducting channel is induced. In this case, the MOSFET is said to be biased at strong inversion. Similarly, a PMOS transistor requires a gate voltage that is more negative than $V_{th,p}$ to induce the conducting channel with holes as charge carriers. For the process under attention in this book

$$V_{th,n} = 0.48 \text{ V}, \tag{1.16}$$

$$V_{th,p} = -0.47 \text{ V}. \tag{1.17}$$

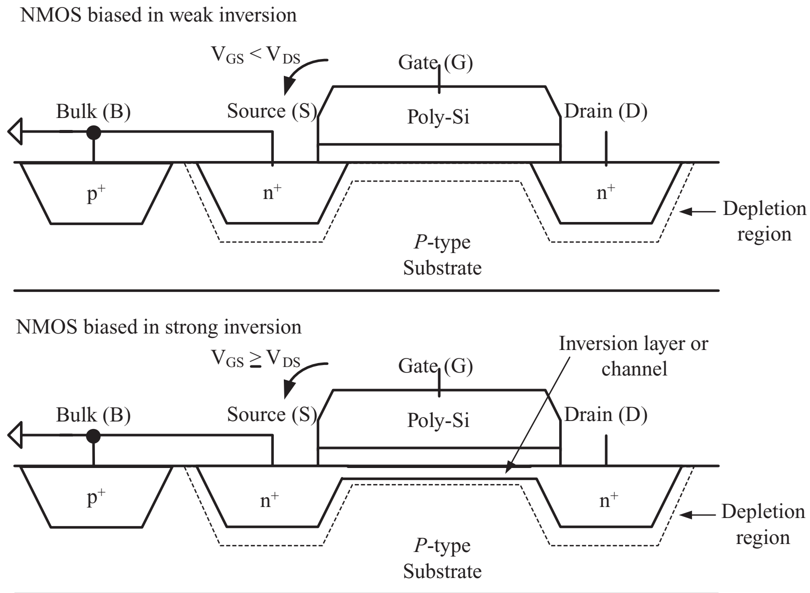

Figure 1.6 NMOS device structure biased in weak inversion and strong inversion.

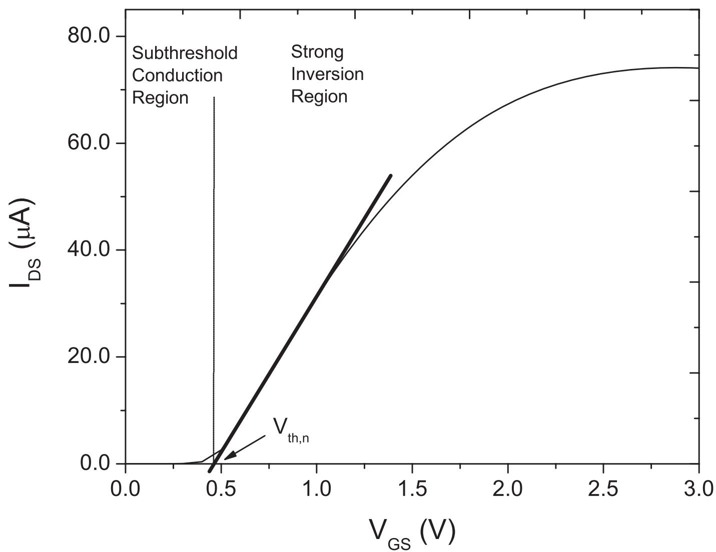

Figure 1.7 The I_{DS} versus V_{GS} of a NMOS transistor with $S = W/L = 2\ \mu m/1\ \mu m$.

Table 1.1 Summary of channel conditions and operation modes of NMOS transistor.

Voltage Condition	Channel Condition	MOS Operation Mode
$V_{GS} = 0$	No Inversion	Cutoff
$0 < V_{GS} < V_{th,n}$	Weak Inversion	Subthreshold
$0 < V_{GS} < V_{th,n}$ $V_{DS} < 4V_{th,n}$	Weak Inversion	Triode, Linear
$V_{GS} \geq V_{th,n}$ $V_{DS} < V_{GS} - V_{th,n}$	Strong Inversion	Triode, Linear
$V_{GS} \geq V_{th,n}$ $V_{DS} \geq V_{GS} - V_{th,n}$	Strong Inversion	Saturation

Note that subthreshold conduction is possible even though the current I_{DS} is very small. In this case the MOSFET is biased at weak inversion with $0 < V_{GS} < V_{th,n}$.

In addition to the inversion condition of the channel, the operation of the MOSFET is also classified into different operation regions with respect to the V_{GS} and V_{DS} voltage conditions. Table 1.1 and Table 1.2 summarize the operation modes and the corresponding channel conditions of the NMOS transistor and PMOS transistor, respectively. As discussed, the physical operation of the NMOS transistor and PMOS transistor are more or less the same with the only difference being that the voltage and current polarity are reversed. To avoid confusion, the use of notation in Table 1.1 and Table 1.2 is the same as the absolute values of the voltages under concern for the case of the PMOS device. In the following sections, we shall discuss the four operation modes of NMOS transistor in detail and in particular we shall emphasize its physical operation and thermal properties which are applicable to bandgap voltage reference circuit design. Since the PMOS transistor exhibits similar properties as that of the NMOS transistor, the physical operation details for PMOS transistor will be skipped. However, to complete our discussions, the relevant analytical relationship of the PMOS transistor will also be presented. In particular, the subscript "*sub*", "*lin*", and "*sat*" will be appended to V_{GS} and

Table 1.2 Summary of channel conditions and operation modes of PMOS transistor.

Voltage Condition	Channel Condition	MOS Operation Mode
$V_{GS} = 0$	No Inversion	Cutoff
$\lvert V_{GS}\rvert < \lvert V_{th,p}\rvert$	Weak Inversion	Subthreshold
$\lvert V_{GS}\rvert < \lvert V_{th,p}\rvert$ $\lvert V_{DS}\rvert < \lvert 4V_{th,p}\rvert$	Weak Inversion	Triode, Linear
$\lvert V_{GS}\rvert \geq \lvert V_{th,p}\rvert$ $\lvert V_{DS}\rvert < \lvert V_{GS} - V_{th,p}\rvert$	Strong Inversion	Triode, Linear
$\lvert V_{GS}\rvert \geq \lvert V_{th,p}\rvert$ $\lvert V_{DS}\rvert \geq \lvert V_{GS} - V_{th,p}\rvert$	Strong Inversion	Saturation