Frequency Acquisition Techniques for Phase Locked Loops

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This book is dedicated to our loved ones who have found their final homes.

Toolkit

Several useful tools, free simulation software, and illustrations accompany this book as a special bonus on the web at: http://booksupport.wiley.com. The reader can thus follow along and run the same simulations described in this book, as well as claim several free tools he/she will find useful throughout an engineering career.

Preface

Many excellent treatises covering phase-locked loops (PLLs) have been published, but to the author's surprise, few books exist covering the frequency acquisition assistance techniques necessary and/or available. A PLL by itself cannot become useful until it has acquired the applied signal's frequency. This acquisition process has been treated with extreme mathematical and/or graphical rigor in the past, mainly by Viterbi and Jet Propulsion Lab (JPL =) in publications featuring phase-plane trajectories. However, most of the PLL circuits in other analyses had no explicit assistive circuitry included. Often, a PLL will never reach frequency acquisition (called “capture” in most texts) by itself without explicit assistive circuits (with exception of the overused phase/frequency detector-based approach that has performance drawbacks during settled closed-loop operation that will be identified and explained later in detail).

This book attempts to bridge this information gap. Since mathematical rigor for its own sake can degenerate to intellectual “rigor mortis,” the author hopes to offer a treatment of the subject that can be comprehended by both engineer and technician (except for an occasional formula that might be included for essential reasons and even then the book is organized so that the nonmathematician can skip it and move on to the essence of the thought being discussed). A more important reason exists for avoiding excessive mathematical verbosity: often the objective gets forgotten and lost in the minutia; assumptions are too confining or too optimistic or too pessimistic, and the motive behind the complexity is not well stated. For this reason, we have decided to focus on the practical and to simulate actual situations wherever possible, both for clarity, so that

the reader can take an active role in altering the assumptions and qualifications of a certain architecture and then rerun the simulation to see what his or her results might be. It is disappointing to be shown a solution that does not fit the problem.

Most of the approaches in this book have been developed through years of experience rather than from articles and books, but where references exist they will be cited. The author believes that it is good to communicate in something besides “mathspeak” (e.g., the English language is quite powerful) and to go directly to the fundamentals. Einstein once stated, “Everything should be made as simple as possible, but not simpler.” So get out your 64-bit Divining Rod and 32-bit abacus. The author's intention is to communicate with you, the reader, not snow you, “educate” you, and “intellectually subordinate” you. One can get subordination for free; one need not pay good money for it by buying a math-heavy book in which the author's main accomplishment is to write as esoterically as he possibly can and leave the reader with a feeling of general intellectual inferiority, even if unintentional. It is a hope that clarity trumps verbosity and it remains for you, the reader, to determine whether we succeed.

Chapter 1

Introduction

We must begin any treatment of PLL frequency acquisition with a review of the fundamentals of the PLL. Thereafter, the following subjects can be discussed (not necessarily in that order):

a. The difference between the type I second-order and the type II second-order PLL and why the type II second-order PLL is usually preferred

b. The mechanism for acquisition in an ordinary unassisted PLL

c. The multiplying phase detector (numerical multiplier, analog multiplier, RF mixer, or XOR gate used as a multiplier) and effects of hard limiting

d. The edge-triggered digital phase/frequency detector

e. The ramp-and-sample phase detector and a technique to exploit its uniqueness to realize wideband capture acquisition assistance

f. The quadricorrelator, balanced and unbalanced

g. The Costas PLL, “Frequency Squaring” Carrier Recovery, etc.

h. The clock and data recovery PLL

i. PLL considerations for frequency synthesizers

j. Signal-to-noise ratio (SNR) of the various phase detectors

k. Short- and long-term phase and frequency settling effects in a PLL

l. The effect of a phase detector dead zone on phase noise and wander

m. The reduction or elimination of phase detector dead zone and impact on reference frequency suppression

n. Sweeping techniques

o. Sweep disabling after lock and a self-disabling method

p. False locking on data or modulation sidebands

q. Preventing false lock on spurious signals, such as modulation sidebands

r. Comments on converting an analog to an all-digital architecture

s. Limiting acceleration in swept acquisition methods

t. Cycle slipping due to excessive acceleration or modulation within the loop

u. Killing the quadricorrelator output during final lock to suppress its otherwise added phase noise; using a dead zone versus a switch

v. DC offsets and noise and the effect on PLL acquisition

w. Heroic spur suppression using DC offset minimization and brickwall filtering

x. Brute force methods such as wideband/narrowband PLL bandwidth modes

y. The frequency ratio detector using counter techniques

z. Advantages and disadvantages of different assistive techniques and when to use which technique

Chapter 2

A Review of PLL Fundamentals

2.1 What is a PLL?

A PLL (phase-locked loop) is a circuit that varies a VCO (voltage-controlled oscillator) frequency (hence its phase) relative to that of an input until it matches that of the input signal [1,2]. If the VCO is replaced with a voltage-controlled phase modulator or a voltage-controlled delay element, it is then called a DLL (delay-locked loop) and cannot operate offset in its resting frequency.

The advantage of the VCO is that by changing its frequency relative to that of the other signal, billions of degrees of phase shift over time can be obtained. A DLL cannot do this, and therefore, looks like a completely different animal. By definition, it has no need of frequency acquisition. Its output frequency always matches its input frequency even before the loop is closed or settled. But its phase excursion is extremely limited, often to magnitudes of 360° or under. A VCO is an integrator for phase, whereas the voltage-controlled delay element is zero-order. By that we mean the following. If we apply a step function (a sudden change in DC from voltage A to voltage B) to the VCO input, the VCO output's phase begins to ramp in the direction of the voltage step (which is the frequency step) and phase accumulates. The voltage-controlled delay element's output phase merely “pops” from value A to value B. Hence, a VCO output phase is automatically smoothed compared to that of the voltage-variable delayer.

We will not discuss the DLL any further, since this book is about frequency acquisition methods for phase-locked loops.

To realize a PLL, the following building blocks ("block diagram" elements) are required:

1. a phase comparator or detector whose DC output voltage depends on the phase difference between its two inputs

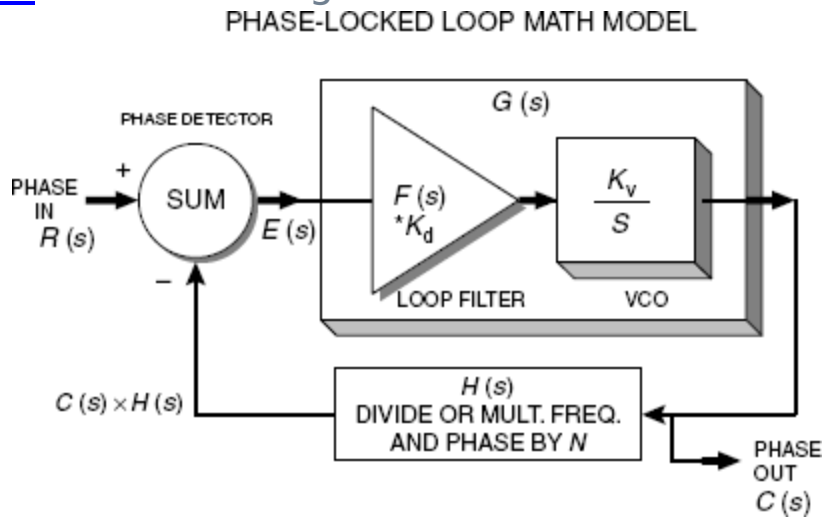
2. a filter and amplifier to interface the DC voltage from the phase detector with the VCO control-voltage input

3. a VCO, whose output frequency is directly proportional (or mainly so) to the applied DC control voltage at its input.

The block diagram is shown in Figure 2.1. The phase detector output voltage is called the error signal "$E(s)$". The control voltage at the VCO input is called "V_C" and the output phase of the VCO (which is mathematically the integral of its frequency) is called " $\emptyset_{out}$ "(or "$C(s)$" in the figure). The input signal phase is called "$\emptyset_{in}$"(or "$R(s)$" in the figure, which is the notation used by classical control systems [3]). The element between the phase detector output and the VCO input is a lowpass filter, usually first order, and amplifier. That element has a gain-versus-frequency property called its "transfer function," mathematically represented as "$F(s)$".(The letter "s" represents complex frequency, not to be confused with the Laplace operator for differentiation.) The transfer function $F(s)$ is NOT generally equal to the closed-loop PLL transfer function, as we shall show. Rather, it is a completely general mathematical expression representing the gain versus frequency properties of whatever we wish the element to be. If we pick an element having too high an order (too many rolloffs), it will be unusable within the PLL and will cause oscillation when the feedback loop is closed. Notice

for now that the phase detector is represented as a differencer. This is a highly simplified representation, but one has to begin somewhere. So far, the loop we are describing is called a “linearized” model; that is because the dynamic range (clipping level) of the ideal phase detector is limitless with no overflow or wraparound. Such a PLL would always acquire the applied frequency without any assistance, whatsoever; if we could obtain such a phase detector, you would not need to read this book and this author would not need to write it. But let us press on.

Figure 2.1 PLL block diagram.



Practical phase detectors (those that can be built) often have wraparound, also called “periodicity.” In a nutshell, a periodic phase detector (describing nearly all of them) is one that cannot distinguish between 360 and 720°, for instance. In fact, a human being observing two waveforms on an oscilloscope cannot do any better if he is suddenly presented with the two waveforms without the opportunity of knowing their complete previous history (tracking the phase between them for all negative time). But there is a difference between 360 and 720°. An ideal phase detector would output twice the voltage for 720° as it does for 360. A periodic phase detector, however, outputs the same voltage for 360 and 720°(or perhaps some submultiple or multiple

of 360) and repeats its voltage versus phase angle curve. This periodicity may be sine shaped, triangular, sawtooth, and so on. The sine or cosine shape, for example, is a shape that mathematically repeats every multiple of + or -90°. The behavior is comparable to the “rollover” of a car's mechanical odometer when it reaches 100,000 miles. An ideal odometer would not repeat, but would keep incrementing. The shape of the odometer rollover is sawtooth. Mileage accumulates until the maximum (clipping or overflow) amplitude (in this case 100,000 miles), then resets to zero and begins again. Instead of resetting to zero miles after 100,000, if it started to decrement back toward zero, then reach zero before incrementing again, its periodic behavior would be called triangular. An odometer with a 10,000 mile maximum before rollover would be annoying, and one with a 10 mile rollover (overflow) would be exasperating. However, all three would each qualify as an odometer. But one would deal with each very differently. Most practical phase detectors have a very small rollover window analogous to a <<1 mile odometer rollover.

The block marked SUM is the phase detector (in the classical control systems approach, it is actually a differencer). Its conversion gain is K_d that is the voltage produced at its output divided by the phase difference between its two inputs in radians; hence, its units are volts per radian. In analog phase detectors, this conversion gain is highly influenced by signal levels at its two inputs.

Although the detector is typically implemented as a multiplier of waveforms, its function is to create an output proportional to phase difference, so it is properly represented here. Note that this entire block diagram is applicable only to the linear region of the PLL (noncycle-slipping operation[1]), not to the capture behavior prior to lock.

The VCO is shown as having a gain K_V expressed in radians per second per volt. It has an "s" term in its denominator, because it outputs frequency, which is the derivative of phase. Therefore, phase is the integral of frequency, and $1/s$ is the operator for integration. The VCO is driven by a filter having a transfer function $F(s)$. For a "type 2" second-order PLL this filter has a gain of infinity at 0 Hz (requiring an op-amp).

The full set of equations needed to express the linear model of the PLL is given as follows:

(2.1) $$\frac{\theta_{\text{out}}}{\theta_{\text{in}}}(s) = \frac{C(s)}{R(s)} = \frac{G(s)}{1 + G(s)H(s)}$$

(2.2) $$H(s) = \frac{1}{N} \text{ for a frequency divider}$$

(2.3) $$H(s) = N \text{ for a frequency multiplier}$$

(2.4) $$G(s) = \frac{K_{\text{d}} K_{\text{v}} F(s)}{s}$$

When the transfer function block labeled $F(s)$ is expressed by a zero-order (scalar) expression it results in a first-order PLL overall transfer function, due to the presence of the VCO acting as a single pole at zero frequency.

Thus, if $F(s) = A$, then

(2.5) $$\frac{\theta_{\text{out}}}{\theta_{in}}(s) = \frac{AK_{\text{d}}K_{\text{v}}}{s + HAK_{\text{d}}K_{\text{v}}}$$

If we then substitute $s = j\omega$ we get a lowpass function whose gain at 0 Hz is $1/H$ and whose −3 dB bandwidth is

(2.6) $$\omega_{-3\,\text{dB}} = HAK_{\text{d}}K_{\text{v}}$$

The units for Equation 2.6 are sec^{-1}, interpreted as radians per second. Note several features of this expression. First, the 3 dB bandwidth increases in direct proportion to any of the constants to the right of the equal sign, or in direct proportion to their collective product. Second, the units of K_{d} are volts per radian, the units for K_{v} are radians per second per volt, and the remaining constants have no

units. Thus, the product of the terms is indeed inverse seconds.

We see the expression for frequency response of the phase transfer function immediately by inspection, by writing

(2.7) $$\frac{\Delta\theta_{\text{out}}}{\Delta\theta_{\text{in}}} = \frac{\theta_{\text{out}}}{\theta_{\text{in}}}$$

What is the frequency response of the frequency modulation (FM) transfer function? It is simply given by

(2.8) $$\frac{(\Delta\theta_{\text{out}}/\Delta t)}{(\Delta\theta_{in}/\Delta t)} = \frac{\Delta\theta_{\text{out}}}{\Delta\theta_{\text{in}}}$$

Thus, we see that the FM frequency response is the same as the phase modulation (PM) frequency response. This is true in general for any PLL.

2.2 Second-Order PLL

A limitation of the first-order PLL is the fact that it has a range of phase angles beyond which it loses lock and also fails to capture. This happens when the phase rollover point of the phase detector is encountered, combined with the finite gains of *A* and *K* coefficients. On the other hand, a second-order PLL can track over an infinite frequency range, assuming it is type 2. We shall next examine what type one and type two means for a second-order PLL.

2.3 Second-Order PLL Type One

A type one (written type I for Roman numeral one) PLL has a lead-lag filter $F(s)$ of the following form:

(2.9) $$F(s) = \frac{sZ + 1}{sP + 1}$$

where Z = lead time constant and P = lag time constant.

Substituting terms, we get the following open-loop PLL transfer function:

(2.10) $$G(s) = G_0 \frac{K_\mathrm{d} K_\mathrm{v} (sZ + 1)}{s(sP + 1)}$$

Note the presence of a single free "*s*" term in the denominator. This property makes the PLL a "type I" and the resulting closed-loop transfer function (Eqn. 2.1) is second order.

The type-I PLL closed loop behavior exhibits finite phase error at zero frequency for θ_in.

2.4 Second-Order PLL Type Two

The type-II PLL exploits the characteristics of an operational amplifier to provide infinite gain at zero frequency for the loop filter. The loop filter is thus of the following form:

(2.11) $$F(s) = \frac{sZ + 1}{sP}$$

where again *Z* = lead time constant and *P* = lag time constant. But notice this time that the open-loop PLL transfer function is given as:

(2.12) $$G(s) = \frac{K_\mathrm{d} K_\mathrm{v} (1 + sZ)}{s^2 P}$$

where we now see a denominator containing the product of two free integrations (free "*s*" terms). When the loop is closed, the result is a PLL whose static phase error at zero frequency is $\{\theta_\mathrm{in} - (\theta_\mathrm{out}/H) = 0\}$ at $s = 0$ (i.e., at $\mathrm{at}\ \omega = 0$). We have omitted the negative sign multiplying the loop filter equation using the op-amp in inverting mode (required for operation). This negative sign is important when the periodic phase detector has only one slope (sawtooth periodicity), but unimportant for a phase detector having triangular or sinusoidal periodicity. It can be shown that regardless of the sign of the open-loop transfer function, employment of either of the two latter kind of phase

detectors will result in a PLL which will slip cycles until it discovers the stable slope providing negative feedback around the loop. The process will be explained a bit later.

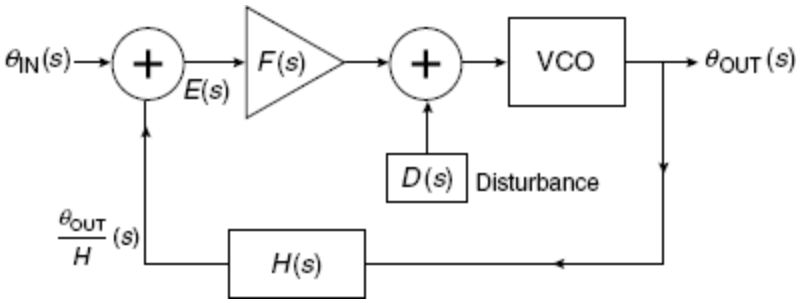
2.5 Higher-Order PLL's

The need occasionally arises for a PLL of higher than second order, such as when acceleration of the input phase must be tracked (requiring a third-order PLL). Most higher-order loops are not the classical beneficiaries of higher-order terms, that is, the higher order is simply the result of unwanted parasitic poles or sideband suppression filtering (to be briefly discussed a bit later). Such higher order terms are usually arranged to have poles well above the natural loop frequency of ω_n(in the case of a second-order PLL).

2.6 Disturbances

In all cases of order ≥2 and type-II PLL or higher, a low-frequency (within the loop's bandwidth) disturbance signal $D(s)$ summed into the VCO input tends to become cancelled by the loop (refer to Fig. 2.2). Proof is left to the reader. This is profound, because it states that a direct current (DC) offset at the VCO input will be perfectly cancelled. Such an offset can represent a voltage offset at the VCO control input, or equivalently a steady-state frequency error. Since we have assumed a linear PLL model, this cancellation is perfect so that any equivalent VCO frequency error, no matter how large, will be cancelled. In other words, since the filter function has infinite gain at DC, the error signal $E(s)$ needs to be merely infinitesimal in order to steer the VCO onto the correct frequency. The two phases at the phase detector input will be such as to produce zero error signal.

Figure 2.2 PLL with disturbance at VCO input.



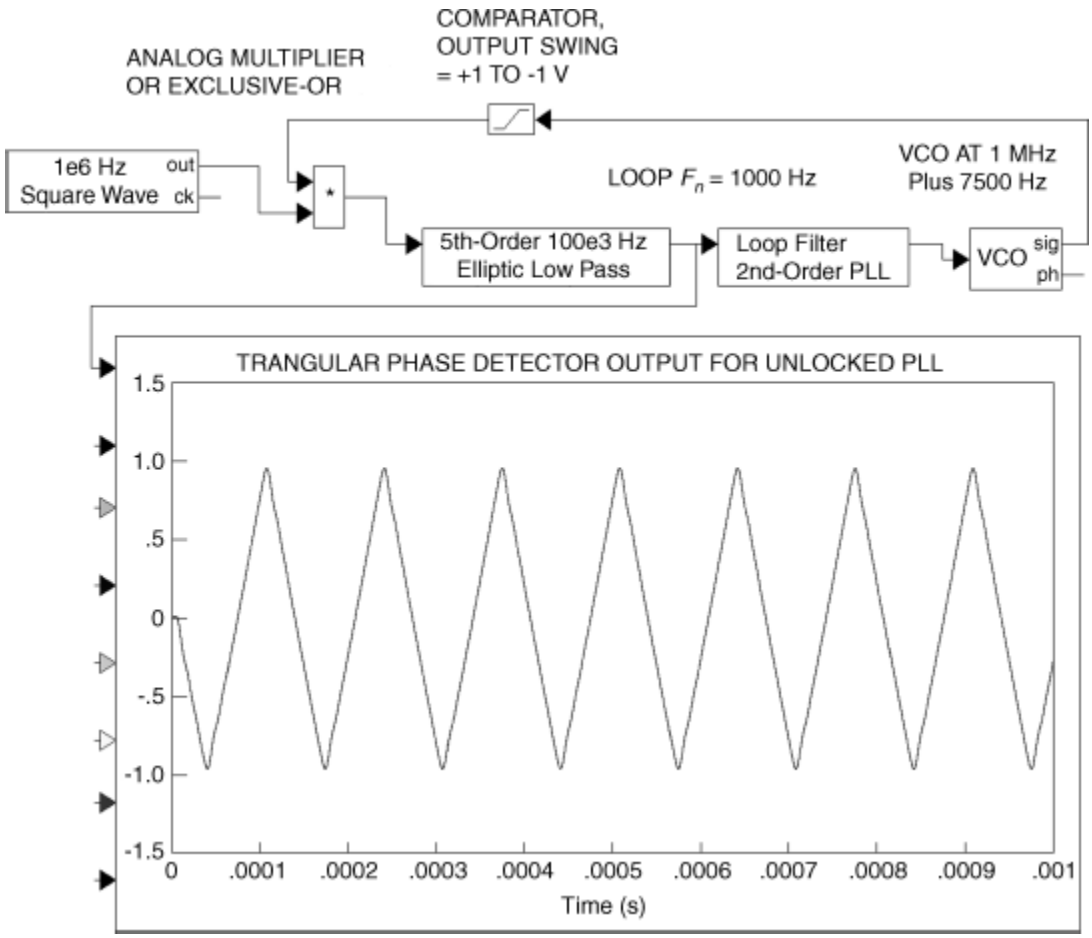
As the disturbance frequency increases, the cancellation deteriorates. Notice that the disturbance is a VCO-frequency disturbance, not a phase disturbance. We will need to model a phase (noise) disturbance using a summer at the VCO output rather than its input. But VCO phase noise is flat in the FM sense, -6 dB/octave in the phase sense, as we shall see from the later discussion of Leeson's model. Thus, VCO phase noise can indeed be modeled using resistor noise (and 1/*f* shaping if required) appropriately summed into the VCO input.

2.7 Frequency Steering and Capture

Thus, we see that the VCO can be steered to the correct frequency from any displacement. Thus, the capture range for our ideal PLL is nearly infinite. This is also true of the PLL model using waveform multiplication for the phase detection, although many cycle slips may be encountered. The way in which an analog multiplier or RF mixer or exclusive-OR gate generates an error signal $E(s)$ is by multiplying the two input waveforms to obtain the trigonometric identity of the product of the two waveforms, which is sinusoidally or triangularly related to the phase difference between them. Harmonics (produced as by-products) are discarded via high-frequency lowpass filtering, usually passive. The two waveforms can be in the RF range whereas the error signal produced is ordinarily in the low-frequency (audio to video) range.

In the case of an exclusive-OR phase detector (which can be modeled simply as an analog multiplier with a comparator or hard limiter at each input), which produces a triangular rollover curve, a frequency error results in an initial cycle slipping beat frequency shown in the example of Figure 2.3.

Figure 2.3 Unlocked PLL (VCO offset frequency too large) having an exclusive-OR or square-wave input multiplying phase detector.



The same PLL will eventually lock, by producing a weak but essential DC error brought about by second-order distortion [1] of the cycle-slipping beat waveform (see Fig. 2.4). Notice two slopes exist but the PLL will push away if it attempts to reach equilibrium on the wrong slope. Thus, we need not worry about the polarities of the VCO control signal or the phase detector itself.

Figure 2.4 Locking process for a PLL having an exclusive-OR or a square-wave input multiplying phase detector.