

# Dependability in Electronic Systems

Nobuyasu Kanekawa · Eishi H. Ibe · Takashi Suga ·  
Yutaka Uematsu

# Dependability in Electronic Systems

Mitigation of Hardware Failures, Soft Errors,  
and Electro-Magnetic Disturbances

 Springer

Nobuyasu Kanekawa  
Hitachi Research Laboratory, Hitachi, Ltd.  
Hitachi-shi 319-1292, Ibaraki, Japan  
nobuyasu.kanekawa.ef@hitachi.com

Eishi H. Ibe  
Production Engineering Research  
Laboratory, Hitachi, Ltd.  
Yokohama-shi 244-0817,  
Kanagawa, Japan  
hidefumi.ibe.hf@hitachi.com

Takashi Suga  
Production Engineering Research  
Laboratory, Hitachi, Ltd.  
Yokohama-shi 244-0817,  
Kanagawa, Japan  
takashi.suga.pt@hitachi.com

Yutaka Uematsu  
Production Engineering Research  
Laboratory, Hitachi, Ltd.  
Yokohama-shi 244-0817,  
Kanagawa, Japan  
yutaka.uematsu.ws@hitachi.com

ISBN 978-1-4419-6714-5  
DOI 10.1007/978-1-4419-6715-2  
Springer New York Dordrecht Heidelberg London

e-ISBN 978-1-4419-6715-2

Library of Congress Control Number: 2010937189

© Springer Science+Business Media, LLC 2011

All rights reserved. This work may not be translated or copied in whole or in part without the written permission of the publisher (Springer Science+Business Media, LLC, 233 Spring Street, New York, NY 10013, USA), except for brief excerpts in connection with reviews or scholarly analysis. Use in connection with any form of information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed is forbidden.

The use in this publication of trade names, trademarks, service marks, and similar terms, even if they are not identified as such, is not to be taken as an expression of opinion as to whether or not they are subject to proprietary rights.

Printed on acid-free paper

Springer is part of Springer Science+Business Media ([www.springer.com](http://www.springer.com))

# Preface

The word “dependability” that appears in the title is not used so often to be familiar with. The word has wider meaning and not only means “reliability” but also includes robustness, safety, security, resilience, and so on. Fault-tolerance technology that equips the redundant subsystems or components in preparation for failure in order to improve “reliability” has been used for many decades. In the meantime, J.C. Laprie expanded the term dependability as a wider concept in 1985 [1] because the meaning of “reliability” that the fault-tolerance technology treated had broadened. After then, dependability and dependable have been used in various fields to this day. Based on such situation and as I also belonged to the committees concerning “dependability,” I dare to use “dependability” in this text, thinking it is one of my vocations to spread the term.

As for terms related to reliability, the two terms have been used exclusively in Japanese. The Japanese word *shinrai-do* means quantitative index of reliability and the word *shinrai-sei* means qualitative character of reliability. In my personal opinion, the *shinrai-sei* may fall on the dependability.

As written in the title of this book, mitigation of hardware failures, soft errors, and electro-magnetic disturbances is indispensable in order to realize dependability of electronic systems. This book introduces authors’ original mitigation technologies of soft errors, electro-magnetic interference, and power supply noise, in addition to general mitigation technologies.

The authors have brought up the mitigation technology to realize dependability through a lot of industrial fields such as railroad, atomic energy, and IT networks. The dependable technology starts unifying with the latest LSI technology and being succeeded by the safety processor technology by on-chip redundancy. As a result, great reduction in costs will become possible by the effect of mass production of LSI technology in the future. I am convinced that we can contribute to safety and convenience of our ordinary life using dependable technology in more familiar field such as automotives.

Lake Hatori, Japan

Nobuyasu Kanekawa  
3rd May, 2010

## Reference

1. J.C. Laprie, “Dependable Computing and Fault Tolerance: Concepts and Terminology,” *Proceedings of the 15th IEEE International Symposium on Fault-Tolerant Computing, Austin, TX, USA*, pp. 2–11 (1985).

# Acknowledgements

For [Chapter 2](#), the authors would like to gratefully acknowledge Professors Emeritus T. Nakamura, M. Baba, Professor Y. Sakemi of Tohoku University for their helpful discussions and support for the database on nuclear reactions and high energy neutron irradiation tests. The authors also gratefully acknowledge Professor J. Blomgren and Dr. A. Prokofiev for their support of neutron irradiation experiments in TSL.

Dr. M. Nicolaidis of TIMA Laboratory, Dr. C. Slayman of Ops A La Carte and Dr. D. Alexandrescu of iRoC Inc. have made invaluable discussions toward new standards on neutron testing methods.

For [Chapter 5](#), the authors would like to gratefully acknowledge Prof. Emeritus T. Takano,<sup>1</sup> Prof. T. Yamada, and Mr. K. Shutoh of ISAS (Space and Astronautical Science of Japan)<sup>2</sup> for giving us opportunity to pursue research on fault-tolerance through Hiten Onboard Computer development and its experiments.

The authors wish to express their gratitude to the members of Hiraiso Solar Terrestrial Research Center, Communication Research Laboratory of Japan for furnishing their solar flare data, and the members of the Orbit Planning Group, ISAS for furnishing their orbit data of Hiten.

The authors are grateful to Professors Emeritus Y. Tohma and T. Nanya of Tokyo Institute of Technology, Professors A. Avizienis<sup>3</sup> and D. Rennels of University of California, Los Angeles, Mr. H. Nakanishi,<sup>4</sup> ex-Deputy General Manager, Ohmika-Works, Hitachi, Ltd., and Dr. H. Ihara, ex-Chief Engineer of the Space System Division, Hitachi, Ltd., for their help and advices in pursuing research on fault tolerance.

The authors thank Mr. C. Glaser and the members of Springer for their efforts in publishing this book, and the members of Hitachi, Ltd., for their advices and efforts in implementing dependable systems stated in this book.

---

<sup>1</sup>Currently in Nihon University.

<sup>2</sup>Currently Institute of Space and Astronautical Science, Japan Aerospace Exploration Agency (JAXA).

<sup>3</sup>Currently in Vytautas Magnus University, Lithuania.

<sup>4</sup>Currently, President of Hitachi, Ltd.

After the correction of the text, the authors were informed news with the deepest sadness. We would like to pay a tribute to the memory and contribution of the late Dr. J. C. Laprie, who advocated the term “dependability” ([1] in Preface).

# Contents

<b>1</b>	<b>Introduction</b>	1
1.1	Trends in Failure Cause and Countermeasure	1
1.2	Contents and Organization of This Book	3
1.3	For the Best Result	5
	References	5
<b>2</b>	<b>Terrestrial Neutron-Induced Failures in Semiconductor Devices and Relevant Systems and Their Mitigation Techniques</b>	7
2.1	Introduction	7
2.1.1	SER in Memory Devices	7
2.1.2	MCU in Memory Devices	8
2.1.3	SET and MNU in Logic Devices	8
2.1.4	Chip/System-Level SER Problem: SER Estimation and Mitigation	9
2.1.5	Scope of This Chapter	9
2.2	Basic Knowledge on Terrestrial Neutron-Induced Soft-Error in MOSFET Devices	10
2.2.1	Cosmic Rays from the Outer Space	10
2.2.2	Nuclear Spallation Reaction and Charge Collection in CMOSFET Device	11
2.3	Experimental Techniques to Quantify Soft-Error Rate (SER) and Their Standardization	12
2.3.1	The System to Quantify SER – SECIS	12
2.3.2	Basic Method in JESD89A	13
2.3.3	SEE Classification Techniques in Time Domain	15
2.3.4	MCU Classification Techniques in Topological Space Domain	16
2.4	Evolution of Multi-node Upset Problem	17
2.4.1	MCU Characterization by Accelerator-Based Experiments	17
2.4.2	Multi-coupled Bipolar Interaction (MCBI)	21
2.5	Simulation Techniques for Neutron-Induced Soft Error	23
2.5.1	Overall Microscopic Soft-Error Model	23



2.5.2	Nuclear Spallation Reaction Models . . . . .	24
2.5.3	Charge Deposition Model . . . . .	24
2.5.4	SRAM Device Model . . . . .	26
2.5.5	Cell Matrix Model . . . . .	27
2.5.6	Recycle Simulation Method . . . . .	28
2.5.7	Validation of SRAM Model . . . . .	29
2.6	Prediction for Scaling Effects Down to 22 nm	
	Design Rule in SRAMs . . . . .	29
2.6.1	Roadmap Assumption . . . . .	29
2.6.2	Results and Discussions . . . . .	30
2.6.3	Validity of Simulated Results . . . . .	39
2.7	SER Estimation in Devices/Components/System . . . . .	40
2.7.1	Standards for SER Measurement for Memories . . . . .	40
2.7.2	Revisions Needed for the Standards . . . . .	40
2.7.3	Quantification of SER in Logic Devices and Related Issues . . . . .	42
2.8	An Example of Chip/Board-Level SER Measurement and Architectural Mitigation Techniques . . . . .	43
2.8.1	SER Test Procedures for Network Components . . . . .	43
2.8.2	Results and Discussions . . . . .	49
2.9	Hierarchical Mitigation Strategies . . . . .	51
2.9.1	Basic Three Approaches . . . . .	51
2.9.2	Design on the Upper Bound (DOUB) . . . . .	52
2.10	Inter Layer Built-In Reliability (LABIR) . . . . .	56
2.11	Summary . . . . .	57
	References . . . . .	59
<b>3</b>	<b>Electromagnetic Compatibility . . . . .</b>	<b>65</b>
3.1	Introduction . . . . .	65
3.2	Quantitative Estimation of the EMI Radiation Based on the Measured Near-Field Magnetic Distribution . . . . .	68
3.2.1	Measurement of the Magnetic Field Distribution Near the Circuit Board . . . . .	68
3.2.2	Calculation of the Electric Current Distribution on the Circuit Board . . . . .	68
3.2.3	Calculation of the Far-Field Radiated EMI . . . . .	70
3.3	Development of a Non-contact Current Distribution Measurement Technique for LSI Packaging on PCBs . . . . .	71
3.3.1	Electric Current Distribution Detection . . . . .	71
3.3.2	The Current Detection Result and Its Verification . . . . .	74
3.4	Reduction Technique of Radiated Emission from Chassis with PCB . . . . .	75
3.4.1	Far-Field Measurement of Chassis with PCB . . . . .	75
3.4.2	Measurements of Junction Current . . . . .	79

3.4.3	PSPICE Modeling . . . . .	80
3.4.4	Experimental Validation . . . . .	85
3.5	Chapter Summary . . . . .	86
	References . . . . .	88
<b>4</b>	<b>Power Integrity . . . . .</b>	<b>91</b>
4.1	Introduction . . . . .	91
4.2	Detrimental Effect and Technical Trends of Power Integrity Design of Electronic Systems and Devices . . . . .	92
4.2.1	Detrimental Effect by Power Supply Noise on Semiconducting Devices . . . . .	92
4.2.2	Trends of Power Supply Voltage and Power Supply Current for CMOS Semiconducting Devices . . . . .	98
4.2.3	Trend of Power Distribution Network Design for Electronic Systems . . . . .	100
4.3	Design Methodology of Power Integrity . . . . .	102
4.3.1	Definition of Power Supply Noise in Electric System . . . . .	102
4.3.2	Time-Domain and Frequency-Domain Design Methodology . . . . .	104
4.4	Modeling and Design Methodologies of PDS . . . . .	115
4.4.1	Modeling of Electrical Circuit Parameters . . . . .	116
4.4.2	Design Strategies of PDS . . . . .	121
4.5	Simultaneous Switching Noise (SSN) . . . . .	125
4.5.1	Principle of SSN . . . . .	126
4.5.2	S–G loop SSN . . . . .	127
4.5.3	P–G loop SSN . . . . .	129
4.6	Measurement of Power Distribution System Performance . . . . .	131
4.6.1	On-Chip Voltage Waveform Measurement . . . . .	131
4.6.2	On-Chip Power Supply Impedance Measurement . . . . .	137
4.7	Summary . . . . .	140
	References . . . . .	141
<b>5</b>	<b>Fault-Tolerant System Technology . . . . .</b>	<b>143</b>
5.1	Introduction . . . . .	143
5.2	Metrics for Dependability . . . . .	144
5.2.1	Reliability . . . . .	144
5.2.2	Availability . . . . .	145
5.2.3	Safety . . . . .	147
5.3	Reliability Paradox . . . . .	148
5.4	Survey on Fault-Tolerant Systems . . . . .	150
5.5	Technical Issues . . . . .	153
5.5.1	High Performance . . . . .	154
5.5.2	Transparency . . . . .	156
5.5.3	Physical Transparency . . . . .	156
5.5.4	Fault Tolerance of Fault Tolerance for Ultimate Safety . . . . .	157
5.5.5	Reliability of Software . . . . .	160

- 5.6 Industrial Approach . . . . . 161
  - 5.6.1 Autonomous Decentralized Systems . . . . . 163
  - 5.6.2 Space Application . . . . . 164
  - 5.6.3 Commercial Fault-Tolerant Systems . . . . . 164
  - 5.6.4 Ultra-Safe System . . . . . 165
- 5.7 Availability Improvement vs. Coverage Improvement . . . . . 166
- 5.8 Trade-Off Between Availability and Coverage – Stepwise Negotiating Voting . . . . . 166
  - 5.8.1 Basic Concept . . . . . 166
  - 5.8.2 Hiten Onboard Computer . . . . . 169
  - 5.8.3 Fault-Tolerance Experiments . . . . . 170
  - 5.8.4 Extension of SNV – Redundancy Management . . . . . 173
- 5.9 Coverage Improvement . . . . . 175
  - 5.9.1 Self-Checking Comparator . . . . . 176
  - 5.9.2 Optimal Time Diversity . . . . . 179
- 5.10 On-Chip Redundancy . . . . . 184
- 5.11 High Performance (Commercial Fault-Tolerant Computer) . . . . . 188
  - 5.11.1 Basic Concepts of TPR Architecture . . . . . 188
  - 5.11.2 System Configuration . . . . . 189
  - 5.11.3 System Reconfiguration on Fault Occurrence . . . . . 191
  - 5.11.4 Processing Take-Over on Fault Occurrence . . . . . 191
  - 5.11.5 Fault Tolerance of Fault Tolerance . . . . . 192
  - 5.11.6 Commercial Product Model . . . . . 195
- 5.12 Current Application Field: X-by-Wire . . . . . 196
- References . . . . . 198
- 6 Challenges in the Future . . . . . 201**
  - References . . . . . 202
- Index . . . . . 203**

# List of Figures

1.1	Trends in failure cause . . . . .	1
1.2	Trends of LSI technology . . . . .	2
1.3	Chronology on dependability . . . . .	4
2.1	Macroscopic neutron-induced soft-error mechanism . . . . .	10
2.2	Neutron differential flux spectrum at the sea level in NYC (JESD89A) [6] . . . . .	11
2.3	Microscopic mechanism of neutron-induced soft-error in a SRAM bit. Secondary ions are produced by nuclear spallation reaction and soft-error takes place when enough amount of charge is collected to the n <sup>+</sup> storage node . . . . .	11
2.4	Altitude dependency of field SER measured in three locations in Japan. Accuracies of estimated field SER with (quasi-)mono-energetic neutron method and simulated field SER with the simulator CORIMS are demonstrated (© 2002 IEEE) . . . . .	12
2.5	Quasi-mono-energetic neutron energy spectra in various facilities (FNL, CYRIC, and TSL) . . . . .	13
2.6	Typical conventional Weibull Fit curve . . . . .	14
2.7	Sequential classification algorithm of SEE in time domain (© 2006 IEEE) . . . . .	15
2.8	Topological classification algorithm of MCU in space domain (© 2006 IEEE) . . . . .	16
2.9	Example of MCU codes and categories . . . . .	17
2.10	Triple-well structure of the one-bit SRAM cell model (© 2005 IEEE) . . . . .	18
2.11	Bit multiplicity of MCU in 130 nm SRAM measured at TSL (© 2006 IEEE) . . . . .	19
2.12	Distribution of SEUs along with bit line. <i>Arrows</i> indicate p-well tap locations where V <sub>SS</sub> is supplied. <b>(a)</b> Single-bit upset <b>(b)</b> Multi-cell upset (© 2006 IEEE) . . . . .	20
2.13	Three categories identified in each run. For <i>bars</i> in each data pattern correspond to neutron energies of 21, 46, 96, 176 MeV, respectively, from <i>left side</i> (© 2006 IEEE) . . . . .	21

2.14	MCU code dependency in data pattern and neutron peak energy for group A (CHB) and group B (all 0) . . . . .	21
2.15	Mechanism of MCBI (© 2005 IEEE) . . . . .	22
2.16	Mechanism of error bit pattern dependency on data pattern . . . . .	22
2.17	Energy spectra of secondary ions produced from Si by neutron spallation reaction with neutron energy spectrum in NYC (© 2010 IEEE) . . . . .	25
2.18	Charge density spectra in Si of secondary ions as functions of energy (© 2010 IEEE) . . . . .	25
2.19	Mean range of secondary ions in Si as functions of energy (© 2010 IEEE) . . . . .	26
2.20	Dynamic cell shift (DCS) method to track ion trajectory in the infinite cell matrix (© 2010 IEEE) . . . . .	27
2.21	Method to set any data pattern on the cell matrix . . . . .	28
2.22	Comparison of SEU cross-sections measured by (quasi-) monoenergetic neutron test and simulated by using CORIMS . . . . .	29
2.23	Predicted trends in SER per device and Mbit (© 2010 IEEE) . . . . .	31
2.24	Predicted trend in MCU ratio and maximum bit multiplicity in MCU (© 2010 IEEE) . . . . .	32
2.25	Charge deposition density spectra when secondary ions penetrate the storage node (© 2010 IEEE) . . . . .	34
2.26	Total collected charge spectra for 130 and 22 nm process SRAM (© 2010 IEEE) . . . . .	35
2.27	Failed bit map for 58,000 nuclear spallation reaction with NYC sea level neutron spectrum from 130 nm SRAM to 22 nm SRAM (© 2010 IEEE) . . . . .	36
2.28	Change in SEU cross-section curves from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE) . . . . .	37
2.29	Change in MCU cross-section curves from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE) . . . . .	37
2.30	Change in SBU cross-section curves from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE) . . . . .	38
2.31	Change in MCU ratio as a function of neutron energy from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE) . . . . .	39
2.32	Change in MCU bit multiplicity from 250 nm SRAM to 22 nm SRAM (© 2010 IEEE) . . . . .	39
2.33	Example of simulated excitation function of the 90 nm SRAM and fitted curve with sum of two (for proton and heavier ions) modified Weibull Fit curves . . . . .	41
2.34	Chain of NAND gates with FFs in-between to measure gate-level SER in NAND and FFs. By-pass is used by switching to measure SER in FF only . . . . .	42

2.35 Neutron spectrum used for the partial irradiation test in CYRIC. Peak flux is obtained at about 65 MeV (© 2010 IEEE) . . . . . 42

2.36 Layout of irradiation room and a photograph of neutron beam aperture (© 2010 IEEE) . . . . . 44

2.37 Board setup and conceptual layout of experimental components (© 2010 IEEE) . . . . . 45

2.38 Selection of critical components and mechanisms that cause rebooting the BUT (© 2010 IEEE) . . . . . 46

2.39 Critical chip layout and irradiation area on the BUT (© 2010 IEEE) . . . . . 46

2.40 Board casing and CPU access memory map for set A and set B (© 2010 IEEE) . . . . . 46

2.41 Flowchart of irradiation test (© 2010 IEEE) . . . . . 47

2.42 Image of data acquisition and handling (© 2010 IEEE) . . . . . 48

2.43 Comparison of estimated SER in accelerator test and measured SER in field for sets A and B (© 2010 IEEE) . . . . . 49

2.44 Conventional WF curve, an MWF curve shown in Fig. 3.12, and an MWF curve adjusted to make SER estimate based on Eq. (2.3) consistent with the field data (© 2010 IEEE) . . . . . 51

2.45 Concept of availability of tolerable level set for chips. Availability depends significantly on the range of variation (© 2010 IEEE) . . . . . 51

2.46 General design flow of stepwise reduction in SER under the design on upper bound concept. Power consumption, cost, and global warming are key issues (© 2010 IEEE) . . . . . 56

2.47 Single layer hardened-by-design and examples of LABIR . . . . . 57

3.1 Typical configuration of printed board circuit with ground, power supply, and signal lines [2] . . . . . 65

3.2 Semi-anechoic chamber . . . . . 66

3.3 Basic setup and procedures for EMI evaluation . . . . . 68

3.4 Principle of the near-field measurement . . . . . 69

3.5 Iterative procedure for calculation of current distribution . . . . . 69

3.6 Estimated current distribution of CPU board . . . . . 70

3.7 Estimated EMI radiated from the CPU board . . . . . 71

3.8 Sample board . . . . . 72

3.9 Measurement system for near magnetic field distribution . . . . . 73

3.10 Result of near magnetic field distribution measurement . . . . . 73

3.11 Result of detecting current ( $I_x$ ) by pattern matching . . . . . 73

3.12 Magnetic field distribution, anti-phase current probing process, and probing result . . . . . 75

3.13 Probing accuracy with respect to the number of iterations. (a) Anti-phase current probing result. (b) Equi-phase current probing result . . . . . 76

3.14 Current probing accuracy with respect to current frequency . . . . . 77

3.15 Configuration of fabricated PCB. (a) 3.5-Inch hard disk drive chassis and PCB as DUT. (b) Schematic circuit diagram for evaluation board . . . . . 77

3.16 The location of GND connection dependence of electric field 3 m away. Screws 1–4 indicate the result with only each connection individually . . . . . 78

3.17 Frequency spectra of junction current. Each plot shows the result with only each connection of screw (e.g., screw 1 indicates the current of screw 1 with only connection of screw 1) . . . 79

3.18 Far-field electric field measurement result with connections of only screw 1, only screw 4, and both of screws 1 and 4 . . . . . 80

3.19 Frequency spectra of junction current for screw 1 with only connection of 1 and with connections of 1 and 4, and for screw 4 with connections of 1 and 4 . . . . . 81

3.20 LCR meshed network model of PCB and chassis in SPICE simulation . . . . . 82

3.21 Calculation results of junction current. Each plot shows the result with only each connection (e.g., screw 1 indicates the current of screw 1 with only connection of screw 1) . . . . . 83

3.22 Calculation results of junction current for screw 1 with only connection of 1 and with connections of 1 and 4, and for screw 4 with connections of 1 and 4 . . . . . 83

3.23 Dependence of junction current on the location of additional bypass capacitor. (a) Location of additional bypass capacitor on meshed model. (b) Calculation results of junction current at screw 4 with only connection of screw 4 changing the location of additional bypass capacitor . . . . . 84

3.24 Additional bypass capacitor located close to the screw for experiment . . . . . 85

3.25 Frequency spectra of far-field electric field with/without additional bypass capacitor . . . . . 86

3.26 Improvement of radiated emission with additional capacitors . . . . . 87

3.27 Measurement results of junction current for screws 1 and 4 with connections of both screws 1 and 4 with/without 1,000 pF capacitors . . . . . 87

4.1 Influence of power supply noise . . . . . 92

4.2 Two types of clock jitter: (i) cycle-to-cycle jitter, (ii) peak-to-peak jitter . . . . . 93

4.3 Single-ended transmission line . . . . . 95

4.4 Single-ended signaling with reference voltage . . . . . 96

4.5 Differential signaling scheme . . . . . 96

4.6 Single-ended signaling with reference voltage . . . . . 97

4.7 Influence of the power supply noise for differential transmission line . . . . . 98

4.8 Trend of power supply voltage for CMOS circuits. Voltage noise margin and process technology are also plotted . . . . . 99

4.9 Trends of power supply current and transient current of high performance microprocessors . . . . . 100

4.10 Demands of small factor for semiconducting products . . . . . 100

4.11 Power Gating Technique using (a) PMOS Gating, (b) NMOS Gating, and (c) Dual Gating (© IEEE) . . . . . 101

4.12 Selective powering down of Lincroft power domains with power gates (© IEEE) . . . . . 102

4.13 Definition of the voltage noise variation . . . . . 103

4.14 A possibility of appearance of quite large noise when several waves overlap with certain phase . . . . . 103

4.15 Relationship between noise source and response . . . . . 104

4.16 Specification of  $V_{REF}$  voltage noise margin for DDR3 SDRAM . . . . . 105

4.17 Time-domain simulation model that consist of all components in the PDS . . . . . 107

4.18 (a) Transient simulation results of the PDS. (b) Frequency domain analysis for the circuit model . . . . . 108

4.19 Trend of power supply voltage and target impedance . . . . . 109

4.20 Impedance profile and step response of a 10-milliohm Big-V PDN with AVP (© IEEE) . . . . . 110

4.21 Schematic of jitter generation due to supply noise (© IEEE) . . . . . 111

4.22  $V_{DDQ}$  supply noise sensitivity profile (© IEEE) . . . . . 111

4.23 Measurement setup of  $V_{REF}$  noise tolerance (© IEEE) . . . . . 112

4.24 Voltage waveform induced to  $V_{REF}$  (© IEEE) . . . . . 113

4.25 Measured  $V_{REF}$  noise tolerance (shmoo plot) of DDR2-SDRAM test chip (© IEEE) . . . . . 113

4.26 Practical setting of target impedance (© IEEE) . . . . . 114

4.27 Combination of frequency and time-domain approach . . . . . 115

4.28 Power distribution network description . . . . . 116

4.29 Circuit parameters control the low-frequency step response . . . . . 117

4.30 Most voltage regulators behave like this simple circuit . . . . . 117

4.31 Passive components of PDS included in PCB and LSI package . . . . . 118

4.32 Equivalent circuit model and impedance profile of bypass capacitor . . . . . 119

4.33 Example of capacitor land and mounting geometry . . . . . 119

4.34 BGA balls for LSI package . . . . . 121

4.35 The PDS which has flat impedance profile for all frequency range (© IEEE) . . . . . 122

4.36 The PDS which has dips and peaks in impedance profile (© IEEE) . . . . . 122

4.37 Impedance profile for parallel bypass capacitors with different types . . . . . 123

4.38 Bypass capacitor with different BQF . . . . . 124

4.39 LW inverse bypass capacitors . . . . . 125



- 4.40 Comparison of impedance profiles of normal and multi-terminal caps . . . . . 125
- 4.41 Impedance profile dependence of PDS with different number of capacitors . . . . . 126
- 4.42 Simultaneous low to high transition . . . . . 126
- 4.43 Bit number dependence of simultaneous switching noise for two kinds of LSI package . . . . . 128
- 4.44 Simplified model of SSN (2-bit case) . . . . . 128
- 4.45 Simplified model of SSN (4-bit case) . . . . . 129
- 4.46 Parallel *Leff* . . . . . 129
- 4.47 An example of single-resonance PDNs (© IEEE) . . . . . 130
- 4.48 Time-domain impulse response of PDNs (© IEEE) . . . . . 131
- 4.49 Overall block diagram of on-chip sampling oscilloscope (© IEEE) . . . . . 132
- 4.50 Measured and simulated waveforms of power supply line with varying decoupling capacitor location (© IEEE) . . . . . 133
- 4.51 In situ supply-noise-map measurement scheme (© IEEE) . . . . . 133
- 4.52 Sampling of a ring oscillator (© IEEE) . . . . . 134
- 4.53 Measured local supply noise by VMON1 (© IEEE) . . . . . 135
- 4.54 Single and *N*-inverter chain output delay by a voltage drop (© IEEE) . . . . . 135
- 4.55 Inverter chain circuit for on-chip voltage measurement (© IEEE) . . . . . 136
- 4.56 Comparison of measurement (dashed) and simulation (solid) results (© IEEE) . . . . . 137
- 4.57 The concept of IFDIM measurement (© IEEE) . . . . . 138
- 4.58 IFDIM measurement setup (© IEEE) . . . . . 138
- 4.59 Correlation between IFDIM measurement and power SI simulation (© IEEE) . . . . . 139
- 4.60 Concept of impulse response method (© IEEE) . . . . . 139
- 4.61 Comparison of voltage waveforms between experiment (Exp.) and simulation (Sim.) (© IEEE) . . . . . 140
- 5.1 Series system . . . . . 145
- 5.2 Parallel system . . . . . 145
- 5.3 Markov model . . . . . 146
- 5.4 Functional safety standards . . . . . 148
- 5.5 Reliability comparison . . . . . 149
- 5.6 Error of commission and error of omission . . . . . 150
- 5.7 Stand-by redundancy . . . . . 151
- 5.8 Majority voting redundancy . . . . . 151
- 5.9 HMR . . . . . 151
- 5.10 Self-purging voting . . . . . 152
- 5.11 Dependable system matrix . . . . . 152
- 5.12 Dependable system . . . . . 154
- 5.13 Synchronization and overhead in task/message level . . . . . 154
- 5.14 Synchronization and overhead in clock level . . . . . 155

5.15	Signal propagation delay	155
5.16	Delay vs. frequency	156
5.17	Bus Guardian	159
5.18	Cascade TMR	159
5.19	Expertise in dependability	162
5.20	Autonomous decentralized system	162
5.21	Autonomous decentralized system	163
5.22	Self-checking application	165
5.23	Mechanism of misdetection	167
5.24	Order of $R_d$	167
5.25	System configuration for the SNV	168
5.26	Configuration of MV	168
5.27	Switch logic of MV	169
5.28	Hiten OBC	169
5.29	Chronology chart of the Hiten OBC	171
5.30	SEUs in each portion of the OBC	172
5.31	OBC structure	172
5.32	SEU occurrence	172
5.33	Reliability with redundancy management	173
5.34	Basic idea of redundancy management	174
5.35	Behavior of redundancy management	174
5.36	Online regulator tuning	175
5.37	Behavior of redundancy management	176
5.38	Behavior of redundancy management	176
5.39	Self-checking comparator	177
5.40	Waveforms in the self-checking comparator	178
5.41	Cross-talk among wiring nets	178
5.42	Concept of time diversity	179
5.43	Effect of time diversity (in macroscopic aspect)	179
5.44	Effect of time diversity (in microscopic aspect)	180
5.45	Effect of time diversity	180
5.46	Effect of time diversity (power supply noise reduction)	181
5.47	Effect of time diversity (runaway ratio reduction)	181
5.48	Effect of time diversity (retry coverage improvement)	182
5.49	Experimental system	182
5.50	Self-checking processor prototype	183
5.51	Recovery process in task-level synchronized systems	183
5.52	Recovery process in clock-level synchronized systems	184
5.53	Self-checking LSI prototype	185
5.54	ATP (automatic train protection) system	186
5.55	Safety micro-controller prototype (FUJINE)	187
5.56	Safety micro-controller	187
5.57	Immediate/deferred reconfiguration	188
5.58	Intra-board synchronization	189
5.59	TPR architecture	190

5.60	Signal flow on fault in MPU A . . . . .	191
5.61	Deferred reconfiguration . . . . .	192
5.62	FT of FT mechanism . . . . .	193
5.63	MPU checker . . . . .	193
5.64	FT-6100 . . . . .	195
5.65	3500/FT . . . . .	196
5.66	Congenial applications for ADS . . . . .	197
5.67	Scale merit for X-by-Wire . . . . .	197

# List of Tables

2.1	Comparison of bipolar action mechanisms in CMOSFET device	23
2.2	Assumed roadmap of SRAM parameters	30
2.3	General trends obtained from simulation (CHB)	30
2.4	General trends obtained from simulation (All1)	31
2.5	Major predicted categories and MCU codes	33
2.6	Merits and demerits of full and partial board irradiation	43
2.7	Parameters used for conventional Weibull Fit and their possible ranges	44
2.8	Test results of SER normalized at Tokyo sea level for set A and B in accelerated and field tests	49
2.9	Concepts of mitigation design of chip-level SER	53
3.1	Measuring and detecting parameters	73
3.2	Derived parameters for model	82
4.1	Comparison of each design methodology with different domain	114
5.1	Necessity for Dependability	143
5.2	SIL (Safety Integrity Level): Low demand mode of operation	147
5.3	SIL (Safety Integrity Level): High demand mode of operation or continuous mode of operation	147
5.4	Specification of OBC	170
5.5	SEU rates	191
5.6	System reconfiguration on fault occurrence	194
5.7	MPU checker (Fault location vs. Comp. report)	194
5.8	MPU checker (Comp. result vs. rationality check result)	194

# List of Acronyms

ACCM	AC common-mode conversion
ALARP	as low as reasonably practicable
ATP	automatic train protection
BGA	ball grid array
BOM	bill of materials
BQF	bypass quality factor
CDR	clock data recovery
CHB	checker board
CHBc	checker board complement
CMRR	common-mode reduction ratio
CORIMS	cosmic radiation impact simulator
COTS	commercial off-the-shelf
DDR	double data rate
DMAC	direct memory access controller
DOA	design on average
DOAV	design on average and variation
DOUB	design on upper bound
DRAM	dynamic random access memory
ECC	error correction code
EMC	electromagnetic compatibility
EMI	electromagnetic interference
ENIAC	electronic numerical integrator and computer
ESL	equivalent series resistance
ESL	equivalent series inductance
ESR	equivalent series resistance
FDTIM	frequency-domain target impedance meter
FIT	failure in time, failure unit
FPGA	field programmable gate array
FTMP	fault-tolerant multi-processor
GND	ground
HMR	hybrid modular redundancy
IFDIM	integrated power-supply frequency-domain impedance meter

ISAS	Space and Astronautical Science of Japan, currently Institute of Space and Astronautical Science, Japan Aerospace Exploration Agency (JAXA)
ISI	inter-symbol interference
JAXA	Japan Aerospace Exploration Agency
JPL	jet propulsion laboratory
LSI	large-scale integrated circuit
MASR	modified asymmetrical slew rate
MBU	multi-bit upset
MCBI	multi-coupled bipolar interaction
MCP	multi-chip package
MCU	multi-cell upset
MFTF	mean fluence to failure
MOS	metal oxide semiconductor
MTTF	mean time to failure
MTTR	mean-time to repair, or mean-time to restoration
NMR	N-tuple modular redundancy
OBC	onboard computer
OLTP	online transaction processor
OSPM	operating system power management
PCB	printed circuit board
PCSE	power cycle soft error
PDN	power distribution network
PDS	power distribution system
PI	power integrity
PKG	package
PLL	phase locked loop
PoP	package on package
PWL	piecewise linear
RAM	random access memory
RF	radio frequency
SBU	single-bit upset
SDRAM	synchronous dynamic access memory
SEB	single-event burnout
SEFI	single-event functional interruption
SEGR	single-event gate rupture
SEL	single-event latchup
SER	soft-error rate
SESB	single-event snap-back
SEU	single-event upset
SIFT	software implemented fault tolerance
SIL	safety integrity level
SNV	stepwise negotiating voting
SPICE	simulation program with integrated circuit emphasis
SRAM	static random access memory

SSN	simultaneous switching noise
STAR	self-testing and repairing
TMR	triple modular redundancy
TRON	the real-time operating system nucleus
TTP	time-triggered protocol
USEF	Institute for Unmanned Space Experiment Free Flyer
VRM	voltage regulator module
ZIR	zero-input response
ZSR	zero-state response