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Load-Pull Techniques with Applications to Power Amplifier Design

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Fadhel M. Ghannouchi dedicates this book to his wife Asma, and daughters Layla and Nadia

Mohammad S. Hashmi dedicates this book to his wife Rabeya, and son Jafar

Preface

For the purpose of identifying the large-signal behavior of the transistor devices, the use of linear S-parameter is often inadequate. Large-signal characterization, therefore, is essential for the estimation and determination of the device performance in the nonlinear domain. The load-pull approach is one recommended approach for the large-signal characterization, optimization, and design of transistor devices and radio frequency (RF), microwave and mm-wave power amplifiers (PAs).

The load-pull technique was first reported almost four decades ago. This pioneering work brought a paradigm shift in the characterization, measurement, and optimization of transistor devices and PAs. The first load-pull setup can be considered rudimentary but has definitely helped in advancing the state-of-the-art in load-pull techniques.

This book describes the principles of operation, calibration, design and realization approaches and application of load-pull techniques in the context of PAs. It explores the topic from the basic principles of load-pull techniques through to their many interesting advancements, including passive and active techniques, high power load-pull and envelope load-pull setups with applications to amplifier, mixer and noise measurements. In addition, the book also covers waveform engineering systems, their calibration techniques and applications.

The book can be used by graduate students, researchers and design engineers in microwave and wireless design areas. It is assumed that the readers have already acquired a basic knowledge of RF and microwave circuit design. A solid background in transmission line theory and basic communication concepts is required. The book may also be used as a textbook for a graduate course on large signal device measurement and characterization.

Chapter 1 is a brief reminder of the basic concepts related to PA characteristics, figures of merits of PA, power amplifier classes of operation, PA design methodologies, and introduction to load-pull systems along with their important features.

Chapter 2 is dedicated to passive load-pull techniques. It explains the fundamentals of passive load tuning techniques and elaborates on the two most common techniques, namely electronic tuner (ETS) and electromechanical tuner (EMT), employed to achieve impedance tuning using passing approach. Measurement and

calibration procedure applied in a load-pull measurement setup is then discussed in detail. The chapter also provides extensive details on various passive harmonic load-pull architectures along with their respective advantages and limitations. Subsequently, common techniques used to enhance the tuning range of passive load-pull setups are discussed.

Chapter 3 provides extensive details on active load-pull techniques and systems. It starts with closed-loop active load-pull technique and its realization methods. Adequate details have been included for the design of application specific closed-loop load-pull system. It then covers feed-forward active load-pull and various methods to develop hybrid setup, for enhancing the tuning range and achieving highly reflective load-pull systems. Active open-loop load-pull requires iterative operation of the system for converging on optimal impedance solution. The last section is dedicated to an algorithm for high speed convergence in active open-loop load-pull systems.

Chapter 4 presents the theory, techniques and principles behind using six-port reflectometer in reverse and forward configurations to characterize transistors operated in large signal conditions, and the issues related to the implementation of these techniques are discussed. Source-pull characterization using six-port reflectometer for transistor noise measurement, mixer testing and design, as well as oscillator device line measurement purposes are explained and discussed. AM/AM and AM/PM distortion measurement and passive and active load-pull large signal characterization of transistors using the six-port reflectometer technique are also presented and discussed.

Chapter 5 deals with the issues involved in the characterization of high power microwave transistor devices. There are multiple aspects that need to be addressed in order to overcome those issues. All these have been discussed in detail in this chapter. The techniques adopted in customizing the load-pull setup for high power device measurements and characterization applications have been elaborated and explained in detail. Finally, emerging solutions catering to large periphery high power microwave devices are presented.

Chapter 6 presents the theory of active envelope load pull (ELP) and the associated design and calibration techniques of active envelope load-pull. Thereafter harmonic envelope load-pull is explained in detail which is followed by some unique measurement applications of envelope load-pull system.

Chapter 7 is dedicated to theory and calibration approaches adopted in developing error corrected nonlinear time-domain waveform measurements systems. Subsequently the concept of waveform engineering is presented. Finally, a number of applications of waveform engineering system are discussed.

Chapter 8 presents some advanced applications and configurations of load-pull setups. The first part of this chapter primarily discusses the concept of load-pull systems for multi-tone and modulated excitations. It experimentally demonstrates that such systems are extremely useful for real life practical applications. Then the use of load-pull and source-pull systems in noise characterization is described in detail. Finally application of load-pull systems in mixer characterization and measurements in presented.

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Contents

Chapter 1
Fundamentals

This chapter presents the fundamentals of three aspects, namely radio frequency (RF) power amplifiers, approaches adopted for the optimal design of these amplifiers, and load-pull measurement systems.

1.1 Introduction

The key component in any wireless communication system is the RF power amplifier (RFPA). RFPAs convert the DC power into RF power, which enables the transmission of the RF signal containing digital information from the transmitter to the receiver via wireless environments. The quality of RFPAs, in terms of efficiency and linearity, has a significant impact on the cost, reliability, size and performance of wireless communication systems.

Achievement of both high efficiency and linearity in RFPAs is a complex process, as the power amplifier (PA) has to be designed to operate closer to saturation. Operation of the PA at saturation increases the efficiency, but also increases the distortion. Therefore, the RFPA design process requires a trade-off between two important metrics, namely efficiency and linearity. Here, efficiency refers to the capability of the PA in converting DC power into RF power, which is extremely important as any PA exhibiting low efficiency will consume much more DC power than an efficient one when delivering the same amount of RF power.

For a handheld application that uses a battery as the primary power source, poor efficiency means shorter talk and standby times. This can seriously limit the competency of the final product in the market. Moreover, poor efficiency leads to a large amount of heat dissipation, which requires additional effort and money for high-capacity cooling facilities.

In the context of the PA, linearity refers to a measure of how faithfully a PA can amplify the input signal. PAs always demonstrate certain levels of nonlinearities. The tolerance for nonlinearity really depends on the applications. For example, CDMA (code division multiple access) and WCDMA (wideband code division multiple access) based wireless systems require, apart from the usual high efficiency,

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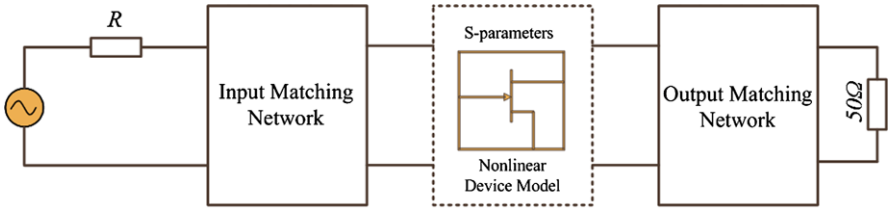

Fig. 1.1 Generic block diagram of a single-stage RF amplifier

a high linearity over a large dynamic power range. In contrast, the linearity is a relatively less serious issue for PAs based on the GSM (global system for mobile applications) standards, due to the constant envelope characteristics of the GSM signal.

It is not possible for the efficiency and linearity to reach their optimal levels simultaneously on a stand-alone power device. Various types of advanced PA architectures, such as Doherty, Kahn and LINC (linear amplification using nonlinear components), have been proposed to achieve good efficiency and linearity at the same time [1–10]. These architectures provide promising results, but inevitably increase the complexity of the communication systems, thereby contributing to higher costs with decreasing reliability. Therefore, it is always a challenge for PA designers to adopt an appropriate optimization solution with which a good compromise in specifications can be reached.

1.2 RF Power Amplifier Characteristics

Before getting into the description of RFPAs, it is prudent to understand the characteristics of RF amplifiers. For this purpose, a generic block diagram of a single-stage RF amplifier is depicted in Fig. 1.1. It consists of input and output matching networks, and a transistor device. Ideally, this configuration is generic both for small- or large-signal power amplifiers.

Matching networks are application specific and are appropriately designed. For example, matching networks can be customized for amplifying extremely small signals with very low noise at the output (i.e., a low noise amplifier), can be designed such that maximum gain is realized, or can be intended for maximum output power (i.e., a power amplifier). Irrespective of the applications, the matching networks are realized using lumped components, distributed elements (transmission lines) or a combination of both. They are basically characterized by intrinsic linear elements and, therefore, are considered linear time-invariant networks.

An active device can, however, be thought as either a linear or nonlinear network, depending on the electrical power range of the signals involved in the process [11]. If the power level of the input signal is so small that the output is just the amplified version of input, as depicted in Fig. 1.2, the device is considered to be operating in linear mode. On the contrary, if the power level of the input is large enough to

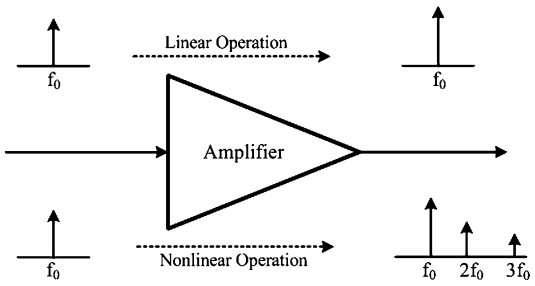

Fig. 1.2 Depiction of linear and nonlinear behavior of an amplifier

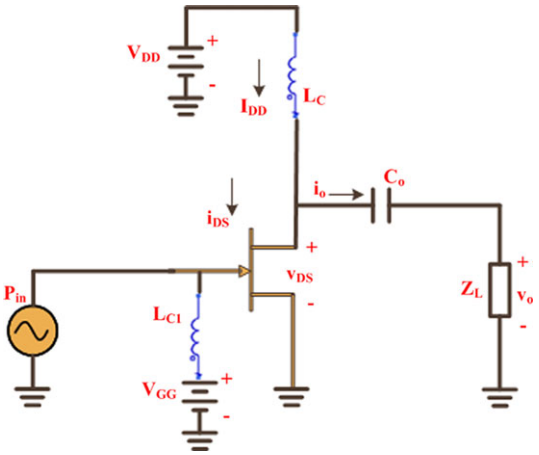

Fig. 1.3 Schematic of an amplifier for definition of load line

generate harmonics in the output signal, as also depicted in Fig. 1.2, the device is said to be operating in nonlinear mode.

The linear mode of operation is modeled in terms of scattering parameters (S-parameters). The S-parameters are frequency dependent, described for a specific biasing condition and independent of the power level of the stimulus. These parameters are inadequate for describing the characteristics of devices operating in nonlinear mode. In order to address this problem, there have been proposals of complex large-signal models [12–15] to describe the nonlinear characteristics of devices.

In an alternative context, it is a common practice to link the performance characteristics of a power amplifier to the load line, as it identifies the capabilities of devices for maximum output power application. The load line represents the trajectory of all the instantaneous values of current (i_{DS}) and voltage (v_{DS}) of a device when it is operated under a specific load and at a given bias point.

For the purposes of the explanation of a load line, let us consider the typical schematic of an amplifier, as given in Fig. 1.3. The amplifier is biased through an RF choke inductor, L_C, with a bias voltage, V_{DD}, and drain bias current, I_{DD}. The DC blocking capacitor, C_0, is selected to be large enough to keep a steady-state voltage, V_{DD}, during the entire RF cycle. During a steady state, this schematic can

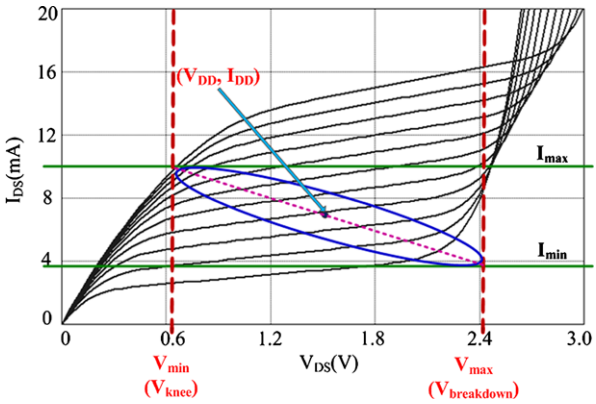

Fig. 1.4 Typical load line of an amplifier (*dashed straight line*: resistive load, *solid elliptic line*: complex load)

be solved to determine the expression between the instantaneous current (i_{DS}) and instantaneous voltage (v_{DS}) given in Eq. (1.1).

$$i_{DS} = I_{DD} - \frac{v_{DS} - V_{DD}}{Z_L} \tag{1.1}$$

Equation (1.1), known as the load line equation, defines the trajectory of all the combination of values (i_{DS}, v_{DS}) of the device under specific operating conditions of a device for specific quiescent points (I_{DD}, V_{DD}) and load impedance (Z_L). For the real value of Z_L, the load line equation represents a straight line; whereas a complex Z_L converts the load line equation into the equation of a shifted and rotated ellipse [78], as shown in Fig. 1.4.

In theory, v_{DS} could be any value and, therefore, can produce any value of i_{DS}. In practice, however, this is not the case, as the load line is regulated by the device DCIV characteristic, as can be seen in Fig. 1.4. It is evident that the trajectory is limited by the knee voltage (V_{min} or V_{knee}), the breakdown voltage (V_{max} or $V_{breakdown}$), the device's maximum current (I_{max}), and the zero value current (I_{min}).

The load line is considered a very effective tool, as it can provide information about the load impedance (real or complex) just by visual inspection. However, it is imperative to understand that if an RF transistor is loaded with 50 Ω impedance without a matching circuit, the load line is an ellipse instead of a straight line. It is due to the presence of intrinsic device output capacitance that combines with the real 50 Ω impedance to form a complex load. In addition, load line trajectories also help in the design of optimal matching circuit by determining the condition when the device output capacitance is canceled out by the matching circuit i.e., the situation when the device sees only real load impedance at its terminals.

1.3 Figures of Merit

Evaluation of an RF power amplifier for any particular application is carried out using established figures of merit, such as drain efficiency (η_D), power-added efficiency (PAE), harmonic distortion, intermodulation distortion, Adjacent Channel

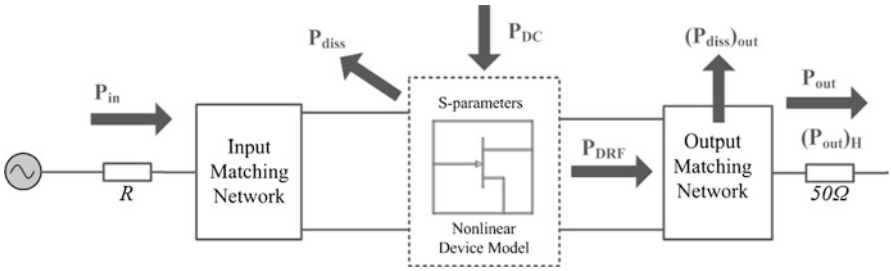

Fig. 1.5 Power flow depiction in a power amplifier

Power Ratio (ACPR), and Error Vector Magnitude (EVM). The values of these figures of merit are the reference values for comparison with other amplifiers using other design techniques or technologies.

1.3.1 Drain Efficiency and Power Added Efficiency

Several forms of the definition of efficiency have been adopted previously, but the most commonly used are drain efficiency (η_D) and the power-added efficiency (PAE). For defining the efficiency metrics, let us look to the power flow in a power amplifier, as depicted in Fig. 1.5. Power P_{in} is the power flowing into the amplifier input over a specified frequency range; whereas P_{out} is the power flowing out of the amplifier over a specified frequency. If P_{in} is only contained in one harmonic component (i.e., the fundamental frequency), then P_{out} is the corresponding power at the fundamental frequency and $(P_{out})_H$ is the output power of the harmonic components generated by nonlinear characteristics of the power amplifier.

The dc power, P_{DC}, is supplied to the active device for the operation of the power amplifier. The active device also receives the input ac power, P_{in}, and dissipates a portion of the combined P_{DC} and P_{in} as heat, while it converts the remaining into ac power, P_{DRF}, which gets delivered to the output matching network. The output network dissipates a portion of P_{DRF} and then delivers the remainder in the form of P_{out} and $(P_{out})_H$. The optimal design of a power amplifier requires minimization of these power losses at various stages and maximization of power transfer to the load with minimal distortion.

The drain efficiency (η_D) is defined as the ratio between the output power (P_{out}) and the dc power (P_{DC}).

$$\eta_D = \frac{P_{out}}{P_{DC}} \tag{1.2}$$

The drain efficiency is good for amplifiers that possess high gain or where the input power comes at no cost. It is a very useful metric in the evaluation of conduction loss independent from the input power dissipation. As the drain efficiency

ignores the effect of input power, it helps measure the effectiveness of the amplifier in avoiding the dissipation on the controlled resistance of the output port [79].

An alternative efficiency metric called total efficiency (η_T), although rarely used but more physically significant, is defined as the ratio of the output power and the sum of all powers fed to the amplifier. From Fig. 1.5, the expression of η_T can be deduced as:

$$\eta_T = \frac{P_{out}}{P_{DC} + P_{in}} \tag{1.3}$$

The total efficiency can be used to measure the effectiveness of an amplifier in reducing the need for heat removal, as can be seen in Eq. (1.4), which relates the total dissipated power, $(P_{diss})_T$, and the total efficiency, η_T [79].

$$(P_{diss})_T = P_{DC} + P_{in} - P_{out} = \left(\frac{1}{\eta_T} - 1\right) P_{out} \tag{1.4}$$

The most commonly used efficiency metric is called PAE which is defined as the (RF) power added by the amplifier, $(P_{out} - P_{in})$, divided by the dc power consumption, P_{DC}.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}\left(1 - \frac{P_{in}}{P_{out}}\right) = \eta_D\left(1 - \frac{1}{G}\right) \tag{1.5}$$

The PAE carries more information than the drain efficiency, as it also depends on the gain of the amplifier (G). While the drain efficiency increases monotonically with the input power, the PAE reaches a maximum and then its value decreases until reaching zero and could even have a negative value.

1.3.2 Intermodulation and Harmonic Distortions

A power amplifier is a nonlinear system that generates harmonic components in addition to the frequency corresponding to the excitation signal. Intermodulation and harmonic distortions quantify the impact of distortion associated with the harmonic components and provide a measure of linearity performance of a power amplifier.

Harmonic distortion is measured when the amplifier is excited with a single-tone test signal and harmonic distortion components are generated at the output, as depicted in Fig. 1.2. Usually the second and third harmonics carry most of the energy; therefore, the harmonic distortions are defined for these harmonic components.

$$HD_{2,dBc} = 10\log\left(\frac{P_{out}(2f_0)}{P_{out}(f_0)}\right) \tag{1.6}$$

$$HD_{3,dBc} = 10\log\left(\frac{P_{out}(3f_0)}{P_{out}(f_0)}\right) \tag{1.7}$$

The harmonic distortions are expressed in dBc relative to the fundamental frequency power. The power level of the harmonics changes with the input power; therefore, the corresponding harmonic distortion figures in dBc change as well.

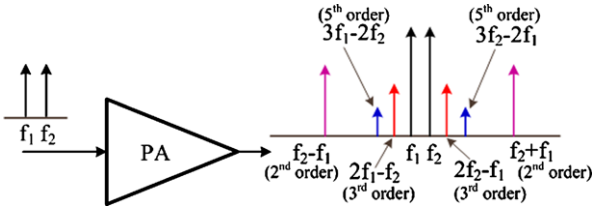

Fig. 1.6 Illustration of the intermodulation products and the associated frequencies with two-tone excitation

Another harmonic distortion term that is very commonly used is called total harmonic distortion (THD) which is given in Eq. (1.8). It includes all the harmonic distortion components in one figure of merit.

$$THD_{dBc} = 10\log\left(\frac{\sum_{n\geq 2} P_{out}(nf_0)}{P_{out}(f_0)}\right) \tag{1.8}$$

Intermodulation distortion (IMD) is more realistic for the actual wireless communication system. It is the result of two or more signals interacting in a power amplifier to produce additional unwanted signals. For example, the additional unwanted signals (intermodulation products) for two input signals occur at the sum and difference of integer multiples of the original frequencies given by Eq. (1.17) and as depicted in Fig. 1.6.

$$(IMD)_{products} = mf_1 \pm nf_2 \tag{1.9}$$

where m and n are integers and define the order of intermodulation products as a sum of $m + n$.

It is evident from Fig. 1.6 that the two-tone third-order components ($2f_1 - f_2$ and $2f_2 - f_1$) are most relevant, as they are very close to the fundamental components and, therefore, cannot be easily filtered. Higher order intermodulation products generally do not affect the performance of PAs significantly, as these components either possess very low amplitudes or are far from the fundamental components [11].

Equation (1.10) corresponds to third-order intermodulation product (IMD3) when the fundamental components f_1 and f_2 are very close.

$$IMD_{3,dBc} = 10\log_{10}\left(\frac{P_{out}(2f_2 - f_1)}{P_{out}(f_2)}\right) \approx 10\log_{10}\left(\frac{P_{out}(2f_1 - f_2)}{P_{out}(f_1)}\right) \tag{1.10}$$

Another metric to describe the linearity performance of a power amplifier is known as the intercept point. For third-order products, it is known as the third-order intercept point (IP3), as shown in Fig. 1.7. IP3 is an important parameter and helps in the estimation of spurious free dynamic range (DR_{SF}) [80].

It is important to understand that THD, IMD3, and IP3 are good metrics for describing the performance of PAs exhibiting weak memory effects [16]. However, these are insufficient for the situations when the PAs exhibit strong nonlinearity.

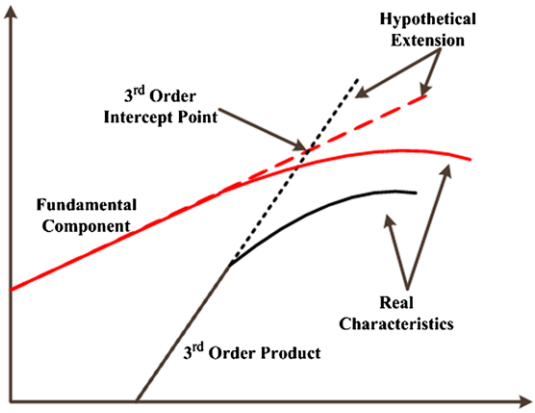

Fig. 1.7 Representation of third-order intercepts point

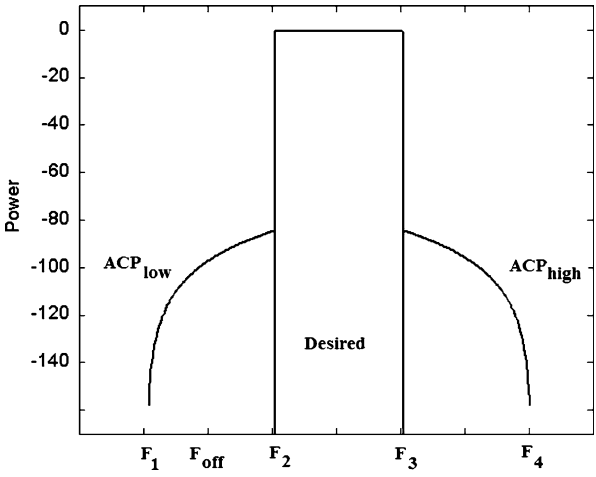

Fig. 1.8 Ideal representation of main and adjacent channel power spectra and their respective frequency band definitions [81], © IEEE 2006

1.3.3 Adjacent Channel Power Ratio

For amplifiers exhibiting strong nonlinearity or for digitally modulated excitations, adjacent channel power ratio (ACPR) is more relevant considering that harmonic distortion is applicable for single tone excitation and the usefulness of intermodulation distortion is limited to excitations with specified number of tones (usually 2).

ACPR describes the level of spectral regrowth and is often expressed in dB below the main carrier power (dBc) as depicted in Fig. 1.8 and is expressed as the ratio of the power leaking into the adjacent channel to the power in the main channel given by Eq. (1.11) [17].

$$ACPR_{dBc} = 10\log\left(\frac{\int_{F_2}^{F_3} P(F)dF}{\int_{F_1}^{F_2} P(F)dF}\right) \tag{1.11}$$

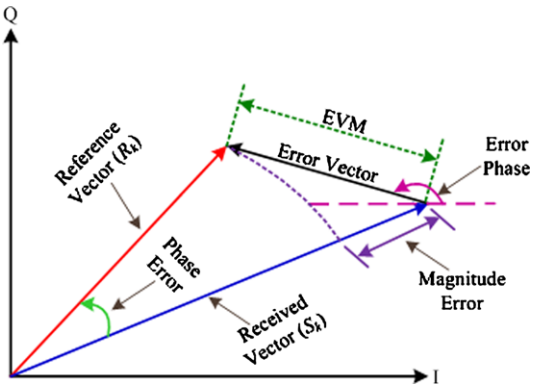

Fig. 1.9 Illustration of error vector magnitude (EVM) and its components

The plot shows a representative power spectrum showing the driving signal (between frequencies F_2 and F_3) and the adjacent channel power (ACP) resulting from third order interactions only. In an ideal system, ACPR should be as high as possible as it conveys that the leakage from the main channel to the side channel is low.

Alternatively, a measure of ACPR is the distortion level at a given frequency offset F_{off} from the lowest desired frequency (F_2) [81].

1.3.4 Error Vector Magnitude

According to 3GPP standards, EVM is a measure of the difference between the reference waveform and the measured waveform [82]. The difference is called error vector, illustrated in Fig. 1.9, and the EVM, usually mentioned in percentage, is defined as the square root of the ratio of the mean error vector power to the mean reference power expressed in Eq. (1.12).

$$EVM_{RMS} = \sqrt{\frac{\sum_{k \in K} |S_k - R_k|^2}{\sum_{k \in K} |R_k|^2}} \tag{1.12}$$

where S_k is the received (measured) vector, R_K is the reference symbol vector, and K is the total number of symbols.

The ACPR provides information about the out-of-band distortion, the error vector magnitude (EVM) estimates the in-band distortion caused by the amplifier nonlinearities. EVM possesses a direct relation with the signal to noise ratio and can be used to determine the physical error introduced at different stages of communication system and thus serves as an easily tool for designers in troubleshooting specific problems. One of the advantages of EVM is the simplicity in their measurement as it does not require an entire communication system, instead EVM can be calculated from the measured down-converted digitally modulated radio signal [17].

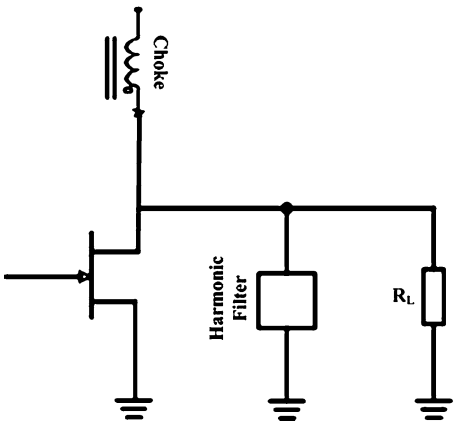

Fig. 1.10 A generic topology of transconductance amplifier

1.4 Power Amplifier

Transconductance amplifiers, in which the transistor device is operated as a current source and whose current is dependent on the voltage presented to its input, are the most common types of power amplifiers. In these amplifiers, the transistor devices drive a controlled current into a load network which consists of a harmonic filter and resistive load as depicted in Fig. 1.10. The harmonic filters are designed in such a way that it possesses high impedance at fundamental frequency and extremely low impedance at the harmonics. This ensures that the impedance presented to the device at the fundamental frequency is simply the load resistance, R_L, whereas the harmonics are presented with virtually open circuit. As a result, the voltage across the device output port remains sinusoidal for any current driven by the device.

It is imperative to understand that performance, such as efficiency, of transconductance amplifiers can be varied by varying the shape of current waveform considering that these amplifiers are utilize transistor devices as current source. The modification or shaping of current waveforms leads to operating classes of power amplifiers namely class-A, class-B, class-AB, class-C, and class-F.

In class-A, the transistor device is biased in such a way that it conducts current all the time. In theory, the current through the device should exactly replicate the shape of the input voltage signal; and, the dc bias current should be sufficient to ensure that the device remains in conductance region at all times [79]. To satisfy this requirement and to obtain the optimal performance of the amplifier in class-A mode, the biasing point (I_{DD}, V_{DD}) shown in Fig. 1.11 is chosen according to Eqs. (1.13) and (1.14). This biasing provides plenty of room for the output signal swing, and hence the chances of reaching cut-off and saturation regions are small. It is primarily due to this reason that class-A amplifier exhibits very low distortion in its output.

$$I_{DD} = \frac{I_{max}}{2} \tag{1.13}$$

$$V_{DD} = V_{knee} + \frac{V_{max} - V_{knee}}{2} = \frac{V_{max} + V_{knee}}{2} \tag{1.14}$$

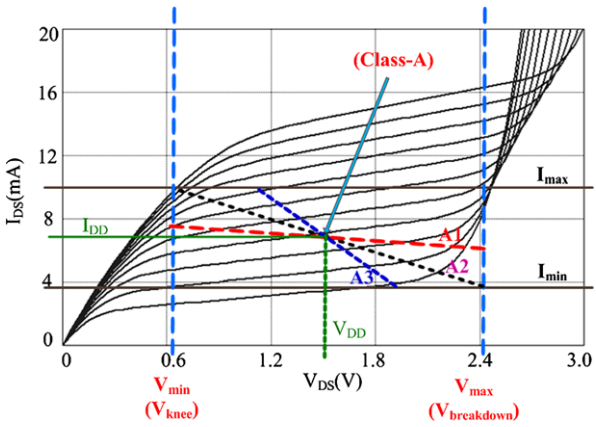

Fig. 1.11 Load lines for different loading conditions

The bias point defined by Eqs. (1.13) and (1.14) are also applicable for small-signal amplifiers. However there is significant difference in the operation of large-signal (power) amplifier and the small-signal amplifier. In the case of small-signal, the appropriate matching involves the termination of device output with its complex conjugate. Under this type of matching the device load line, plotted using Eq. (1.1), is represented by A1 in Fig. 1.11 [83]. It is apparent that in such a situation the current swing is less than the maximum device current (I_{max}). Similarly for load impedance with a smaller resistance than the device output resistance, the load line is the one indicated as A3 in Fig. 1.11 and this leads to a condition where the voltage swing is smaller as compared to the maximum voltage rating (V_{max}).

In the cases of both A1 and A3, the maximum achievable output power is not reached, as these load lines do not utilize the full current and voltage swings. However, for a power amplifier, the goal is to obtain maximum output power from the device; therefore, the load line must correspond to the one marked as A2 in Fig. 1.11. For load line A2, the real part of load impedance given by Eq. (1.15) is dependent on the maximum current and voltage ratings of the device, while the imaginary part of load impedance is selected in such a way that it cancels the output reactance of the device. However, this optimal value of load impedance for maximum output power creates a mismatch between the device and load impedance and has the potential to cause a high voltage standing wave ratio (VSWR) at the output of the device [18].

$$\mathrm{Re}(Z_L)_{opt\text{-}classA} = (R_{opt})_{classA} = \frac{V_{max} - V_{knee}}{I_{max}} \tag{1.15}$$

The voltage and current at the device output in the class-A operation mode are sinusoidal and swing between the minimum and maximum values, which are dependent on the device's technology. In such a situation, expressions for the dc power delivered to the device, the power at the output of device, and the drain efficiency are given as:

$$P_{DC} = V_{DD} I_{DD} = \left(\frac{I_{max}}{2}\right)\left(\frac{V_{max} + V_{knee}}{2}\right) \tag{1.16}$$

$$(P_{out})_{classA} = \frac{I_{out}^2 (R_{opt})_{classA}}{2} = \frac{(I_{max}/2)^2}{2}\left(\frac{V_{max} - V_{knee}}{I_{max}}\right)$$
$$= \frac{I_{max}(V_{max} - V_{knee})}{8} = \frac{I_{max}(V_{DD} - V_{knee})}{4} \quad (1.17)$$

$$(\eta_D)_{classA} = \frac{(P_{out})_{classA}}{P_{DC}} = \frac{V_{max} - V_{knee}}{2(V_{max} + V_{knee})} = \frac{V_{DD} - V_{knee}}{2V_{DD}} \quad (1.18)$$

It is apparent from Eqs. (1.16), (1.17), (1.18) that output power and drain efficiency of class-A PA increases with the square of the output current I_{out}; whereas the consumed dc power is constant. For class-A, the optimum values of P_{out} and efficiency occurs for the situation when the current I_{out} reaches its maximum value $(I_{max}/2)$.

The theoretical maximum drain efficiency of class-A PA reaches 50 % when the knee voltage (V_{knee}) is very small. This low value is contributed by the continuous consumption of dc power. In order to overcome this issue, and to improve the efficiency of PAs, bias current (I_{DD}) is reduced while keeping the same maximum voltage and current swing. The reduction in the bias current is achieved by reducing the conduction angle, which forms the basis of reduced conductions angle power amplifiers [83].

In order to enhance the efficiency of transconductance amplifier, it is essential to have at least one of the waveforms to be non-sinusoidal. For the replication of this condition, the voltage waveform is kept same as in class-A while the current waveforms are altered such that there are periods in which the device does not conduct. The PAs in such a situation are called reduced conduction angle power amplifiers with the assigned terminology of classes AB, B, and C; as summarized in Table 1.1. The conduction angle (α) is determined by the quiescent gate voltage (V_{GSQ}), which is a function of the device pinch-off voltage (V_p) as well as the device built-in voltage (V_{bi}).

It is also important to understand that the linearity of PA is affected by the reduction in the conduction angle. It is essentially due to the fact that the output current and voltage has smaller swing in the linear region when the conduction angle is reduced. The most linear amplifier is obtained for class-A operation and the linearity worsens while moving from class-A to class-C. An amplifier operating in class-A or class-B exhibits similar linearity performance if the transconductance of the device (g_m) remains constant [21]. However, in practical situations this is not normally the case and as a consequence class-A power amplifier exhibits better linearity.

Even with all the advantages, the reduced conduction angle power amplifiers with shorted harmonics have some limitations. The main problem of such power amplifiers lies in the fact that it involves increase in the input RF signal with the reduction in the conduction angle if the peak current is to be maintained constant. As a consequence, the gains of such amplifiers get reduced which limit the usefulness of these techniques in the design of amplifiers with devices possessing high gain.

An alternative solution to overcome the problems caused by harmonics present in the output of the PA is to provide either an open circuit condition at all harmonics except the fundamental frequency for achieving class-E and class-D operation modes [19, 20, 22, 23] or drain current and voltage shaping for achieving class-F, class-F^{-1},