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David J. Lockwood *Editors*

Silicon Photonics III

Systems and Applications

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Preface

This is the third volume in the Silicon Photonics series, which we started in 2004 with a book simply entitled Silicon Photonics. At that time, the field was in its infancy and the research was concentrated on the basic building blocks for integrated photonic circuits. Then in 2011, we edited the second volume, Silicon Photonics II: Components and Integration. This volume was devoted to the description of the different requirements needed to integrate the basic building blocks into integrated circuits. Today, we present this book where we focus on the state of the art of silicon photonics in industry and also make comparisons with other competing technologies. It is impressive to see the paradigmatic change that the field has witnessed in just 5 years. Specifically, silicon photonics has moved from the research laboratory to manufacturing companies. Indeed, in the first books, the contributors were mainly from academia, while in the present volume, more than half of them are from companies.

In Chap. 1, the use of silicon photonics to solve the bandwidth bottleneck of inter-chip interconnects is addressed. Fully hybrid integrated systems are described and a bandwidth density of 30 Tbps/cm^2 is demonstrated. In addition, the problem of the temperature reliability of the system is addressed with the discussion of error-free data links operating up to 125 °C at 25 Gbps. The use of quantum physics and its integration in silicon photonics is at the heart of Chap. 2. Quantum technologies promise to revolutionize the way we handle information. Though the control of quantum systems remains extraordinarily challenging, silicon quantum photonics, with its density and manufacturability, is a credible challenger.

One still open issue in silicon photonics is the temperature dependence of many of its components. Chapter 3 reviews the various approaches to overcome the high temperature dependence of wavelength-filtering devices such as ring resonators and arrayed waveguide gratings. Based on specific designs, athermal devices are presented. Key to this achievement is a proper simulation software that enables the development of athermal geometries. Chapter 4 discusses the challenges and the opportunities in photonic integrated circuit design software tools, examines existing design flows for photonic design, and how these fit different design styles.

Modeling of chip-scale interconnects is presented in Chap. 5 with reference to high-performance computer systems that need to distribute extremely large amounts of data in an energy efficient manner. A fully functional co-integrated hardware–software system is presented to encompass device functionality, control schema, and software logic seamlessly. Each layer, ranging from individual device characterization, to higher layer control of multiple devices, to arbitration of networks of devices, and ultimately to encapsulation of subsystems to create the entire computing system is explored.

Silicon photonics is going to enable more and more commercial applications as the technology matures. This will increase the demand for foundries to produce the photonic integrated chip. The accessibility to foundries becomes then a critical aspect for any business models. Chapter 6 reports on the foundry services for multi-project wafer shuttles, customized process runs, and small volume production. Results and challenges in setting up a CMOS manufacturing foundry line for silicon photonics research and development along with commercialization are also presented. A specific aspect is the move from the chip to the packaged device. In Chap. 7 the path from a device-by-device packaging to automatic packaging, which allows scaling to high volumes, is described. Packaging challenges still remain in areas such as fiber array coupling, laser source and electronic integration, and efficient thermal management. The problems and the challenges to automatize the fiber array pigtailing and the laser integration in relation to silicon photonics devices are addressed in Chap. 8. Solving these manufacturing issues, whether silicon photonics needs a dedicated fab or not, still remains an open topic. Megafabs produce 10,000–25,000 12″ wafers per week in their normal capacity. The silicon photonics industry has the potential for approximately 25,000 wafers per year or ~500 wafers per week by 2021. This volume forethought and the path to low-volume production of silicon photonics devices are presented in Chap. 9. With growing production volume, dedicated fabs are needed. Chapter 10 presents the development of silicon photonics within a CMOS line. Cost process issues, efficient electronic and photonic integration, a usable design kit, an industrial testing strategy, and a low cost packaging strategy are discussed and presented from the perspective of a complete industrialization of silicon photonics.

Applications of silicon photonics are diverse. Chapter 11 reports on the use of silicon photonics for signal processors in microwave photonic frontends. These are especially attractive for their compact size and performance. Silicon photonics for optical interconnect applications is addressed in Chap. 12. The development of transceivers is presented starting from wafer process technology to photonic device libraries, to integration with electronic circuits and optical probing technology. An alternative approach to silicon photonics transceivers is discussed in Chap. 13. The heterogeneous integration of InP into a silicon photonics platform enables the inclusion of all photonic elements in a cost-effective manufacturing process. Chapter 14 compares the two technologies and reviews the technical merits of silicon photonics devices and integrated circuits. Various applications such as chip-scale optical interconnects, short-reach communications in datacenters and supercomputers, and metro/long-haul optical transmissions are enabled by the

technical merits of silicon photonics. Specifically, in Chap. 15 silicon photonics for telecom and datacom is reviewed. Detailed architectures to enable high-performance systems are discussed. Chapter 16 focuses on the fundamental and high-speed characteristics of small-footprint integrated optical modulators designed and fabricated with silicon photonics. Here the application framework is digital coherent communication in optical fiber links and the demonstration of long-haul transmission of up to 1000 km in length at a bit rate as high as 128 Gbps is reported. Datacenters are the application discussed in Chap. 17. An overview of optical interconnect requirements for large-scale datacenters is presented here together with a comparison between silicon photonics technologies and more traditional options in meeting these requirements. Finally, Chap. 18 unfolds a technology roadmap of VLSI photonics applications for datacenters from an industrial perspective. The roadmap of the microelectronics industry development indicates that Si will remain the prime microelectronics material. Therefore, sophisticated silicon photonics devices will serve as the backbone for new architecture to bring the next generation of datacenters to the world soon.

We feel honored to be the editors of this series of volumes on Silicon Photonics, because we have witnessed the evolution of this field from a privileged point of view and could accompany it from its infancy to full maturity. Nevertheless, in these volumes, we have also tried to perceive the future of silicon photonics in terms of both industrial applications and fundamental research. We thank all the authors of the present volume for their invaluable contributions, the staff of Springer for their support, and our co-workers for sharing with us their research in this field. We look forward to further excitement ahead and new developments in silicon photonics, and we hope to share them with you, our esteemed readers, in the next volume of this series.

Trento — Lorenzo Pavesi
Ottawa — David J. Lockwood
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Chapter 1
Silicon Optical Interposers for High-Density Optical Interconnects

Yutaka Urino, Takahiro Nakamura and Yasuhiko Arakawa

Abstract One of the most serious challenges in the information industry is bandwidth bottlenecks in inter-chip interconnects. We proposed a photonics–electronics convergence system in response to this issue, demonstrated silicon optical interposers integrated with all optical components on a silicon substrate, and achieved a high bandwidth density of 30 Tbps/cm^2, which is sufficient for the needs of the late 2010s.

1.1 Introduction

1.1.1 Trends and Requirements of Computing Systems in Data Centers

First, we give an overview of the trends in computing systems mainly used in data centers, and point out requirements led by these trends. In the application layer, the most significant trend is data explosion. According to a report from IBM, 90 % of data in the world was created in the last 2 years alone [1]. This is a simple and impressive fact to understand the speed of the recent data explosion. The data explosion speed is expected to become faster due to the penetration of data analytics using "big data" and Internet of Things (IoT), because these applications will

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handle much bigger data sets than conventional web-searching or video-casting. Data centers are facing serious challenges to catch up with this data explosion. These trends are encouraging a shift to data-centric computing in data centers.

In the system layer, we believe that "disaggregation" of computing resources such as processors, memories, storages, and networks to make the system more flexible, scalable, and efficient is a notable new trend, as well as data-centric computing [2]. These trends require wider bandwidth and longer reach for interconnects between devices. The appearance of mega data centers also requires longer reach interconnects.

In the device/module layer, we point out three trends. First, although transistor size is still shrinking based on Moore's law, its clock frequency has already hit the ceiling [3]. This trend is consequently requiring enhanced performance from many-core processors (MCPs) by means of parallelism. As a result, data quantity handling within a processor die is still growing. The second trend is three-dimensional (3-D) packaging, which has been mainly introduced for stacked memory modules such as Wide I/O 2 [4], high bandwidth memory (HBM) [5], and hybrid memory cube (HMC) [6], and successfully provides large capacity and wide bandwidth for inter-die (intra-module) interconnects by using through-silicon vias (TSVs). The 3-D packaging can be also applied to increase the capacity of non-volatile memory such as flash memory used as a solid-state drive (SSD), for data storage. As a result, data quantity handling within a memory module is also increasing. The third trend is system in a package (SiP) or multi-chip module (MCM), which consists of multiple chips in a single package and provides multiple functions with higher flexibility and shorter developing time than system on a chip (SoC). Generally, SiP can be implemented by 2.5-D packaging, where some bare dice are stacked vertically and some single chips or stacked dice are mounted side-by-side on an interposer. All of these three trends also require wider bandwidth for inter-chip interconnects.

1.1.2 Problems with Electrical Interconnects

Although wider bandwidth for inter-chip interconnects is required from application, system and device/module layers, the bandwidth of conventional inter-chip interconnects with electric wires is limited due to their low channel line rate and low input/output (I/O) pin density, namely low bandwidth density. For example, we estimate the required inter-chip bandwidth will be several tens of Tbps in the late 2010s, while LSI I/O pad pitches, such as flip-chip pad pitches, are expected to remain large at around 100 μm [7]. This is why the required line rate for inter-chip interconnects is estimated to exceed 40 Gbps by the late 2010s, and there are currently no known solutions to achieve the line rate with electrical interconnects on a printed circuit board (PCB) [7]. The reach of electric wires with a high channel line rate is also limited due to their high transmission loss on the PCB and reflections at connectors.

1.1.3 Optical Interconnects with Silicon Photonics

Optical interconnects with silicon photonics are potential candidates for solving the bandwidth bottleneck and limited reach problem and have been investigated [8–11]. We believe they have three major advantages. The first is the intrinsic properties of optical signals, such as wide bandwidth, low latency, low power consumption, and low mutual interference, compared with those of electrical signals. The second is the industrial advantages of silicon with which we can share the huge amount of existing resources in the electronics industry in terms of design, fabrication, testing, and supply chain. For example, we can use electronic design automation (EDA) tools and foundry services with 300-mm wafers for silicon photonics as with electronics. The common platforms between photonics and electronics also lead to high adaptability to photonics–electronics convergence. The third is the compactness due to their optical waveguides (OWs) with high refractive index contrast. The device compactness also leads to high performance in terms of speed and power consumption.

1.1.4 Vision for on-Chip Servers

Based on the examination of the above-mentioned trends, requirements, and problems of computing systems in data centers, we have propose a concept of an on-chip server in which the functions and performance of a present on-board server will be integrated on a substrate in the 2020s, as shown in Fig. 1.1 [12]. It is a kind of SiP or MCM. A 3-D MCP, 3-D memory (3-D Mem), and 3-D SSD are integrated on an interposer. While the vertical interconnects between stacked dice are electrical through TSV, horizontal interconnects between modules that consist of the stacked dice are mainly optical with silicon photonics. We call this system the photonics–electronics convergence system. More details are given in the following sections.

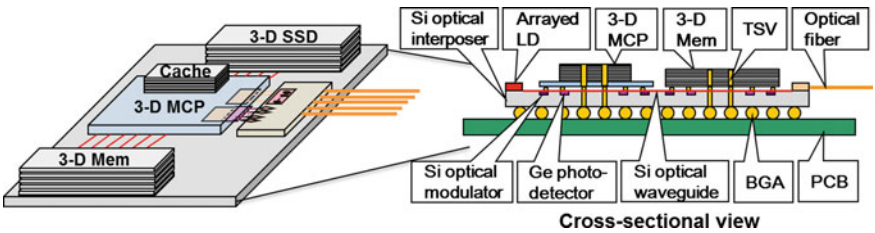

Fig. 1.1 On-chip servers based on silicon optical interposers

1.1.5 Photonics-Electronics Convergence System Technology (PECST) Project

To develop interconnects for future on-chip servers in Japan, the Photonics-Electronics Convergence System Technology (PECST) project was started in March 2010 as one of the 30 Funding Programs for the World-Leading Innovative R&D on Science and Technology (FIRST) projects supported by the Council for Science and Technology Policy in the Cabinet Office. This project was carried out for 4 years, mainly involving the University of Tokyo, Photonics Electronics Technology Research Association (PETRA), and Advanced Industrial Science and Technology (AIST). The PECST aimed to establish chip-to-chip interconnect technologies with a bandwidth density of 10 Tbps/cm^2. This chapter mainly describes the vision, methods, and achievements of the PECST project.

In Sect. 1.2 of this chapter, we first introduce our proposed photonics–electronics convergence system based on silicon optical interposers and in Sect. 1.3, we explain the configuration and characteristics of optical components for silicon optical interposers. Then, we discuss the evaluation of these optical interposers for high bandwidth density and wide temperature range operation in Sects. 1.4 and 1.5. Furthermore, we discuss the 25-Gbps data links using silicon optical interposers in Sect. 1.6 and the advanced fabrication and optical components for wider bandwidth in Sect. 1.7. Finally, we provide a perspective on inter-chip interconnects in Sect. 1.8 and conclude the chapter in Sect. 1.9.

1.2 Photonics–Electronics Convergence System for Inter-chip Interconnects

1.2.1 Optical Interconnects for Short Reach

Figure 1.2 shows the building blocks of optical interconnects, which consist of a light source, light distributor, electrical-to-optical (E/O) signal converter, optical wire, optical to electrical (O/E) signal converter, transmitter (Tx) circuits, and receiver (Rx) circuits. The photos in the figure show our optical components for examples of an arrayed laser diode (LD), silicon optical splitter (OS), silicon optical modulator (OM), silicon OW, and germanium photodetector (PD). With this system, light is not modulated directly by the light source, so the light source is not required to have high-speed operation but high output power is required for multichannel distribution. To build the integrated optical interconnects, we have to examine two integration methods, photonics–electronics integration and light source integration.

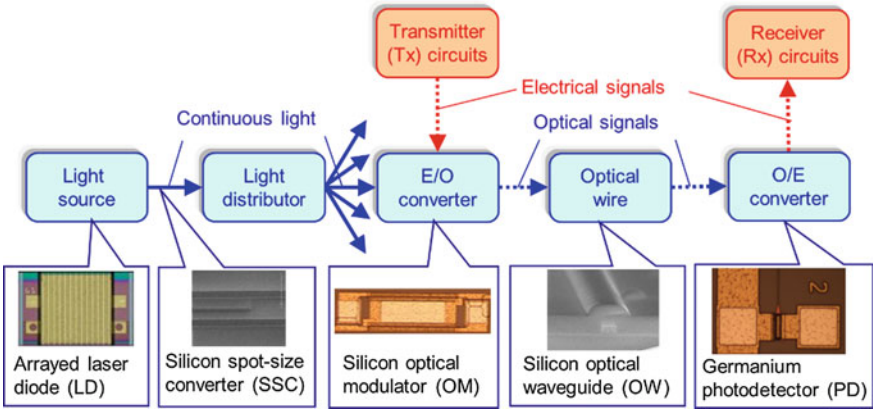

Fig. 1.2 Building blocks of optical interconnects

1.2.2 Integration Between Photonics and Electronics

Because the performance of electrical interconnects generally declines more rapidly with their distance than does that of optical interconnects, it is important to place optical transceivers (E/O and O/E signal converters) as close to large-scale integration (LSI) chips as possible for wide-bandwidth inter-chip interconnects with photonic wiring. Silicon photonics is the most suitable technology for these applications because of its compactness and compatibility with LSIs.

Generally, there are three types of integration methods between photonic and electronic circuits with silicon photonics. Their schematic cross sections are shown in Fig. 1.3: front-end integration, back-end integration, and flip-chip bonding. In front-end integration, both electronic and photonic circuits are integrated near the surface of a silicon substrate by a front-end process. In back-end integration, photonic circuits are integrated on the wiring layer by a back-end process. In flip-chip bonding, electronic and photonic chips are fabricated separately then stacked by flip-chip bonding. The first two are monolithic integrations and the last is a hybrid integration. The characteristics of these integrations are compared in Table 1.1. Monolithic integration, especially front-end integration, is expected to provide higher speed and lower assembling cost than hybrid integration, but it requires very strict CMOS compatibilities in terms of design, fabrication, and testing. We believe that it will be a long time before the technology is mature enough. In contrast, hybrid integration enables us to individually choose the most suitable technology nodes for photonic and electronic circuits, to design, fabricate and test them separately, and then combine their good dies. This scheme can improve product yields and stimulate horizontal specialization between electronics and photonics or between LSI chips and their inter-chip interconnects. Therefore,

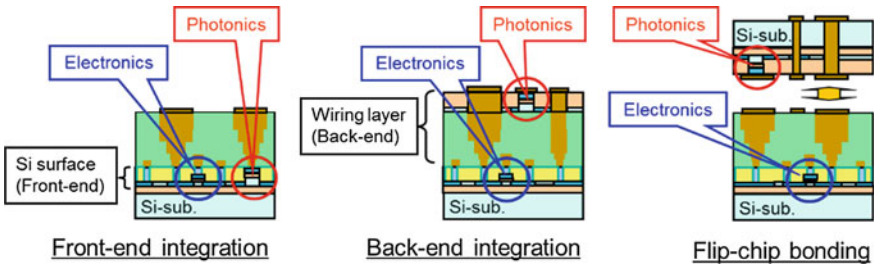

Fig. 1.3 Schematic cross sections of integration between photonic and electronic circuits

Table 1.1 Comparison of photonics–electronics integration methods

Integration type	Monolithic		Hybrid
	Front-end integration	Back-end integration	Flip-chip bonding
Operation speed	Higher	Lower	Lower
Assembly cost	Lower	Lower	Higher
Wafer process cost	Higher	Intermediate	Lower
Challenge for integration	Harder	Harder	Easier
Available waveguide	SOI, bulk-Si	SiN, a-Si	SOI

since we believe that hybrid integration is the most practical choice both now and in the near future, we have taken the hybrid-integration route to photonic–electronic integration for inter-chip interconnects.

1.2.3 Light Source Integration

Generally, light sources for high-density inter-chip interconnects are classified, as shown in Fig. 1.4. First, when considering the light source arrangement in our inter-chip optical interconnects, we have to choose between off-chip or on-chip sources. Although off-chip light sources are the more flexible of the two, they require highly precise optical connectors and care regarding polarization dependence to deliver optical power from the off-chip light sources into the substrate via optical fibers. Because we believe that this is not practical for large-scale interconnects, we chose on-chip light sources, which require neither optical connecters nor special care regarding polarization dependence. Although on-chip light sources are often affected by heat generated by LSIs mounted near the light sources, we

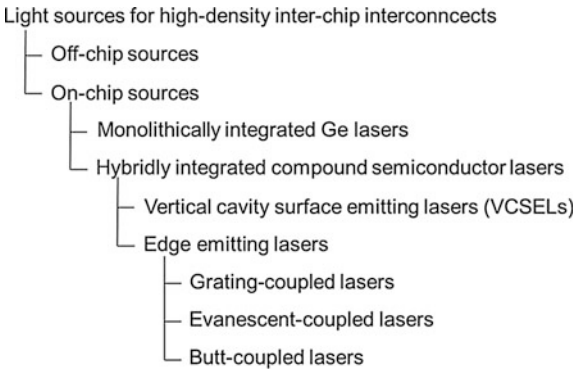

Fig. 1.4 Classification of light sources for high-density inter-chip interconnects

introduce a solution for this problem, as mentioned in Sect. 1.5. There are two types of integration for on-chip light sources: monolithic integration with germanium lasers and hybrid integration with compound semiconductor lasers. Because the efficiency and output power of monolithically integrated Ge-on-Si lasers are still low for inter-chip interconnect applications [13], we chose hybridly integrated lasers. There are two types of compound semiconductor lasers for optical interconnects: edge-emitting lasers and vertical cavity surface emitting lasers (VCSELs). Because VCSELs cannot maintain single-mode operation when the optical output is high, we chose edge-emitting lasers. There are also three types of edge-emitting lasers in terms of optical coupling structures between active OWs in the LDs and silicon OWs: grating-coupled lasers [14], evanescent-coupled lasers [15], and butt-coupled lasers [16]. The grating-coupled laser is a subassembly module, in which an LD, ball-lens, isolator, and 45° mirror are packaged in a hermetic silicon housing [14]. Although this method is highly reliable and tolerant of optical feedback, the module is much bigger than bare LD chips in the following methods. It is difficult to apply an arrayed LD chip for scale-out. The evanescent-coupled lasers have higher tolerance against alignment error when the compound semiconductor chips are mounted on the silicon substrate than the butt-coupled lasers do. However, we found that the bandwidth density and power consumption per channel in LDs can be improved using a branching configuration, in which the light from a single LD is divided and distributed to many channels [17], and we believe the efficiency and output optical power of the evanescent-coupled lasers are not high enough for the branching configuration. We therefore chose to use butt-coupled hybrid lasers for inter-chip interconnect applications and developed spot-size converters (SSCs) between LDs and silicon OWs to relax the alignment tolerance, as mentioned later.