Superior-Order Curvature-Correction Techniques for Voltage References

Cosmin Radu Popa

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Cosmin Radu Popa
Faculty of Electronics, Telecommunication and Information Technology
Department of Devices, Circuits and Electronic Apparatus
University Politehnica of Bucharest
Bucharest, Romania
cosmin_popa@yahoo.com

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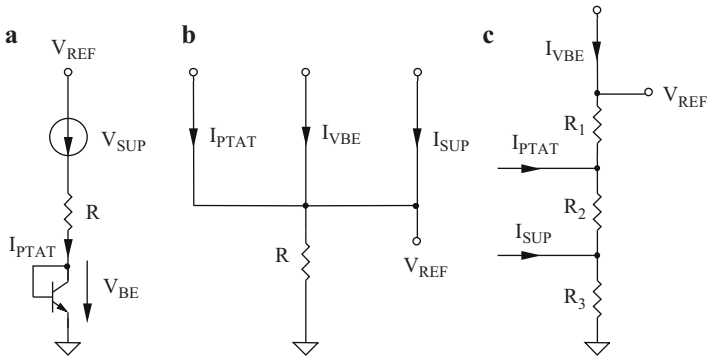
This book is dedicated to the memory of my Grandfather

Preface

Voltage references represent important VLSI structures, having multiple applications in analog and mixed-signal circuits: measurement equipment, voltage regulators, temperature sensors, data acquisition systems, memories, or AD and DA converters. Operating as a subcircuit in a complex system, an important requirement for this class of circuits is represented by the possibility of implementation in the existing technology, using the available active and passive devices.

The most important performances of a voltage reference circuit are represented by temperature behavior, power supply rejection ratio, transient response and, for the latest designs, by low-power low-voltage operation. Depending on the load requirements, the output of the circuit can be regulated or unregulated. In order to reduce the sensitivity of the reference voltage with respect to the supply voltage variations, modified cascode structures can be implemented, a trade-off between line regulation and low-voltage operation being necessary in this case. A large bandwidth of the voltage reference improves the transient behavior of the circuit, implying also a good noise rejection.

Referring to the possibilities of implementing a voltage reference circuit, two different approaches could be identified: voltage-mode and current-mode topologies, being also possible to design a mixed-mode voltage reference.



Most voltage references are based on voltage-mode architecture (a), the PTAT (proportional to absolute temperature) voltage across resistor R compensating the linear dependence on temperature term from $V_{BE}(T)$, while $V_{SUP}(T)$ voltage contains nonlinear terms, complementary to the nonlinear components of $V_{BE}(T)$. The most important disadvantage of the voltage-mode voltage references is that the minimal reference voltage is about 1.2 V (the silicon bandgap energy), so these architectures are not suitable for very low-voltage applications. In order to obtain reference voltages inferior to the value of 1.2 V, a current-mode design (b) can be used. The compensation of the reference voltage temperature dependence is obtained by summing three currents with different temperature dependencies: a base–emitter derived current I_{VBE}, a PTAT current I_{PTAT}, and a superior-order correction current I_{SUP}, the sum current passing through the resistor R. As the reference voltage depends on the ratio of resistors, their temperature coefficient does not strongly affect the overall performance of the circuit, only superior-order terms being slightly influenced by the resistor temperature dependence. The benefits of both voltage-mode and current-mode designs could be obtained using a mixed-mode topology (c) of the voltage reference. The current-mode approach decreases the value of reference voltage, while the voltage-mode topology offers better possibilities for temperature compensation.

The complexity of voltage references is correlated with the quality of temperature behavior required by the circuits that use the reference voltage. Relating to the possibility of reducing the temperature dependence of voltage references, three important classes of circuits could be identified: zero-order curvature-corrected structures, first-order curvature-corrected voltage references, and superior-order curvature-corrected circuits.

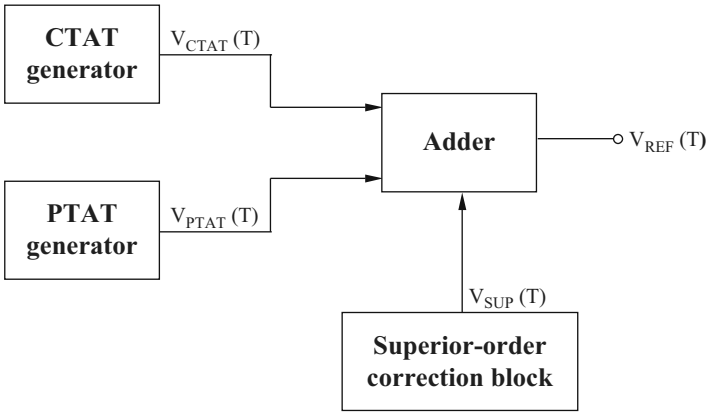
The zero-order curvature-corrected voltage references show the advantage of simplicity, the obtained performances being relatively poor. Concerning the temperature dependence of the reference voltage, these circuits could be classified in PTAT voltage references, showing a linear positive temperature variation and CTAT (complementary to absolute temperature) voltage references, with approximately linear negative temperature dependence. The concrete implementation of a CTAT circuit, which represents the core of a voltage reference, is based on the base–emitter voltage, gate–source voltage for a subthreshold-operated MOS transistor, or on the threshold voltage. Three terms in the temperature dependence of a CTAT voltage could be identified: a constant term V_{CT}, a linear dependence on temperature term $V_{LIN}(T)$, and a term having a nonlinear temperature dependence, $V_{NL}(T)$, usually proportional with $T \ln T$:

$$
\begin{aligned}
&V_{PTAT}(T) = AT,\ A > 0,\\
&V_{CTAT}(T) = V_{CT} + V_{LIN}(T) + V_{NL}(T),\\
&V_{CTAT}(T) = B + CT + DT \ln T, \quad B > 0, \quad C < 0.
\end{aligned}
$$

The improvement of temperature behavior of voltage references imposes the implementation of curvature-correction techniques. The fundamental correction

principle is based on summing with CTAT voltage of two correction voltages, having temperature variations that are complementary with $V_{\mathrm{LIN}}(T)$ and $V_{\mathrm{NL}}(T)$ from the $V_{\mathrm{CTAT}}(T)$ expression:

$$V_{\mathrm{REF}}(T) = V_{\mathrm{CTAT}}(T) + V_{\mathrm{PTAT}}(T) + V_{\mathrm{SUP}}(T).$$



Supposing an accurate implementation of these correction voltages ($\alpha_{V_{\mathrm{LIN}}} = -\alpha_{V_{\mathrm{PTAT}}}$, $\alpha_{V_{\mathrm{NL}}} = -\alpha_{V_{\mathrm{SUP}}}$), the resultant reference voltage will have a theoretically null temperature coefficient. The first-order curvature-correction of the reference voltage temperature dependence supposes the mutual compensation of $V_{\mathrm{LIN}}(T)$ and $V_{\mathrm{PTAT}}(T)$ voltages, while the superior-order curvature-correction imposes, additionally, the compensation of $V_{\mathrm{NL}}(T)$ and $V_{\mathrm{SUP}}(T)$ terms. Presenting the advantage of a medium complexity, the performances of first-order curvature-corrected voltage references are better than the performances of zero-order curvature-corrected circuits, but still poor for high-precision applications. The increased complexity of superior-order curvature-corrected voltage references is compensated by the possibility of achieving a very good temperature behavior of the circuit.

The necessity of implementation CTAT and first-order/superior-order correction voltages imposes the necessity of obtaining currents having well-known and controllable temperature dependencies, useful for biasing the blocks from the voltage reference circuits.

The fundamental methods for designing voltage references are adapted to the implementation of these circuits in bipolar and CMOS technology, with the advantages and limitations associated with each technology. The first-order analysis is followed by the study of errors introduced by the second-order effects that affect the active devices' operation. The weak inversion biasing of MOS transistors allows obtaining a low-power operation of circuits designed in CMOS technology, while the current-mode operation and specific design techniques assure a low-voltage operation of

voltage references. The improvement of the power supply rejection ratio of designed circuits is achieved by proposing simple and cascode self-biasing methods for the elementary structures.

The first chapter reviews the basic principles for designing current references, required for biasing the main blocks of voltage references. CTAT, PTAT, PTAT^2, and PTAT^n current references, as well as first-order curvature-corrected current references, are analyzed.

Zero-order curvature-corrected voltage references are analyzed in Chap. 2, the relatively poor performances being compensated by the reduced complexity of this class of circuits. CTAT and PTAT voltage references are studied, with elementary voltages as V_{BE}, V_{GS}, V_T, or their linear combinations being used for implementing zero-order curvature-corrected structures.

The improvement of temperature behavior of voltage references will be studied in Chap. 3 by analyzing the first-order curvature-corrected circuits. Usual methods for designing these circuits include the compensation, using a PTAT voltage, of the base–emitter, gate–source, or threshold voltage temperature dependencies, as well as the mutual compensation of the carriers' mobility and threshold voltage temperature dependencies.

The implementation of high-performance voltage references is possible by designing superior-order curvature-correction techniques. The study of high-precision voltage references will be the goal of Chap. 4. The fundamental design principles of these circuits for the bipolar technology will refer to the correction of the nonlinear temperature dependence of base–emitter voltage using a proper biasing of bipolar transistor and to the compensation of the nonlinear temperature dependence of base–emitter voltage using a correction current or a correction voltage. For voltage references implemented in CMOS technology, the methods for obtaining high-accuracy circuits are referring to the correction of the nonlinear temperature dependence of gate–source voltage using a proper biasing of the MOS transistor or to the compensation of the nonlinear temperature dependence of gate–source voltage using a correction current or a correction voltage. Improved performance programmable voltage references are also presented, allowing to obtain a digitally selected type of the superior-order curvature-correction technique, adapted to the technology in which the circuit is implemented.

Degradation of the overall behavior of voltage references produced by multiple sources of errors that affect the circuit operation (mismatches, components' tolerances, offsets, resistor temperature variation, second-order effects, supply voltage variations, package-shift effects, and layout errors) is quantitatively evaluated in Chap. 5, showing the importance of each error in the decreasing of voltage references' performances.

Taking into account that voltage references represent very important VLSI structures, with a lot of applications in various theoretical and practical approaches, every step ahead constitutes an interesting and useful matter.

Bucharest, Romania Cosmin Radu Popa

Contents

Chapter 1
Current References

Abstract Current references represent important building blocks in bipolar and CMOS designs. They usually act as biasing structures that deserve other applications, but, sometimes, they can be used as independent circuits. The most used, PTAT (proportional to absolute temperature) current references represent essential blocks in a voltage reference, required for compensating the negative decrease with temperature term from base–emitter, gate–source, or threshold voltages or for biasing the active device from the voltage reference core. CTAT (complementary to absolute temperature) current references have an approximately negative linear decrease on temperature variation, a design that fulfills the complementary of PTAT and CTAT currents presenting an improved temperature behavior. PTAT^2 and PTAT^n currents represent the basis of implementing superior-order curvature-correction techniques in order to obtain an extremely low temperature coefficient of the voltage reference.

The necessity of current references and the analysis of their temperature dependence represent a consequence of a large area of applications that impose the biasing of different blocks at a current having a controllable temperature dependence. Because the accuracy of current references is, usually, inferior to the accuracy of voltage references, the current references are used, in most cases, as internal biasing blocks, not as independent structures.

Taking into account the temperature dependence of the output current, the current references could be classified as follows:

- PTAT (proportional to absolute temperature), current references, having an approximately linear positive temperature dependence, $I_{\text{PTAT}}(T) = AT, A > 0$
- CTAT (complementary to absolute temperature) current references, with an approximately linear negative temperature dependence, $I_{\text{CTAT}}(T) = I_{\text{CT}} + I_{\text{LIN}}(T) + I_{\text{NL}}(T)$; I_{CT} represents a constant term with respect to temperature variations, $I_{\text{LIN}}(T) = BT, B < 0$ presents a linear negative temperature dependence, while $I_{\text{NL}}(T)$ is a complex function on temperature, usually proportional with $T \ln T$
- First-order curvature-corrected current references, presenting a relatively small temperature dependence

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- PTAT^2 and PTAT^n current references, useful for implementing second-order and superior-order curvature-correction techniques for the voltage reference circuits

There are multiple causes of the nonlinear temperature dependence of PTAT and CTAT current references:

- Intrinsic nonlinear temperature dependence of base–emitter voltage, gate–source voltage (for a MOS transistor biased in weak inversion region), or threshold voltage
- Temperature dependence of used resistors
- Second-order effects that affect the operation of active devices
- Finite value of the current gain of bipolar transistors and its temperature dependence

The improvement of power supply rejection ratio can be realized by self-biasing the current source. An additional improvement of power supply rejection is possible by using a cascode current source for implementing the self-biasing, in hypothesis of the existing relatively large supply voltage. Quantitative evaluation of the dependence of output current on supply voltage is made by using the sensitivity of output current with respect to supply voltage variations, $S_{I_O}^{V_{DD}}$, defined as the ratio between the relative variation of output current and the relative variation of supply voltage:

$$S_{I_O}^{V_{DD}} = \frac{dI_O/I_O}{dV_{DD}/V_{DD}} = \frac{V_{DD}}{I_O}\frac{dI_O}{dV_{DD}}. \tag{1.1}$$

1.1 PTAT Current References

Most voltage references impose the biasing of some of their composing transistors at a current having a linear positive temperature dependence (PTAT), usually for implementing the linear correction term, $V_{PTAT}(T)$. In bipolar technology, the design method is based on the difference between two base–emitter voltages of bipolar transistors biased at different current densities. The alternative of implementing in CMOS technology of PTAT current generators supposes the replacing of bipolar transistors with MOS transistors biased in weak inversion region. For a bipolar PTAT current reference, the output current will have the following temperature dependence:

$$I_{PTAT}(T) = \frac{V_{BE1}(T) - V_{BE2}(T)}{R} = \frac{kT}{qR}\ln\left(\frac{I_{C1}}{I_{C2}}\frac{I_{S2}}{I_{S1}}\right) = AT. \tag{1.2}$$

The I_{C1}/I_{C2} ratio is fixed using an additional circuit (usually a current mirror) and it is not dependent on temperature, while the ratio of saturation currents is equal with the ratio of the areas of composing transistors. Imposing that constant A from (1.2) must be positive, the output current will have a PTAT variation. The implementing in CMOS technology of the PTAT generator is similar, resulting in:

$$I_{PTAT}(T) = \frac{V_{GS1}(T) - V_{GS2}(T)}{R} = \frac{nkT}{qR}\ln\left[\frac{I_{D1}}{I_{D2}}\frac{(W/L)_2}{(W/L)_1}\right] = AT. \tag{1.3}$$

1.1.1 Self-Biased PTAT Current Reference Using Bipolar Devices

An usual method of designing in bipolar technology of a PTAT current reference with a small dependence of the output current on the supply voltage variations requires the self-biasing of the circuit (Fig. 1.1) [1].

Considering that the ratio of saturation currents for T_1 and T_2 transistors is $I_{S2}/I_{S1} = n$ and that T_3–T_5 transistors are identical, the expression of the output current is as follows:

$$I_O = \frac{V_{BE1} - V_{BE2}}{R} = \frac{V_{th}}{R} \ln\left(\frac{I_{C1}}{I_{C2}}\frac{I_{S2}}{I_{S1}}\right) = \frac{V_{th}}{R} \ln\left(n\frac{I_{C3}}{I_{C4}}\right). \tag{1.4}$$

The errors caused by Early effect in the operation of T_3–T_4 current mirror are concretized in a ratio of their collector currents expressed by:

$$\frac{I_{C3}}{I_{C4}} = \frac{I_{S3}}{I_{S4}} \frac{1 + \frac{V_{CC} - V_{BE1}}{V_A}}{1 + \frac{V_{EB4}}{V_A}} \cong 1 + \frac{V_{CC}}{V_A}. \tag{1.5}$$

So,

$$I_O = \frac{V_{th}}{R} \ln n + \frac{V_{th}}{R} \ln\left(1 + \frac{V_{CC}}{V_A}\right). \tag{1.6}$$

Because $V_{CC}/V_A \ll 1$, it is possible to use in (1.6) the approximation $\ln(1 + x) \cong x$, for $x \ll 1$, resulting in:

$$I_O = \frac{V_{th}}{R} \ln n + \frac{V_{th}}{R}\frac{V_{CC}}{V_A}. \tag{1.7}$$

Deriving with respect to V_{CC} the previous relation, it results in:

$$S_{I_O}^{V_{CC}} = \frac{V_{CC}}{I_O}\frac{dI_O}{dV_{CC}} \cong \frac{V_{CC}}{V_A}\frac{1}{\ln n}, \tag{1.8}$$

so, a relatively small value of $S_{I_O}^{V_{CC}}$, consequence of self-biasing of the circuit.

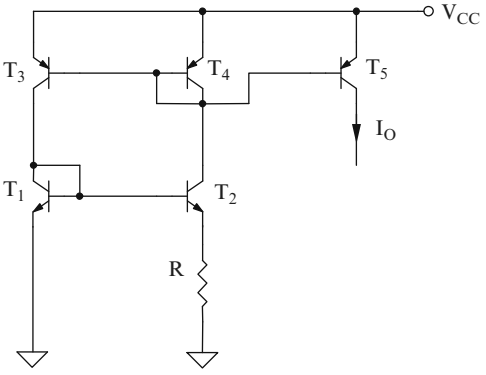

Fig. 1.1 Self-biased bipolar PTAT current reference ([1]; reproduced with permission of Wiley)

1.1.2 Self-Biased PTAT Current Reference Using MOS Devices

Self-biasing of the current reference T_1–T_2 from Fig. 1.2 [2] using the T_3–T_4 current mirror allows the improvement of power supply rejection ratio, quantitatively evaluated by the sensitivity of output current on supply voltage variations, $S_{I_O}^{V_{DD}}$. All MOS transistors are biased in weak inversion; T_3 and T_4 are identical, while T_1 and T_2 have different aspect ratios.

Disregarding the channel-length modulation effect, the output current can be expressed as follows:

$$I_O = \frac{V_{GS1} - V_{GS2}}{R} = \frac{nV_{th}}{R} \ln\left[\frac{I_{D1}}{I_{D2}}\frac{(W/L)_2}{(W/L)_1}\right] = \frac{nV_{th}}{R} \ln\left[\frac{(W/L)_2}{(W/L)_1}\right]. \quad (1.9)$$

Considering, additionally, the errors introduced by the channel-length modulation, the output current expression becomes as follows:

$$I_O \cong \frac{nV_{th}}{R} \ln\left[\frac{(W/L)_2}{(W/L)_1}\right] + \frac{nV_{th}}{R} \ln\left[1 + \lambda(V_{DD} - 2V_{GS})\right]. \quad (1.10)$$

Because $\lambda(V_{DD}-2V_{GS}) \ll 1$, in (1.10) it is possible to use the approximation $\ln(1 + x) \cong x$, for $x \ll 1$, resulting in:

$$I_O \cong \frac{nV_{th}}{R} \ln\left[\frac{(W/L)_2}{(W/L)_1}\right] + \lambda\frac{nV_{th}}{R}(V_{DD} - 2V_{GS}). \quad (1.11)$$

Deriving with respect to V_{DD} the previous relation, it results in:

$$S_{I_O}^{V_{DD}} \cong \frac{\lambda V_{DD}}{\ln\left[\frac{(W/L)_2}{(W/L)_1}\right]}, \quad (1.12)$$

so, a relatively small value of $S_{I_O}^{V_{DD}}$, consequence of self-biasing of the circuit.

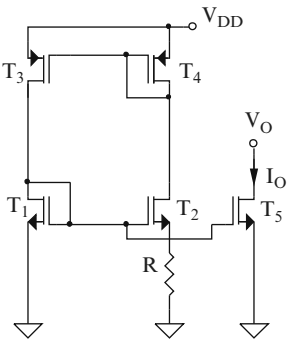

Fig. 1.2 Self-biased CMOS PTAT current reference ([2]; © [2008] IEEE)

1.1.3 Cross-Connection PTAT Bipolar Current Reference

The current reference presented in Fig. 1.3 uses a cross-connection for further improvement of the power supply rejection, this technique being able to compensate the errors introduced by Early effect that affect the bipolar devices' operation. The expression of the output current is as follows:

$$I_O = \frac{V_{BE4} + V_{BE5} - V_{BE3} - V_{BE6}}{R_1} = \frac{V_{th}}{R_1} \ln\left(\frac{I_{C4} I_{C5}}{I_{C3} I_{C6}} \frac{I_{S3} I_{S6}}{I_{S4} I_{S5}}\right). \tag{1.13}$$

Because $I_{C3} = I_{C5}$ and $I_{C4} = I_{C6}$, it results in:

$$I_O = \frac{V_{th}}{R_1} \ln\left(\frac{I_{S3} I_{S6}}{I_{S4} I_{S5}}\right). \tag{1.14}$$

Imposing the design condition $I_{S3} I_{S6} / I_{S4} I_{S5} > 1$, it is possible to obtain a PTAT variation of the output current.

1.1.4 Cross-Connection PTAT CMOS Current Reference

The current reference presented in Fig. 1.4 generates a PTAT output current using T_3–T_6 transistors biased in weak inversion region and T_1–T_2 current mirror for self-biasing the circuit.

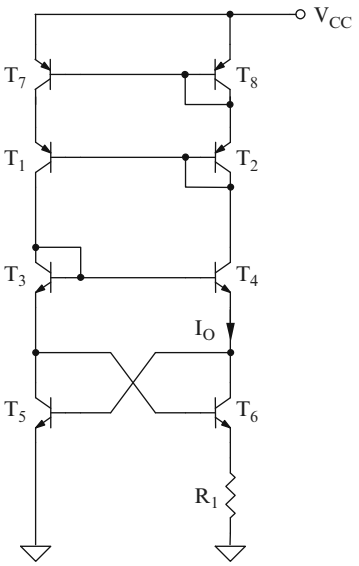

Fig. 1.3 Cross-connection PTAT bipolar current reference

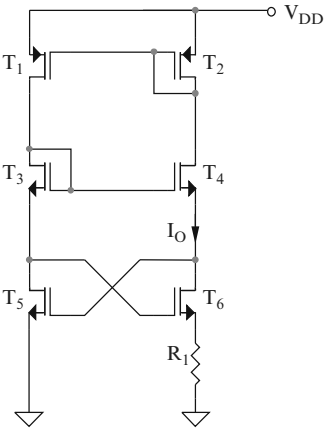

Fig. 1.4 Cross-connection PTAT CMOS current reference

The weak inversion operation of MOS devices is characterized by a logarithmical dependence of the gate–source voltage on drain current:

$$V_{GS} = V_T + nV_{th} \ln\left[\frac{I_D}{I_{D0}\,(W/L)}\right]. \tag{1.15}$$

It results in:

$$\begin{aligned} I_O &= \frac{V_{GS4} + V_{GS5} - V_{GS3} - V_{GS6}}{R_1} \\ &= \frac{nV_{th}}{R_1} \ln\left[\frac{I_{D4}I_{D5}}{I_{D3}I_{D6}} \frac{(W/L)_3(W/L)_6}{(W/L)_4(W/L)_5}\right]. \end{aligned} \tag{1.16}$$

Because $I_{D3} = I_{D5}$ and $I_{D4} = I_{D6}$, the output current expression could be written as follows:

$$I_O = \frac{nV_{th}}{R_1} \ln\left[\frac{(W/L)_3(W/L)_6}{(W/L)_4(W/L)_5}\right]. \tag{1.17}$$

Imposing by design $(W/L)_3(W/L)_6 > (W/L)_4(W/L)_5$, the output current will have a PTAT variation. Additionally, the cross-connection compensates the errors introduced by the channel-length modulation that affect the MOS transistors' operation.

1.1.5 Self-Biased PTAT Current Reference Using Parasite Bipolar Transistors

The current source proposed in Fig. 1.5 [1] generates a PTAT current using the difference between two emitter–base voltages (V_{EB1} and V_{EB7}) of transistors biased at different current densities, the self-biasing being implemented by the T_4–T_5 current mirror.

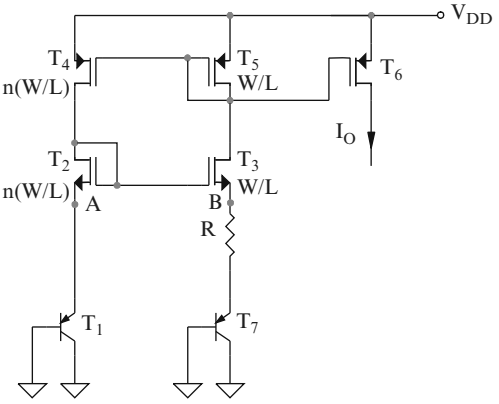

Fig. 1.5 Self-biased PTAT current reference using parasite bipolar transistors ([1]; © 1993 John Wiley & Sons, Inc. Reproduced with permission of Wiley)

The possibility of implementing a PTAT current reference imposes as design restriction the identity between V_A and V_B potentials, in such a way that the voltage across R resistor is the difference between two base–emitter voltages. The differential voltage $V_A - V_B$ has the following expression:

$$V_A - V_B = V_{GS3} - V_{GS2} = \left(V_T + \sqrt{\frac{2I_{D3}}{K_3}}\right) - \left(V_T + \sqrt{\frac{2I_{D2}}{K_2}}\right), \tag{1.18}$$

equivalent with:

$$V_A - V_B = \sqrt{\frac{2I_{D3}}{K_3}}\left[1 - \sqrt{\frac{I_{D2}}{I_{D3}}\frac{(W/L)_3}{(W/L)_2}}\right]. \tag{1.19}$$

Because $I_{D2}/I_{D3} = I_{D4}/I_{D5} = (W/L)_4/(W/L)_5$, it results in:

$$V_A - V_B = \sqrt{\frac{2I_{D3}}{K_3}}\left[1 - \sqrt{\frac{(W/L)_4}{(W/L)_5}\frac{(W/L)_3}{(W/L)_2}}\right]. \tag{1.20}$$

Thus, the design restriction that $V_A = V_B$ equality imposes $(W/L)_2\,(W/L)_5 = (W/L)_3\,(W/L)_4$, with the expression of output current as follows (in the hypothesis of disregarding the channel-length modulation effect):

$$I_O = \frac{|V_{BE1}| - |V_{BE7}|}{R} = \frac{V_{th}}{R}\ln\left(\frac{I_{C1}}{I_{C7}}\frac{I_{S7}}{I_{S1}}\right) = \frac{V_{th}}{R}\ln\left(n\frac{I_{S7}}{I_{S1}}\right). \tag{1.21}$$

Considering, additionally, the errors introduced by this second-order effect, the output current will be expressed as follows:

$$I_O = \frac{V_{th}}{R_1}\ln\left[n\frac{I_{S7}}{I_{S1}}\frac{1 + \lambda\,(V_{DD} - V_{EB1} - V_{GS2})}{1 + \lambda V_{SG5}}\right]. \tag{1.22}$$

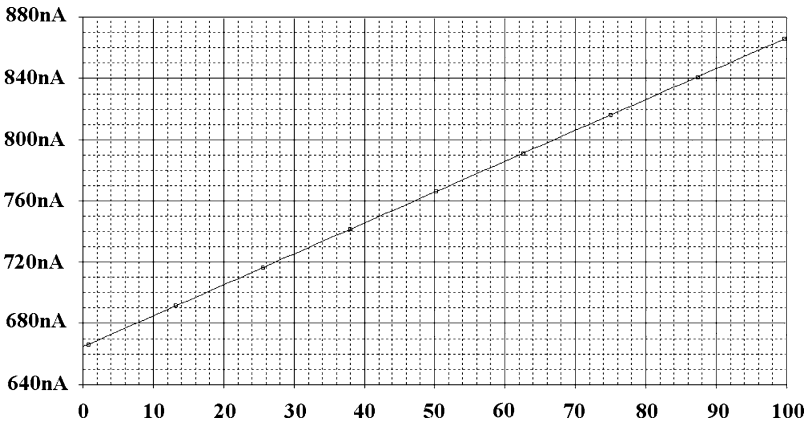

Fig. 1.6 The $I_O(T)$ simulation for the circuit from Fig. 1.5

Deriving, the expression of the sensitivity of output current with respect to the supply voltage variations, $S_{I_O}^{V_{DD}}$, will be as follows:

$$S_{I_O}^{V_{DD}} \cong \frac{\lambda V_{DD}}{\ln\left(nI_{S7}/I_{S1}\right)}. \tag{1.23}$$

Example. Choosing $R = 100\,k\Omega$, the ratio of saturation currents for bipolar transistors $I_{S7}/I_{S1} = 10$, and equal aspect ratios for the MOS transistors ($n = 1$), the temperature coefficient of the output current I_O will be as follows:

$$\frac{dI_O}{dT} = \frac{k}{qR}\ln\left(\frac{I_{S7}}{I_{S1}}\right) = 2nA/K. \tag{1.24}$$

The $I_O(T)$ simulation is presented in Fig. 1.6, showing a temperature coefficient equal with:

$$\frac{dI_O}{dT} = 2.015nA/K. \tag{1.25}$$

1.2 CTAT Current References

Complementary to the PTAT current references from the point of view of temperature variation, the CTAT current references show approximately linear negative temperature dependence. The linearity of this dependence is correlated with the principle of implementing the CTAT reference. Depending on the technology, the following designing methods of these current references can be identified: