Reviews of Nonlinear Dynamics and Complexity

Volume 3

Edited by
Heinz Georg Schuster

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Contents

Preface

Following the appearance of the first two very successful volumes of **Reviews of Nonlinear Dynamics and Complexity**, it is now my pleasure to introduce the third volume, beginning with an outline of the aims and purpose of this new series.

Nonlinear behavior is ubiquitous in nature and ranges from fluid dynamics, via neural and cell dynamics, to the dynamics of financial markets. The most prominent feature of nonlinear systems is that small external disturbances can induce large changes in behavior. This can and has been used for effective feedback control in many systems, from lasers to chemical reactions and the control of nerve cells and heartbeats. A new hot topic involves nonlinear effects that appear on the nanoscale. Nonlinear control of the atomic force microscope has improved its accuracy by orders of magnitude. The nonlinear electromechanical oscillations of nano-tubes, the turbulence and mixing of fluids in nano-arrays and the nonlinear effects in quantum dots are further examples.

Complex systems consist of large networks of coupled nonlinear devices. The observation that scale-free networks describe the behavior of the internet, cell metabolisms, financial markets and economic and ecological systems, has led to new discoveries concerning their behavior, such as damage control, optimal spread of information, or the detection of new functional modules that are pivotal for their description and control.

This shows that the field of **Nonlinear Dynamics and Complexity** consists of a large body of theoretical and experimental work with many applications, which is nevertheless governed and held together by some very basic principles, such as control, networks and optimization. The individual topics are definitely interdisciplinary, which makes it difficult for researchers to discover the new solutions – which

could be most relevant for them – that have been found by their scientific neighbors. Therefore, its seems that there is an urgent need to provide **Reviews of Nonlinear Dynamics and Complexity** where researchers or newcomers to the field can find the most important recent results, described in a fashion which breaks down the barriers between the disciplines.

This third volume contains new topics ranging from chaotic computing, via random dice tossing and stochastic limit-cycle oscillators, to a number theoretic example of self-organized criticality, wave localization in complex networks and anomalous diffusion. I would like to thank all the authors for their excellent contributions. If readers take some inspiration for their further research from these interdisciplinary reviews, then this volume will have fully served its purpose.

I am grateful to all members of the Editorial Board, and the staff of Wiley-VCH, for their excellent help, and would like to invite my colleagues to contribute to the next volumes.

Kiel, January 2010 *Heinz Georg Schuster*

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The Chaos Computing Paradigm

William L. Ditto, Abraham Miliotis, K. Murali, and Sudeshna Sinha

1.1
Brief History of Computers

The timeline of the history of computing machines can probably be traced back to early calculation aids, varying in sophistication from pebbles or notches carved in sticks to the abacus, which was used as early as 500 B.C.! Throughout the centuries computing machines became more powerful, progressing from Napier's Bones and the slide rule, to mechanical adding machines and on to the modern day computer revolution.

The 'first generation' of modern computers, were based on wired circuits containing vacuum valves and used punched cards as the main storage medium. The next major step in the history of computing was the invention of the transistor, which replaced the inefficient valves with a much smaller and more reliable component. Transistorized (still bulky) computers, normally referred to as 'Second Generation', dominated the late 1950s and early 1960s.

The explosion in the use of computers began with 'Third Generation' computers. These relied on the integrated circuit or microchip. Large-scale integration of circuits led to the development of very small processing units. Fourth generation computers were developed, using a microprocessor to locate much of the computer's processing abilities on a single (small) chip, allowing the computers to be smaller and faster than ever before. Although processing power and storage capacities have increased beyond all recognition since the 1970s the underlying technology of LSI (large-scale integration) or VLSI (very-large-scale integration) microchips has remained basically the same, so it is widely regarded that most of today's computers still belong to the fourth generation.

One common thread in the history of computers, be it the abacus or Charles Babbage's mechanical 'anlytical engine' or modern microprocessors, is this: *computing machines reflect the physics of the time and are driven by progress in the understanding of the physical world*.

1.2 The Conceptualization, Foundations, Design and Implementation of Current Computer Architectures

Computation can be actually defined as finding a solution to a problem from given inputs by means of an algorithm. This is what the theory of computation, a subfield of computer science and mathematics, deals with. For thousands of years computing was done with pen and paper, or chalk and slate, or mentally, sometimes with the aid of tables.

The theory of computation began early in the twentieth century, before modern electronic computers had been invented. One of the far-reaching ideas in the theory is the concept of a Turing machine, which stores characters on an infinitely long tape, with one square at any given time being scanned by a read/write head. Basically, a Turing machine is a device that can read input strings, write output strings and execute a set of stored instructions at a time. The Turing machine demonstrated both the theoretical limits and potential of computing systems and is a cornerstone of modern day digital computers.

The first computers were hardware-programmable. To change the function computed, one had to reconnect the wires or even build a new computer. John von Neumann suggested using Turing's Universal Algorithm. The function computed can then be specified by just giving its description (program) as part of the input rather than by changing the hardware. This was a radical idea which changed the course of computing.

Modern day computers still largely implement binary digital computing which is based on Boolean algebra; the logic of the true and false. Boolean algebra shows how you can calculate anything (within some epistemological limits) with a system of two discrete values. Boolean logic became a fundamental component of modern computer architecture, and is remarkable for its sheer conceptual simplicity. For instance, it can be rigorously shown that any logic gate can be obtained by adequate connection of NOR or NAND gates (i.e. any boolean circuit can be built using NOR/NAND gates alone). This implies that the

capacity for universal computing can simply be demonstrated by the implementation of the fundamental NOR or NAND gates [1].

1.3 Limits of Binary Computers and Alternative Approaches to Computation: What Lies Beyond Moore's Law?

The operation of any computing machine is necessarily a physical process, and this crucially determines the possibilities and limitations of the computing device. For the past 20 years, the throughput of digital computers has increased at an exponential rate. Fuelled by (seemingly endless) improvements in integrated-circuit technology, the exponential growth predicted by Moore's law has held true. But Moore's Law will come to an end as chipmakers will hit a wall when it comes to shrinking the size of transistors, one of the chief methods of making chips that are smaller, more powerful and cheaper than their predecessors.

As conventional chip manufacturing technology runs into physical limits in the density of circuitry and signal speed, which sets limits to binary logic switch scaling, alternatives to semiconductor-based binary digital computers are emerging. Apart from analogue VLSI, these include bio-chips, which are based on materials found in living creatures; optical computers that live on pure light; and quantum computers that depend on the laws of quantum mechanics in order to perform, in theory, tasks that ordinary computers cannot.

Neurobiologically inspired computing, quantum computing and DNA computing differ in many respects, but they are similar in that their aim, unlike conventional digital computers, is to utilize at the basic level some of the computational capabilities inherent in the basic, analogue, laws of physics. Further, understanding of biological systems, has triggered the question: what lessons do the workings of the human mind offer for computationally hard problems? Thus the attempt is to create machines that benefit from the basic laws of physics and which are not just constrained by them.

Here we review another emerging computing paradigm: one which exploits the richness and complexity inherent in nonlinear dynamics. This endeavour also falls into the above class, as it seeks to extend the possibilities of computing machines by utilizing the physics of the device.

1.4 Exploiting Nonlinear Dynamics for Computations

We would now like to paraphrase the classic question 'What limits do the laws of classical physics place on computation' to read 'What opportunities do the laws of physics offer computation'.

It was proposed in 1998 that chaotic systems might be utilized to design computing devices [2]. In the early years the focus was on proof-of-principle schemes that demonstrated the capability of chaotic elements to do universal computing. The distinctive feature of this alternative computing paradigm was that it exploited the sensitivity and pattern formation features of chaotic systems.

In subsequent years there has been much research activity to develop this paradigm [3–17]. It was realized that one of the most promising directions of this computing paradigm was its ability to exploit a single chaotic element to reconfigure into different logic gates through a threshold-based morphing mechanism [3, 4]. In contrast to a conventional field programmable gate array element [18], where reconfiguration is achieved through switching between multiple single-purpose gates, reconfigurable chaotic logic gates (RCLGs) are comprised of chaotic elements that morph (or reconfigure) logic gates through the control of the pattern inherent in their nonlinear element. Two input RCLGs have recently been realized and shown to be capable of reconfiguring between all logic gates in discrete circuits [5–7]. Additionally, such RCLGs have been realized in prototype VLSI circuits (0.13 μm CMOS, 30 MHz clock cycles). Further, reconfigurable chaotic logic gates arrays (RCGA) which morph between higher-order functions such as those found in a typical arithmetic logic unit (ALU), have also been designed [17].

In this review we first recall the theoretical concept underlying the reconfigurable implementation of all fundamental logical operations utilizing nonlinear dynamics [3]. We also describe specific realizations of the theory in chaotic electrical circuits. Then we present recent results of a method for obtaining logic output from a nonlinear system using the time evolution of the state of the system. Finally we discuss a method for storing and processing information by exploiting nonlinear dynamics. We conclude with a brief discussion of some ongoing technological implementations of these ideas.

1.5 General Concept

We outline below a theoretical method for obtaining all basic logic gates with a single nonlinear system. The broad aim here is to use the rich temporal patterns embedded in a nonlinear time series in a controlled manner to obtain a computing device that is flexible and reconfigurable.

Consider a chaotic element (our *chaotic chip* or *chaotic processor*) whose state is represented by a value x. In our scheme all the basic logic gate operations (NAND, NOR, XOR, AND, OR, XNOR and NOT) involve the following steps:

1) Inputs:

   $x \rightarrow x_0 + X_1 + X_2$ for 2-input logic operations, such as the NAND, NOR, XOR, AND, OR and XNOR operations,

   and

   $x \rightarrow x_0 + X$ for 1-input operations, such as the NOT operation.

   Here x_0 is the initial state of the system, and

   $X = 0$ when $I = 0$

   and

   $X = V_{\text{in}}$ when $I = 1$

   where V_{in} is a positive constant.

2) Dynamical update, i.e. $x \rightarrow f(x)$

   where $f(x)$ is a nonlinear function.

3) Threshold mechanism to obtain output Z:

   $Z = 0 \quad \text{if } f(x) \leq E, \quad \text{and}$

   $Z = f(x) - E \quad \text{if } f(x) > E$

   where E is a monitoring threshold.

This is interpreted as logic output 0 if $Z = 0$ and logic ouput 1 if $Z > 0$ (with $Z \sim V_{\text{in}}$).

Since the system is strongly nonlinear, in order to specify the inital x_0 accurately one needs a controlling mechanism. Here we will employ a threshold controller [19,20] to set the inital x_0. Namely, we will use the clipping action of the threshold controller to achieve the initialization and subsequently to obtain the output as well.

Note that in our implementation we demand that the *input and output have equivalent definitions* (i.e. one unit is the same quantity for input and output), as well as among various logical operations. This requires that constant V_{in} assumes the same value throughout a network, and this will allow the output of one gate element to couple easily to another gate element as input, so that gates can be wired directly into gate arrays implementing compounded logic operations.

In order to obtain all the desired input-output responses of the different gates, we need to satisfy the conditions enumerated in Table 1.1 simultaneously. So given a dynamics $f(x)$ corresponding to the physical device in actual implementation, one must find values of the threshold and initial state which satisfy the conditions derived from the Truth Tables to be implemented (see Table 1.2).

Table 1.1 Truth table of the basic logic operations for a pair of inputs: I_1, I_2 [1]. The 1-input NOT gate is given by: NOT(0) is 1; NOT(1) is 0.

I_1	I_2	NAND	NOR	XOR	AND	OR	XNOR
0	0	1	1	0	0	0	1
0	1	1	0	1	0	1	0
1	0	1	0	1	0	1	0
1	1	0	0	0	1	1	1

A representative example is given in Table 1.3, which shows the exact solutions of the initial x_0 and threshold E which satisfy the conditions in Table 1.2 when the dynamical evolution is governed by the prototypical logistic equation:

$$f(x) = 4x(1 - x)$$

The constant $V_{\text{in}} = \frac{1}{4}$ is common to both input and output and to all logical gates.

Table 1.2 Necessary and sufficient conditions, derived from the logic truth tables, to be satisfied simultaneously by the nonlinear dynamical element, in order to have the capacity to implement the logical operations AND, OR, XOR, NAND, NOR and NOT (cf. Table 1.1) with the same computing module.

Logic Operation	Input Set (I_1, I_2)	Output	Necessary and Sufficient Condition
AND	(0,0)	0	$f(x_0) < E$
	(0,1)/(1,0)	0	$f(x_0 + V_{\text{in}}) < E$
	(1,1)	1	$f(x_0 + 2V_{\text{in}}) - E = V_{\text{in}}$
OR	(0,0)	0	$f(x_0) < E$
	(0,1)/(1,0)	1	$f(x_0 + V_{\text{in}}) - E = V_{\text{in}}$
	(1,1)	1	$f(x_0 + 2V_{\text{in}}) - E = V_{\text{in}}$
XOR	(0,0)	0	$f(x_0) < E$
	(0,1)/(1,0)	1	$f(x_0 + V_{\text{in}}) - E = V_{\text{in}}$
	(1,1)	0	$f(x_0 + 2V_{\text{in}}) < E$
NOR	(0,0)	1	$f(x_0) - E = V_{\text{in}}$
	(0,1)/(1,0)	0	$f(x_0 + V_{\text{in}}) < E$
	(1,1)	0	$f(x_0 + 2V_{\text{in}}) < E$
NAND	(0,0)	1	$f(x_0) - E = V_{\text{in}}$
	(0,1)/(1,0)	1	$f(x_0 + V_{\text{in}}) - E = V_{\text{in}}$
	(1,1)	0	$f(x_0 + 2V_{\text{in}}) < E$
NOT	0	1	$f(x_0) - E = V_{\text{in}}$
	1	0	$f(x_0 + V_{\text{in}}) < E$

Above, we have explicitly shown how one can select temporal responses, corresponding to different logic gate patterns, from a nonlinear system, and this ability allows us to construct flexible hardware. Contrast our use of nonlinear elements here with the possible use of linear systems on one hand and stochastic systems on the other. It is not possible to extract all the *different* logic responses from the *same* element in the case of linear components, as the temporal patterns are inherently very limited. So linear elements do not offer much flexibility or versatility. Stochastic elements on the other hand have many different temporal sequences. However, they are *not deterministic* and so one cannot use them to *design* components. Only nonlinear dynamics enjoys both richness of temporal behavior as well as determinism.

Table 1.3 One specific set of solutions of the conditions in Table 1.2 which yield the logical operations AND, OR, XOR, NAND and NOT, with $V_{\text{in}} = \frac{1}{4}$. Note that these theoretical solutions have been fully verified in a discrete electrical circuit emulating a logistic map [5].

Operation	AND	OR	XOR	NAND	NOT
x_0	0	1/8	1/4	3/8	1/2
E	3/4	11/16	3/4	11/16	3/4

Also note that, while *nonlinearity* is absolutely necessary for implementing all the logic gates, chaos may not always be necessary. In the representative example of the logistic map presented in Table 1.3, solutions for all the gates exist only at the fully chaotic limit of the logistic map but the degree of nonlinearity necessary for obtaining all the desired logic responses will depend on the system at hand and on the specific scheme employed to obtain the input-output mapping. It may happen that certain nonlinear systems will allow a wide range of logic responses without actually being chaotic.

1.6 Continuous-Time Nonlinear System

We now present a somewhat different method for obtaining logic responses from a continuous-time nonlinear system. Our processor is now a continuous-time system described by the evolution equation $d\,\mathbf{x}/dt = \mathbf{F}(\mathbf{x}, t)$, where $\mathbf{x} = (x_1, x_2, \ldots x_N)$ are the state variables and $\mathbf{F}$ is a nonlinear function. In this system we choose a variable, say x_1, to be thresholded. Whenever the value of this variable exceeds a threshold E it resets to E, i.e. when $x_1 > E$ then (and only then) $x_1 = E$.

Now the basic 2-input 1-output logic operation on a pair of inputs I_1, I_2 in this method simply involves the setting of an inputs-dependent threshold, namely the threshold is:

$$E = V_{\text{C}} + I_1 + I_2$$

where V_C is the dynamic control signal determining the functionality of the processor. By switching the value of V_C one can switch the logic operation being performed.

Again I_1/I_2 has the value 0 when the logic input is 0 and has the value V_{in} when the logic input is 1. So the threshold E is equal to V_C when the logic inputs are $(0,0)$, $V_C + V_{in}$ when the logic inputs are $(0,1)$ or $(1,0)$ and $V_C + 2V_{in}$ when the logic inputs are $(1,1)$.

The output is again interpreted as a logic output 0 if $x_1 < E$, i.e. the excess above threshold $V_0 = 0$. The logic output is 1 if $x_1 > E$, and the excess above threshold $V_0 = (x_1 - E) \sim V_{in}$. The schematic diagram of this method is displayed in Figure 1.1.

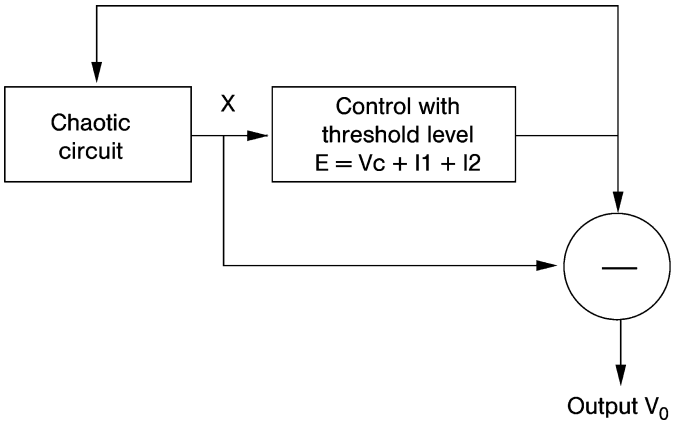

Figure 1.1 Schematic diagram for implementing a morphing 2 input logic cell with a continuous time dynamical system. Here V_C determines the nature of the logic response, and the 2 inputs are $I1, I2$.

Now, for a NOR gate implementation ($V_C = V_{NOR}$) the following must hold true (cf. truth table in Table 1.1):

- when input set is $(0,0)$, output is 1, which implies that for threshold $E = V_{NOR}$, output $V_0 = (x_1 - E) \sim V_{in}$;
- when input set is $(0,1)$ or $(1,0)$, output is 0, which implies that for threshold $E = V_{NOR} + V_{in}$, $x_1 < E$ so that output $V_0 = 0$;
- when input set is $(1,1)$, output is 0, which implies that for threshold $E = V_{NOR} + 2V_{in}$, $x_1 < E$ so that output $V_0 = 0$.

For a NAND gate ($V_C = V_{NAND}$) the following must hold true (cf. truth table in Table 1.1):

- when input set is $(0,0)$, output is 1, which implies that for threshold $E = V_{\text{NAND}}$, output $V_0 = (x_1 - E) \sim V_{\text{in}}$;
- when input set is $(0,1)$ or $(1,0)$, output is 1, which implies that for threshold $E = V_{\text{in}} + V_{\text{NAND}}$, output $V_0 = (x_1 - E) \sim V_{\text{in}}$;
- when input set is $(1,1)$, output is 0, which implies that for threshold $E = V_{\text{NAND}} + 2V_{\text{in}}$, $x_1 < E$ so that output $V_0 = 0$.

In order to design a dynamic NOR/NAND gate one has to find values of V_C that will satisfy all the above input-output associations in a robust and consistent manner.

1.7 Proof-of-Principle Experiments

1.7.1 Discrete-Time Nonlinear System

In this section, we describe an iterated map whose nonlinearity has a simple (i.e. minimal) electronic implementation. We then demonstrate explicitly how all the different fundamental logic gates can be implemented and morphed using this nonlinearity. These gates provide the full set of gates necessary to construct a general-purpose, reconfigurable computing device.

Consider an iterated map governed by the following equation:

$$x_{n+1} = \frac{\alpha x_n}{1 + x_n^{\beta}} \tag{1.1}$$

where α and β are system parameters. Here we will consider $\alpha = 2$ and $\beta = 10$ where the system displays chaos.

In order to realize the chaotic map above in circuitry, one needs two sample-and-hold circuits (S/H): the first S/H circuit holds an input signal (x_n) in response to a clock signal CK1. The output from this sample-and-hold circuit is fed as input to the nonlinear device for subsequent mapping, $f(x_n)$. A second sample-and-hold (S/H) circuit takes the output from the nonlinear device in response to a clock signal CK2. In lieu of control, the output from the second S/H circuit (x_{n+1}) closes the loop as the input to first S/H circuit. The main purpose of the two sample-