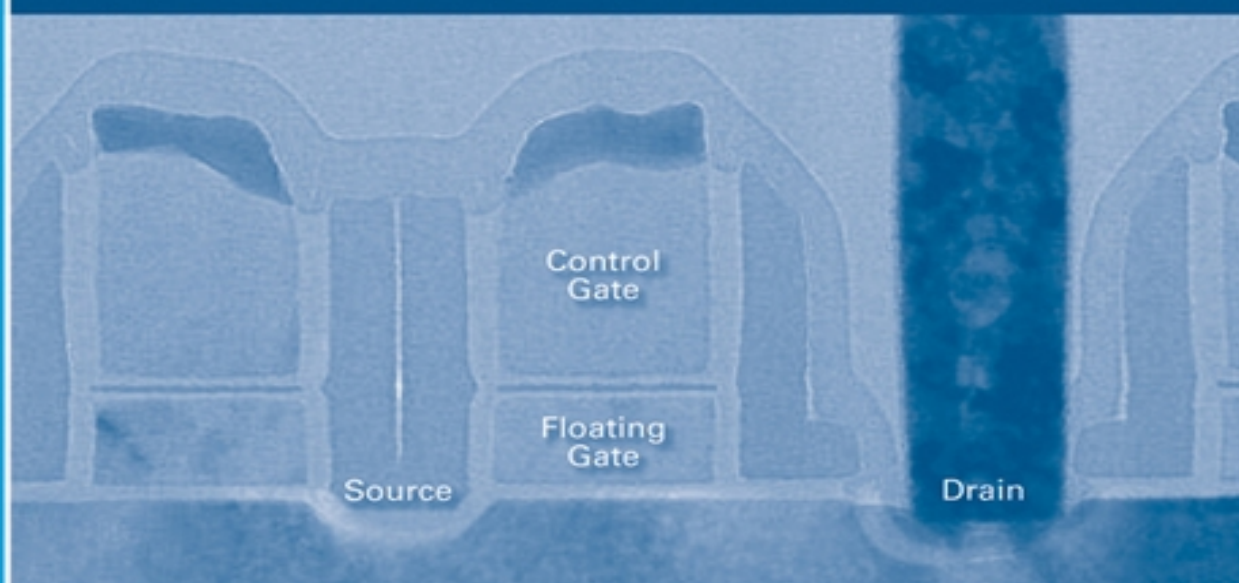


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Nonvolatile Memory Technologies *with* Emphasis on Flash



*A Comprehensive Guide to
Understanding and Using NVM Devices*

Edited by
JOE E. BREWER and MANZUR GILL

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FOREWORD

The story of Flash memory is one of a unique technology that was almost a failure. Only after three unsuccessful attempts did Flash succeed in the marketplace. To succeed, Flash had to solve several technical problems and had to create a market for itself. Once these issues were addressed, Flash quickly became the highest volume nonvolatile memory displacing the EPROM only 5 years after its successful entry in the market. Today, Flash is challenging DRAM for the highest volume semiconductor memory used in the world. While the market forecast for Flash is bright, the technology is approaching fundamental limits in its scalability.

Flash memory was born in a time of turmoil during a semiconductor recession in the mid-1980s. The highest volume writeable nonvolatile memory, the EPROM, was under extreme price pressure due to a maturing market with over 20 competitors. In addition, customers were growing weary of the UV erase required to reprogram an EPROM. They wanted the electrically erase capability of the new high-priced EEPROM technology at EPROM prices. This spurred Toshiba, SEEQ, and Intel to search for the “holy grail of nonvolatile memory,” the single-transistor electrically erasable memory. In 1985, Toshiba was the first to announce a single-transistor electrically erasable memory and coined the name “Flash memory” as the new device erased in a “flash.” Unfortunately, Toshiba’s initial Flash product was difficult to use and, as a result, a market failure. SEEQ followed a year later with another complex Flash device that did not succeed in the market. Meanwhile, Intel took a diversion in attempting to develop a single-transistor EEPROM technology by partnering up with Xicor, one of the early EEPROM memory pioneers. While the single-transistor EEPROM looked good on paper, the reality was the cell operating window was nonexistent and the partnership was

dissolved. Fortunately for Intel, a parallel internal development on an EPROM-based Flash memory technology was started as a “skunkworks project.” By 1985, Intel had a working 64-kb Flash memory in the lab. But to everyone’s surprise, the Intel EPROM business unit was not interested in commercializing Flash, claiming that the market would not accept it based on Toshiba’s lack of success and a fear of Flash cannibalizing Intel’s own EPROM business. If it were not for Gordon Moore and a band of very dedicated pioneers, Intel would never have entered the Flash market. In 1986, Intel formed a separate Flash business unit and introduced a 256-kb Flash memory 2 years later. With over 95% of its manufacturing steps the same as an EPROM, the Intel Flash technology was able to quickly ramp up in volume using existing EPROM fabs. To ensure market success, Intel designed its 256-kb Flash as an EPROM replacement by having the same package pinout and control signals as EPROM devices.

Flash was able to easily cannibalize EPROM embedded applications where cost-effective reprogramming was required. One of the very first commercial Flash memory applications was on an adjustable oil well drill bit. Clearly, the oil drillers did not want to pull up the drill bit every time they needed to adjust it. Other embedded applications followed the conversion to Flash. . . including automotive engine control, laser printers, robotics, medical, factory automation, disk drive controllers, telecommunication, and military applications. With Flash commercially successful, the race was on and several other competitors entered the Flash market.

New customer-desired features were added to Flash that enabled Flash to penetrate markets beyond the simple EPROM replacement business. The memory array was segmented into independently erasable blocks and all the control circuitry was placed on-chip for automated

programming and erase functions. Charge pumps were added to eliminate the need for a high-voltage program/erase supply voltage. New innovative packaging such as TSOP, “bumped” bare die, and memory cards were utilized to enter the portable equipment market.

The real high-volume Flash applications were developed based on these new features. One of these high-volume Flash applications was the digital camera. The first real-time demonstration of a digital camera using a Flash “film card” was in April of 1988 during the Intel 256-kb Flash product introduction at the Eiffel Tower in Paris. A picture was taken of a journalist in the audience; and then, electronically, the journalist was placed on a beach in Tahiti. While a novelty through much of the 1990s, the Flash “electronic film” business took off as the sales of digital cameras crossed over the sales of film-based cameras in 2003. The steep ramp in digital camera sales combined with the rapidly increasing digital picture resolution will drive an insatiable demand for Flash for many years to come. Another high-volume Flash application similar to the digital camera is the portable music player. The portability and the ability to store thousands of songs have made Flash the ideal storage media for these MP3 music players. One of the earliest high-volume Flash applications was the cellular phone. In the early 1990s, the Flash cell phone market took off. Every cell phone needed to have Flash to store the frequently changing cellular digital protocols. Today, cell phones utilize Flash chips up to 256 Mb in density to store games and pictures as well as the cellular protocols.

As Flash prices continue to fall, more high-volume applications will emerge for Flash. In the future, expect to see digital video recorders and portable DVD players that utilize Flash to store videos. In your PC, the portion of the magnetic disk drive that stores your program code (Windows, Word, Photoshop, etc.) will be replaced by

“instantly on” Flash memory. These are a few of the new and exciting applications of Flash that are on the horizon.

Flash memory technology has evolved in two major directions. In the early years of Flash, there was only a single type of Flash, NOR Flash. NOR Flash has a random-access memory cell optimized for high-speed applications such as the cell phone and other code storage applications. A serial-based NAND Flash technology was created to meet the emerging needs of the low-cost file storage market that can live with a slow serial read access time. The primary NAND Flash applications are the digital camera and the portable MP3 music players. Due to technical problems, NAND Flash was not commercially successful until the mid-1990s. However, with the skyrocketing customer demand for digital cameras and MP3 players, NAND Flash volume crossed over NOR Flash volume in 2005.

Flash memory has scaled very nicely following “Moore’s law.” In 1988, the 256 kb Flash memory was fabricated on a 1.5- μm process and had a 36- μm^2 memory cell size. By 2003, Flash evolved to a 256-Mb density on a 0.13- μm process with a 0.154- μm^2 memory cell size. This scaling has driven the pricing of Flash memory from \$1000/MB in 1988 to about 10 cents/MB in 2004. That is an astounding 10,000 times cost reduction in only 16 years! No wonder Flash has become the fastest growing memory market in history. Starting at \$1 million of revenue in 1988, the Flash total available market has grown to over \$10 billion in 2003. Flash is projected to cross over DRAM in sales in 2007 with over a \$40 billion market size.

The future of Flash technology is not as rosy as the business projections. Flash scaling is running out of gas. At the 45-nm level, the physics of the Flash device begins to break down. The electric fields required for programming and erase are so high that materials begin to fall apart. Flash will continue to scale, but it will be a game of

diminishing returns. As a result, almost all the major Flash suppliers have begun work on a Flash replacement technology. Intel is experimenting with Ovonic Unified Memory. Meanwhile, Motorola is looking at silicon nanocrystals. Other alternatives being pursued include magnetic RAM (MRAM), ferroelectric RAM (FeRAM), and polymer memory. It will be interesting to see if one of these innovative technologies can become a reliable high-volume memory replacement for Flash.

RICHARD D. PASHLEY

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BIOGRAPHICAL NOTE

Dr. Pashley retired from Intel in 1998 after 25 years of service. His most significant accomplishment at Intel was the development of Intel's Flash memory business from its technical inception in 1983 to a \$1 billion business in 1998. One of Dr. Pashley's technical teams invented the world's first NOR ETOX Flash memory cell and demonstrated product viability in 1985. In 1986, Gordon Moore gave Dr. Pashley the responsibility to start up a Flash memory business inside Intel. As general manager of the Flash Memory Business, Dr. Pashley directed all aspects of the business including engineering, manufacturing, marketing, and financial. Early in 1988, his Flash business team began selling its first Flash memory product. By 1990, Intel Flash Memory Business was so successful that it was merged with the Intel EPROM Business under Dr. Pashley. In 1993, he was appointed Vice President of Intel.

Dr. Pashley joined Intel in 1973 as a SRAM memory design engineer. One year later, he was promoted to HMOS program manager where he was responsible for the

development of Intel' s next-generation microprocessor and SRAM silicon technology. From 1977 to 1986, he held positions as director of microprocessor/SRAM technology development and director of nonvolatile memory technology development.

Dr. Pashley is currently an adjunct professor in the Graduate School of Engineering at the University of California Davis where he is teaching a class on technology management.

PREFACE

Nonvolatile Memory Technologies with Emphasis on Flash (NMT) was written to provide a detailed view of the integrated circuit main-line technologies that are currently in mass production. It also gives an introduction to technologies that have less manufacturing exposure, and it presents a description of various possible alternative technologies that may emerge in the future. All variations of Flash technology are treated. This includes Flash memory chips, Flash embedded in logic, binary cell Flash, and multilevel cell Flash. The scope of treatment includes basic device structures and physics, principles of operation, related process technologies, circuit design, overall design trade-offs, reliability, and applications.

The ambitious goal for NMT was to serve as *the* authoritative reference guide for nonvolatile memory users, engineers, and technical managers. Individual chapters were written by leading practitioners in the nonvolatile memory field who have participated in the pioneering research, development, design, and manufacture of technologies and devices. We wanted to provide authoritative background information to practicing engineers in the areas of circuit design, applications, marketing, device design, and reliability. We expected that the emergence of Flash embedded in logic chips would increase the audience and demand for a reference book of this nature.

New engineers and graduate students should find the book particularly useful. It may serve as a text or supporting reference for graduate courses. Persons unfamiliar with the nonvolatile memory field will find the inclusion of an elementary tutorial introductory chapter helpful as an orientation to the field. The objective of that chapter was to help the nonspecialist become familiar with the basic concepts of nonvolatile semiconductor memory.

Chapter 2, on applications, explains in detail the nature and utility of nonvolatile memory and delves into the complexities of memory organization, software/hardware internal control, and memory packaging. This is perhaps the most complete treatment of these matters provided in any existing book on nonvolatile memory.

Chapter 3 is devoted to an exposition of the circuit aspects of a modern memory device. Required circuit functions are described, dominant circuit architectures are presented, and key circuit blocks are explained. Techniques for management of defects and “design for test” approaches are provided.

Chapter 4 treats the physics of Flash memories at a mature tutorial engineering level. It begins with an examination of the basic operations of the memory transistor and explains the important characteristics from a physics perspective including circuit models and equations. Physical phenomena associated with programming and erase including conduction modes and key reliability issues are presented. The critical question of oxide degradation is examined in some detail.

The successive chapters are devoted to the mainstream classifications of Flash memory including stacked-gate standard ground Flash (Chapter 5), NAND Flash (Chapter 6), DINOR Flash (Chapter 7), and P-channel Flash (Chapter 8). Both the history and design implementation of these specific Flash variants are treated in great detail. The important topic of embedded Flash is addressed in Chapter 9. It is expected that embedded Flash will become an almost universal feature of emerging “system on a chip” devices. The uses of embedded Flash are explained and supporting circuit and design technology is presented.

In Chapter 10, tunnel dielectrics are briefly examined with an eye toward implementation of dielectric processing. Chapter 11 is a comprehensive examination of Flash

reliability that delves into all aspects of the complex mechanisms that impact device life and performance. Chapter 12 presents the important subject of multilevel cell memory. This is a basic tutorial introduction to the multilevel cells that includes perspective on the value and key issues associated with the approach.

Chapter 13, the final chapter, is devoted to memory technologies that may become successful alternatives to the conventional floating-gate Flash in various applications. Authored by leading developers and advocates of the respective technologies, this chapter provides an excellent engineering level introduction to NROM, ferroelectric memory, solid-state magnetic memory, single- and few-electron memories, resistive (crossbar) memory, and NOVORAM. NROM, of course, is already well on its way into high-volume production as a “non-floating-gate” version of Flash memory.

Credit for the original concept for NMT belongs to my friend and co-editor Manzur Gill. Manzur was the author of the Flash chapter in the 1998 book *Nonvolatile Semiconductor Memory Technology* that William Brown and I co-edited. It is a bit of trivia that a role reversal occurred with NMT. The idea for the early book was mine and Bill Brown bore the bulk of the editorial work in pulling it together. With NMT, my co-editor had the idea and I did the bulk of the editorial work. Of course, that means I am to blame for any errors that survived our many reviews.

The book chapters can be read sequentially, but most chapters provide sufficient background material that they can stand alone. We have tried to reflect the state of the art in 2006–2007, but we are well aware that the passage of time and the pace of the technology will rapidly make some of our pronouncements seem quaint. That is the risk and fun of being in this business.

Manzur and I feel privileged to have had the opportunity to work with the many talented contributors to this work. We have listed their names and affiliations in the list of contributors. Our chapter authors come from countries around the world, and most major NVM device manufacturers are represented in this group. We are also indebted to Richard Pashley for providing a historical view of the technologies in the Foreword.

We hope that you will find our labors useful, and invite your comments and corrections. It is only through feedback that we can improve.

Joe E. Brewer

Gainesville, Florida
October 2007

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ABOUT THE EDITORS

Joe E. Brewer holds a Master of Science degree in Electrical Engineering and has been engaged in nonvolatile memory development for the past four decades. Most of his career was spent with Westinghouse Electric (now Northrop Grumman Corporation) until retirement in May 1998. In 2000, he joined the faculty of the Electrical and Computer Engineering Department of the University of Florida. He was an early contributor to the IEEE Standards for MNOS Arrays and Floating Gate Arrays and led a series of Nonvolatile Memory Technology Workshops hosted at Westinghouse through the 1980s and 1990s. He and William Brown edited the 1998 IEEE Press book *Nonvolatile Semiconductor Memory Technology* and is co-editor with Stuart K. Tewksbury of the IEEE Press Book Series on Microelectronic Systems. He is the Electron Device Society liaison and the CPMT Society liaison to the IEEE Press. From 1996 to 2006, he was an editor for the *IEEE Circuits & Devices Magazine* and he has served as guest editor for several special topics in the *IEEE Transactions on Components, Packaging and Manufacturing Technology*. He is a professional engineer registered in Maryland and Florida and a Fellow of the IEEE. Mr. Brewer holds 7 U.S. patents and has authored more than 100 conference and journal papers.

Manzur Gill holds a Ph.D. in Electrical Engineering and has had more than 25 years of experience in high-tech industry and nonvolatile memory development. He was a senior member of technical staff at Texas Instruments, a nonvolatile memory design manager at National Semiconductor, and senior program manager in Flash memory development in NVM Exploratory Technologies and Ovonic Technology Development at Intel Corporation. He has managed international technology development teams and mentored industry-sponsored student development at universities. Dr. Gill has authored more than 30 technical