MODERN RECEIVER FRONT-ENDS

Systems, Circuits, and Integration

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PREFACE

In recent years, the research and developments in the area of RF and microwave technologies have progressed significantly due to the growing demand for applicability in wireless communication technologies. Starting from 1992, wireless communication technologies have become quite mature. In the modern era of electronic developments, design of wireless handsets is an example of integration of many diverse skill sets. Classical books in the areas of microwave technology provide us with an in-depth knowledge of electromagnetic fundamentals. On the other hand, books covering analog circuit design introduce the reader to the fundamentals of basic building blocks for wireless communications. However, with the tremendous advances in wireless technologies, both in wireless systems as well as semiconductor processes, wireless solutions have become a manifestation of integrated design philosophies in the areas of analog, microwave, and communication system theory. The main focus of this book is the integration of and interaction among various building blocks and the development and characterization of receiver subsystems for wireless applications. During the years of our involvement with the graduate curriculum at the Georgia Institute of Technology, we felt that such a book would be very helpful for understanding of receiver front-end development and architectural trade-offs, and could be helpful to students, professionals, and the interested scientific community. It could also serve the needs of an aggressive researcher in the area of receiver front-ends.

The book is organized into nine chapters, as outlined below.

Chapter 1 provides an introduction to the advanced receiver architectures. Chapter 2 provides the different issues and parameters concerned with system design for receiver front-ends. Chapter 3 is targeted toward an overview of different receiver architectures and their applications. Chapter 4 walks the reader through an example of high-frequency receiver front-end design in a commercially available silicon germanium technology. Receiver design and developments are discussed in detail, along with simulation and characterization techniques necessary to focus on details of implementation to the reader, and the chapter is anticipated to be helpful for students in their research projects. This chapter provides the reader with the full flow of a design cycle, starting from computer simulation and ending with real silicon implementations. Chapter 5 is focused on various subharmonic mixing techniques, starting with the different methods of realizing subharmonic mixing technique, and followed by their integrability with other RF building blocks. Chapter 6 provides a silicon-based active subharmonic mixing approach, which is very helpful in developing an in-depth understanding for the receiver front-ends. Chapter 7 demostrates various types of passive components and their integration methodologies in silicon-based substrates. Chapter 8 describes various practical issues in the integration of receiver subsystems. Chapter 9 introduces the interested reader to the potential future applications of wireless communications.

All in all, we have tried to maintain a good balance of theoretical foundation, design procedures, and practical characterization issues toward the development of fully integrated receiver front-ends. All of the architectures are demonstrated in commercially available semiconductor process technologies. Silicon-based processes have been focused on in greater detail due to their popularity and potential in future generations of lower-cost wireless communication solutions.

This book is written with the assumption that the reader has knowledge of basic electronic circuits, microwave fundamentals, and communication theory. Although the book starts with basic receiver design and integration techniques, and talks about the state-of-the-art implementations afterward, a prior background in all of the above-mentioned areas provides a much better appreciation for the technical material presented in this book.

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INTRODUCTION

Any communication system, in the simplest form, consists of a transmitter, a signal path, and a receiver. The performance of such systems depends heavily on each of the building blocks and the impact of the given communication link on the signal. Although the impact of the path is fixed by the frequency of the RF signal and the properties of the physical medium in which the signal propagates, the behavior of the transmitter and receiver can be flexible. The electrical performances of the transmitter and receiver determine the impact of these blocks on the signal and limit the quality and range of the communication link. The appropriate topology, semiconductor technologies, and a careful design based on well-defined system parameters can make a huge difference in performance, cost, and marketability of the individual transmitter, receiver, and the entire system.

This book will take a very narrow focus on receiver design by limiting its scope to receivers for wireless applications. In order to provide the reader with a comprehensive understanding of the subject at hand, a thorough system and architecture analysis will be presented. This top level analysis will then be complemented with a touch of reality when we start describing choices, compromises, and challenges that a design engineer will face during the process of developing a cost-effective and marketable receiver product in the form of an integrated circuit (IC).

The basic developments in the area of wireless communication date back to the early 20th century. Since the early years of the 20th century, wireless engineering has come a long way. Most of the basic principles of sophisticated radio architecture, as we see it today, were developed using vacuum tubes around 1930. Starting with the basic foundation laid down by Maxwell (1883), and with subsequent inventions in wave propagation and wireless telegraphy by Hertz, Marconi, and others, wireless technology was born around 1900 in a very primitive form. Demonstration of a superheterodyne receiver by Armstrong dates back to as early as 1924.

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Armstrong's superheterodyne receiver underwent considerable refinement during the 1920s and 1930s. This was the time when radio pioneers considered the use of homodyne architectures for single vacuum tube receivers. For over two decades, the standard low-end consumer AM tunable radio used a system of five vacuum tubes [1, 2]. A major milestone was set by the invention of the transistor by Bardeen, Brattain, and Schockley in 1948, which changed the world of vacuum tubes. However, implementing radios was a farsighted vision at that time. As semiconductor technologies became more mature, more circuit integration took place. Starting with small-scale integration in the standard integrated circuits, the trend moved toward more integration and high-speed microprocessors. With the tremendous growth in the VLSI side, demands for ubiquitous computing and wireless applications increased. Vance at ITT was the first to apply direct conversion for pager applications by means of a single-chip receiver [3]. During the early 1980s, direct conversion receivers were developed at Motorola (patents were filed in the 1985 time frame) as a possible way to implement compact radios. However, the first attempt did not make a significant impact in the marketplace. To date, the superheterodyne architecture has been the winner for the industry in wireless communication technologies. Most of the direct conversion architecture realizations still reside in the research domain.

The initial necessity of communicating through short messages eventually evolved to the need to communicate audio- and video-based messages, and many other real-time applications. All of these basic requirements led to the need for increasingly higher data rates for next-generation wireless communication applications. Two primary directions driving the application space as of today include cellular telephony and wireless local area networks (WLANs). In recent years, there has been a lot of interest in more integration on-chip to realize these solutions in a compact and lower-cost fashion. Very low IF (VLIF) and direct conversion architectures are quite attractive for ultracompact, low-power, and low-cost solutions for wireless applications. If implemented successfully, direct conversion radios are the most compact realizations one can achieve. With the growing demand for wireless technology, and simultaneous development of mature and reliable semiconductor technologies, direct conversion architecture is favorable for future wireless communication technologies. At the time of writing this book, a major part of the IC industry is focused toward communication applications, both wireless and wired. Emerging applications include wideband code division multiplexing (WCDMA), IEEE802.11X, multiband, ultrawide band (UWB), and 60 GHz WLAN technology. All of these implementations are being targeted to low supply voltages as well, as a consequence of shrinking dimensions of the transistors, and to realize low-power solutions. All of these developments have motivated researchers to investigate superior process technology, novel circuit design techniques, and improved system engineering. The direct conversion architecture has the potential to satisfy the needs of most of the above mentioned applications.

Along with the development of wireless communication technologies, semiconductor technologies have also experienced tremendous evolution over the past decade. Starting with gallium arsenide (GaAs) based technologies for high-frequency design, the focus has slowly shifted from III–V semiconductors to silicon-based technologies for lower cost and higher integration during the early 1990s in the research domain. Currently available silicon-based technologies, which show enormous potential for RF technologies, include standard digital CMOS, silicon-on-insulator (SOI), and silicon–germanium (SiGe). Bulk CMOS technologies have become much more attractive for RF design during recent times because of low cost and other potential advantages related to continued scaling in the deep-submicron (DSM) regime. RF circuit implementations in standard CMOS technologies have developed considerably well over the past couple of years [4]. However, there still exists a question about how much of the RF CMOS implementation will be really adopted by the industry. This skepticism is the result of the lower yield and reliability of such technologies for high-frequency analog and RF applications. SOI-based CMOS processes have shown improvement over standard digital CMOS technologies in many aspects [5]. Silicon-on-insulator technology has shown promise in digital microprocessor applications and, hence, is a strong candidate for future system-on-a-chip (SOC) realizations. Although SOI technology was originally proposed in 1970, its potential has not yet been fully explored in analog/RF designs. SiGe BiCMOS technology has proven to be a very strong candidate for RF as well as back-end digital designs [6]. Recent reports of state-of-the-art SiGe BiCMOS technologies [7] have shown a cutoff frequency (F_t) of up to 200 GHz and are quite capable of handling next-generation high-data-rate applications. Currently, silicon-based RFIC solutions are just about to penetrate the commercial market for both wired and wireless applications. At this point, it would be quite interesting to take a step back and think carefully about advances in the wireless IC world. It is noteworthy that the very basic principles of circuit design have not changed significantly from the 1920s, but their applications have. Experts are often tempted to call this technical advancement an “evolution” as opposed to a “revolution.”

1.1. CURRENT STATE OF THE ART

Starting with the initial developments of superheterodyne architectures, radio front-ends have gone through many changes. Many researchers are working mostly toward implementing very low IF frequency and direct conversion radio front-ends for low power and compact implementations. Radio frequency receiver integrated circuits require a combination of expertise in the areas of circuit design and system architecture, and the choice of a suitable process technology for various applications. As we progress through the subsequent chapters, the reader will get a clear picture about how these disciplines are intertwined in today’s world of advanced receivers. Table 1.1 summarizes reports of direct conversion solutions to date, along with key distinguishing technological features. It is quite interesting to note the co-existence of the III–V semiconductor (GaAs MESFET) implementations with those in silicon-based technologies.

This book will address the different issues and challenges in the development of highly integrated receiver subsystems. It reviews a wide variety of receiver subsys-

Table-1.1. Summary of reported state-of-the-art direct conversion solutions:

References	Technical Approach	Process Technology	Application
Reference [10, 17] (UCLA)	1. Active circuitry in the front-end 2. Single balanced mixer	0.6 μm CMOS	GSM (0.9 GHz), 1.9 GHz
Reference [11] (Toshiba R&D)	1. Active circuitry in the front-end	0.8 μm SiGe BiCMOS	PCS, 1.9 GHz
Reference [8] (Mitsubishi)	1. Passive-circuit-based front-end 2. Subharmonic APDP-based topology	GaAs MESFET, SiGe	WCDMA
Reference [12] (Helsinki U. of Technology)	1. Active circuitry in the front-end 2. Uses off-chip inductors 3. Modified Gilbert cell mixer	0.35 μm SiGe BiCMOS	WCDMA
Reference [9] (Georgia Tech)	1. Subharmonic APDP-based topology	GaAs MESFET	C band, 5.8 GHz

tem designs, both in terms of topology as well as semiconductor technology. It covers a detailed design perspective, from systems to circuits at high frequency, with a focus on implementation in low-cost semiconductor technologies. It also provides the practical challenges faced by the designers in carrying out a fully integrated receiver solution, with a look forward to futuristic applications in the areas of wireless communications.

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RECEIVER SYSTEM DESIGN

This chapter provides a detailed illustration of system-level parameters for receiver front-end design. A thorough system analysis is the first step in designing a receiver subsystem. The system design helps to define the specification and scope of the entire receiver and every building block in the lineup. This will in turn determine which components will be integrated on-chip or implemented off-chip by other means. Issues such as frequency scheme and the interface with other components in the overall communication system are some of the top-level items determined in this phase. These will allow us to define an overall specification for the receiver, after which the analysis can be extended to the individual blocks of the receiver.

2.1. FREQUENCY PLANNING

Design of a frequency plan has a direct dependence on the receiver topology, number of down-conversions, and the modes of operation, which can be simplified to simplex or duplex operation. This section will focus on the common superheterodyne topology operating in a duplex system. The block diagram of such receiver is shown in Fig. 2.1. There are only two down-conversions, one from RF to IF and the other from IF to baseband I and Q. A thorough frequency planning will involve study of blockers, spurs, and image frequencies. Blockers, spurs, and image interferers are RF signals that are transmitted into the air by other wireless devices and can penetrate and either saturate the receiver or interfere with the signal being received.

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