Device Modeling for Analog and RF CMOS Circuit Design

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Preface

We are fortunate to live in an age in which microelectronics still enjoy an accelerating growth in performance and complexity. Fortunate, since we are experiencing a remarkable progress in science, in communication technology, in our ability to acquire new knowledge, and in the many other wonderful amenities of modern society, all of which are permeated by and made possible by modern microelectronics. This exponential evolutionary trend, as described by Moore's Law, has now lasted for more than three decades, and is still on track, fueled by a seemingly unending demand for ever better performance and by fierce global competition.

A driving force behind this fantastic progress is the long-term commitment to a steady downscaling of MOSFET/CMOS technology needed to meet the requirements on speed, complexity, circuit density, and power consumption posed by the many advanced applications relying on this technology. The degree of scaling is measured in terms of the half-pitch size of the first-level interconnect in DRAM technology, also termed the "technology node" by the International Technology Roadmap for Semiconductors. At the time of the 2001 ITRS update, the technology node had reached 130 nm, while the smallest features, the MOSFET gate lengths, were a mere 65 nm. Within a decade, these numbers are expected to be close to 40 nm and 15 nm, respectively.

Very important issues in this development are the increasing levels of complexity of the fabrication process and the many subtle mechanisms that govern the properties of deep submicrometer FETs. These mechanisms, dictated by device physics, have to be described and implemented into circuit design tools to empower the circuit designers with the ability to fully utilize the potential of existing and future technologies.

Hence, circuit designers are faced with the relentless challenge of staying updated on the properties, potentials, and the limitations of the latest device technology and device models. This is especially true for designers of analog and radio frequency (RF) integrated circuits, where the sensitivity to the modeling details and the interplay between individual devices is more acute than for digital electronics. A deeper insight into these issues is therefore crucial for gaining the competitive edge needed to ensure first-time-right silicon and to reduce time-to-market for new products.

Existing textbooks on analog and RF CMOS circuit design traditionally lack a thorough treatment of the device modeling challenges outlined above. Our primary objectives with the present book is to bridge the gap between device modeling and analog circuit design by presenting the state-of-the-art MOSFET models that are available in analog and SPICE-type circuit simulators today, together with related modeling issues of importance to both circuit designers and students, now and in the future.

This book is intended as a main or supplementary text for senior and graduate-level courses in analog integrated circuit design, as well as a reference and a text for self or group studies by practicing design engineers. Especially in student design projects, we foresee that this book will be a valuable handbook as well as a reference, both on basic modeling issues and on specific MOSFET models encountered in circuit simulators. Likewise, practicing engineers can use the book to enhance their insight into the principles of MOSFET operation and modeling, thereby improving their design skills.

We assume that the reader already has a basic knowledge of common electronic devices and circuits, and fundamental concepts such as small-signal operation and equivalent circuits.

The book is organized into twelve chapters. In Chapter 1, the reader is introduced to the basic physics, the principles of operation, and the modeling of MOS structures and MOSFETs. This chapter also discusses many of the issues that are important in the modeling of modern-day MOSFETs. Chapter 2 walks the reader through the fabrication steps of modern MOSFET and CMOS technology. In Chapter 3, the special concerns and the challenges of accurate modeling of MOSFETs operating at radio frequencies are discussed. Chapter 4 deals with modeling of noise in MOSFETs. Distortion analysis, discussed in Chapter 5, is of special concern for analog MOSFET circuit design. In Chapters 6, 7, and 8, we present the state-of-the-art MOSFET models that are commonly used by the analog design community today. The models covered are BSIM4, EKV, MOS Model 9 and MOSA1. These chapters are written in a reference style to provide quick lookup when the book is used like a handbook. Chapters 9 and 10 are devoted to the modeling of other devices that are of importance in typical analog CMOS circuits, such as bipolar transistors (Chapter 9) and passive devices, including resistors, capacitors, and inductors (Chapter 10). The remaining two chapters deal with essential industry-related issues of circuit design. Chapter 11 discusses the important topic of modeling of process variations and device mismatch effects and Chapter 12 deals with the quality assurance of the device models used by the design houses.

The book is accompanied by two software application tools, AIM-Spice and MOSCalc. AIM-Spice is a version of SPICE with standard SPICE parameters, very familiar to many electrical engineers and electrical engineering students. Running under the Microsoft Windows family of operating systems, it takes full advantage of the available graphics user interface. The AIM-Spice software will run on all PCs equipped with Windows 95, 98, ME, NT 4, 2000, or XP. In addition to all the models included into Berkeley SPICE (Version 3e.1), AIM-Spice incorporates BSIM4, EKV, and MOSA1, which were covered in Chapters 6, 7, and 8. A limited version of AIM-Spice can be downloaded from *www.aimspice.com*. The second tool, MOSCalc, is a Web-based calculator for rapid estimates of MOSFET large- and small-signal parameters. The designer enters the gate length and width, and a range of biasing voltages and/or the transistor currents, whereupon quantities such as gate overdrive voltage, effective threshold voltage, drain-source saturation voltage, all terminal currents, transconductance, channel conductance, and all small signal intrinsic capacitances are calculated. MOSCalc is available at *ngl.fysel.ntnu.no*.

These dedicated software tools allow students to solve real engineering problems, which brings semiconductor device physics and modeling home to the user at a very practical level, bridging the gap between theory and practice. AIM-Spice and MOSCalc can be used routinely by practicing engineers during the design phase of analog integrated circuits.

We are grateful to the following colleagues for their suggestions and/or for reviewing portions of this book: Matthias Bucher and Bjørnar Hernes. We would also like to express our appreciation to the staff at Wiley, UK, and in particular to Kathryn Sharples, for making possible the timely production of the book.

Finally, we would like to thank our families for their great support, patience, and understanding provided throughout the period of writing.

1

MOSFET Device Physics and Operation

1.1 INTRODUCTION

A field effect transistor (FET) operates as a conducting semiconductor channel with two ohmic contacts – the *source* and the *drain* – where the number of charge carriers in the channel is controlled by a third contact – the *gate*. In the vertical direction, the gate-channel-substrate structure (gate junction) can be regarded as an orthogonal two-terminal device, which is either a MOS structure or a reverse-biased rectifying device that controls the mobile charge in the channel by capacitive coupling (field effect). Examples of FETs based on these principles are metal-oxide-semiconductor FET (MOSFET), junction FET (JFET), metal-semiconductor FET (MESFET), and heterostructure FET (HFETs). In all cases, the stationary gate-channel impedance is very large at normal operating conditions. The basic FET structure is shown schematically in Figure 1.1.

The most important FET is the MOSFET. In a silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide (SiO_2) layer. The charge carriers of the conducting channel constitute an inversion charge, that is, electrons in the case of a p-type substrate (n-channel device) or holes in the case of an n-type substrate (p-channel device), induced in the semiconductor at the silicon-insulator interface by the voltage applied to the gate electrode. The electrons enter and exit the channel at n^+ source and drain contacts in the case of an n-channel MOSFET, and at p^+ contacts in the case of a p-channel MOSFET.

MOSFETs are used both as discrete devices and as active elements in digital and analog monolithic integrated circuits (ICs). In recent years, the device feature size of such circuits has been scaled down into the deep submicrometer range. Presently, the 0.13-μm technology node for complementary MOSFET (CMOS) is used for very large scale ICs (VLSIs) and, within a few years, sub-0.1-μm technology will be available, with a commensurate increase in speed and in integration scale. Hundreds of millions of transistors on a single chip are used in microprocessors and in memory ICs today.

CMOS technology combines both n-channel and p-channel MOSFETs to provide very low power consumption along with high speed. New silicon-on-insulator (SOI) technology may help achieve three-dimensional integration, that is, packing of devices into many

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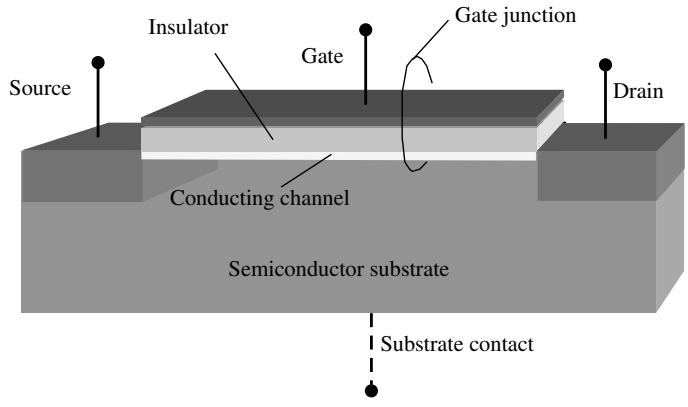

Figure 1.1 Schematic illustration of a generic field effect transistor. This device can be viewed as a combination of two orthogonal two-terminal devices

layers, with a dramatic increase in integration density. New improved device structures and the combination of bipolar and field effect technologies (BiCMOS) may lead to further advances, yet unforeseen. One of the rapidly growing areas of CMOS is in analog circuits, spanning a variety of applications from audio circuits operating at the kilohertz (kHz) range to modern wireless applications operating at gigahertz (GHz) frequencies.

1.2 THE MOS CAPACITOR

To understand the MOSFET, we first have to analyze the MOS capacitor, which constitutes the important gate-channel-substrate structure of the MOSFET. The MOS capacitor is a two-terminal semiconductor device of practical interest in its own right. As indicated in Figure 1.2, it consists of a metal contact separated from the semiconductor by a dielectric insulator. An additional ohmic contact is provided at the semiconductor substrate. Almost universally, the MOS structure utilizes doped silicon as the substrate and its native oxide, silicon dioxide, as the insulator. In the silicon–silicon dioxide system, the density of surface states at the oxide–semiconductor interface is very low compared to the typical channel carrier density in a MOSFET. Also, the insulating quality of the oxide is quite good.

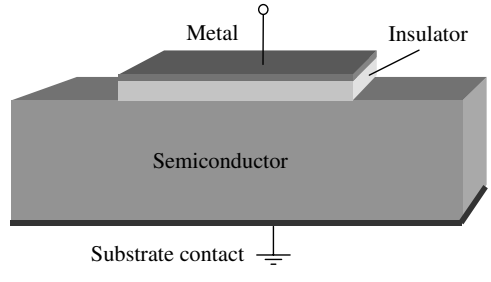

Figure 1.2 Schematic view of a MOS capacitor

We assume that the insulator layer has infinite resistance, preventing any charge carrier transport across the dielectric layer when a bias voltage is applied between the metal and the semiconductor. Instead, the applied voltage will induce charges and counter charges in the metal and in the interface layer of the semiconductor, similar to what we expect in the metal plates of a conventional parallel plate capacitor. However, in the MOS capacitor we may use the applied voltage to control the type of interface charge we induce in the semiconductor – majority carriers, minority carriers, and depletion charge.

Indeed, the ability to induce and modulate a conducting sheet of minority carriers at the semiconductor–oxide interface is the basis for the operation of the MOSFET.

1.2.1 Interface Charge

The induced interface charge in the MOS capacitor is closely linked to the shape of the electron energy bands of the semiconductor near the interface. At zero applied voltage, the bending of the energy bands is ideally determined by the difference in the work functions of the metal and the semiconductor. This band bending changes with the applied bias and the bands become flat when we apply the so-called flat-band voltage given by

$$V_{FB} = (\Phi_m - \Phi_s)/q = (\Phi_m - X_s - E_c + E_F)/q, \tag{1.1}$$

where Φ_m and Φ_s are the work functions of the metal and the semiconductor, respectively, X_s is the electron affinity for the semiconductor, E_c is the energy of the conduction band edge, and E_F is the Fermi level at zero applied voltage. The various energies involved are indicated in Figure 1.3, where we show typical band diagrams of a MOS capacitor at zero bias, and with the voltage $V = V_{FB}$ applied to the metal contact relative to the semiconductor–oxide interface. (Note that in real devices, the flat-band voltage may be

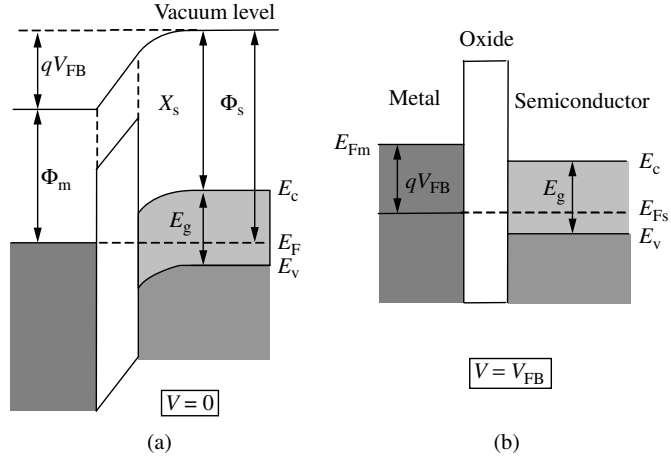

Figure 1.3 Band diagrams of MOS capacitor (a) at zero bias and (b) with an applied voltage equal to the flat-band voltage. The flat-band voltage is negative in this example

affected by surface states at the semiconductor–oxide interface and by fixed charges in the insulator layer.)

At stationary conditions, no net current flows in the direction perpendicular to the interface owing to the very high resistance of the insulator layer (however, this does not apply to very thin oxides of a few nanometers, where tunneling becomes important, see Section 1.5). Hence, the Fermi level will remain constant inside the semiconductor, independent of the biasing conditions. However, between the semiconductor and the metal contact, the Fermi level is shifted by $E_{\mathrm{Fm}} - E_{\mathrm{Fs}} = qV$ (see Figure 1.3(b)). Hence, we have a quasi-equilibrium situation in which the semiconductor can be treated as if in thermal equilibrium.

A MOS structure with a *p*-type semiconductor will enter the *accumulation* regime of operation when the voltage applied between the metal and the semiconductor is more negative than the flat-band voltage ($V_{\mathrm{FB}} < 0$ in Figure 1.3). In the opposite case, when $V > V_{\mathrm{FB}}$, the semiconductor–oxide interface first becomes depleted of holes and we enter the so-called *depletion* regime. By increasing the applied voltage, the band bending becomes so large that the energy difference between the Fermi level and the bottom of the conduction band at the insulator–semiconductor interface becomes smaller than that between the Fermi level and the top of the valence band. This is the case indicated for $V = 0\,\mathrm{V}$ in Figure 1.3(a). Carrier statistics tells us that the electron concentration then will exceed the hole concentration near the interface and we enter the *inversion* regime. At still larger applied voltage, we finally arrive at a situation in which the electron volume concentration at the interface exceeds the doping density in the semiconductor. This is the strong inversion case in which we have a significant conducting sheet of inversion charge at the interface.

The symbol ψ is used to signify the potential in the semiconductor measured relative to the potential at a position x deep inside the semiconductor. Note that ψ becomes positive when the bands bend down, as in the example of a *p*-type semiconductor shown in Figure 1.4. From equilibrium electron statistics, we find that the intrinsic Fermi level E_{i} in the bulk corresponds to an energy separation $q\varphi_b$ from the actual Fermi level E_{F} of the doped semiconductor,

$$\varphi_b = V_{\mathrm{th}} \ln\left(\frac{N_{\mathrm{a}}}{n_{\mathrm{i}}}\right), \tag{1.2}$$

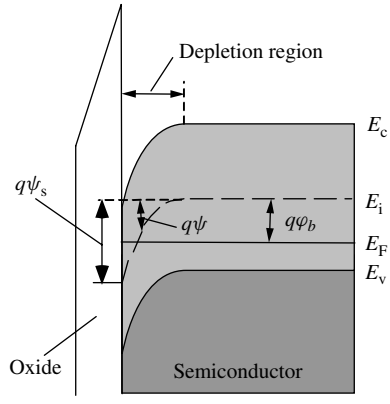

Figure 1.4 Band diagram for MOS capacitor in weak inversion ($\varphi_b < \psi_s < 2\varphi_b$)

where $V_{\rm th}$ is the thermal voltage, $N_{\rm a}$ is the shallow acceptor density in the p-type semiconductor and $n_{\rm i}$ is the intrinsic carrier density of silicon. According to the usual definition, strong inversion is reached when the total band bending equals $2q\varphi_b$, corresponding to the surface potential $\psi_{\rm s} = 2\varphi_b$. Values of the surface potential such that $0 < \psi_{\rm s} < 2\varphi_b$ correspond to the depletion and the weak inversion regimes, $\psi_{\rm s} = 0$ is the flat-band condition, and $\psi_{\rm s} < 0$ corresponds to the accumulation mode.

The surface concentrations of holes and electrons are expressed in terms of the surface potential as follows using equilibrium statistics,

$$p_{\rm s} = N_{\rm a} \exp(-\psi_{\rm s}/V_{\rm th}), \tag{1.3}$$

$$n_{\rm s} = n_{\rm i}^2/p_{\rm s} = n_{\rm po} \exp(\psi_{\rm s}/V_{\rm th}), \tag{1.4}$$

where $n_{\rm po} = n_{\rm i}^2/N_{\rm a}$ is the equilibrium concentration of the minority carriers (electrons) in the bulk.

The potential distribution $\psi(x)$ in the semiconductor can be determined from a solution of the one-dimensional Poisson's equation:

$$\frac{{\rm d}^2\psi(x)}{{\rm d}x^2} = -\frac{\rho(x)}{\varepsilon_{\rm s}}, \tag{1.5}$$

where $\varepsilon_{\rm s}$ is the semiconductor permittivity, and the space charge density $\rho(x)$ is given by

$$\rho(x) = q(p - n - N_{\rm a}). \tag{1.6}$$

The position-dependent hole and electron concentrations may be expressed as

$$p = N_{\rm a} \exp(-\psi/V_{\rm th}), \tag{1.7}$$

$$n = n_{\rm po} \exp(\psi/V_{\rm th}). \tag{1.8}$$

Note that deep inside the semiconductor, we have $\psi(\infty) = 0$.

In general, the above equations do not have an analytical solution for $\psi(x)$. However, the following expression can be derived for the electric field $F_{\rm s}$ at the insulator–semiconductor interface, in terms of the surface potential (see, e.g., Fjeldly *et al.* 1998),

$$F_{\rm s} = \sqrt{2}\frac{V_{\rm th}}{L_{\rm Dp}} f\left(\frac{\psi_{\rm s}}{V_{\rm th}}\right), \tag{1.9}$$

where the function f is defined by

$$f(u) = \pm\sqrt{[\exp(-u) + u - 1] + \frac{n_{\rm po}}{N_{\rm a}}[\exp(u) - u - 1]}, \tag{1.10}$$

and

$$L_{\rm Dp} = \sqrt{\frac{\varepsilon_{\rm s} V_{\rm th}}{q N_{\rm a}}} \tag{1.11}$$

is called the *Debye length*. In (1.10), a positive sign should be chosen for a positive $\psi_{\rm s}$ and a negative sign corresponds to a negative $\psi_{\rm s}$.

Using Gauss' law, we can relate the total charge Q_s per unit area (carrier charge and depletion charge) in the semiconductor to the surface electric field by

$$Q_s = -\varepsilon_s F_s. \tag{1.12}$$

At the flat-band condition ($V = V_{FB}$), the surface charge is equal to zero. In accumulation ($V < V_{FB}$), the surface charge is positive, and in depletion and inversion ($V > V_{FB}$), the surface charge is negative. In accumulation (when $|\psi_s|$ exceeds a few times V_{th}) and in strong inversion, the mobile sheet charge density is proportional to $\exp[|\psi_s|/(2V_{th})]$. In depletion and weak inversion, the depletion charge is dominant and its sheet density varies as $\psi_s^{1/2}$. Figure 1.5 shows $|Q_s|$ versus ψ_s for p-type silicon with a doping density of $10^{16}/\text{cm}^3$.

In order to relate the semiconductor surface potential to the applied voltage V, we have to investigate how this voltage is divided between the insulator and the semiconductor. Using the condition of continuity of the electric flux density at the semiconductor–insulator interface, we find

$$\varepsilon_s F_s = \varepsilon_i F_i, \tag{1.13}$$

where ε_i is the permittivity of the oxide layer and F_i is the constant electric field in the insulator (assuming no space charge). Hence, with an insulator thickness d_i, the voltage drop across the insulator becomes $F_i d_i$. Accounting for the flat-band voltage, the applied voltage can be written as

$$V = V_{FB} + \psi_s + \varepsilon_s F_s / c_i, \tag{1.14}$$

where $c_i = \varepsilon_i / d_i$ is the insulator capacitance per unit area.

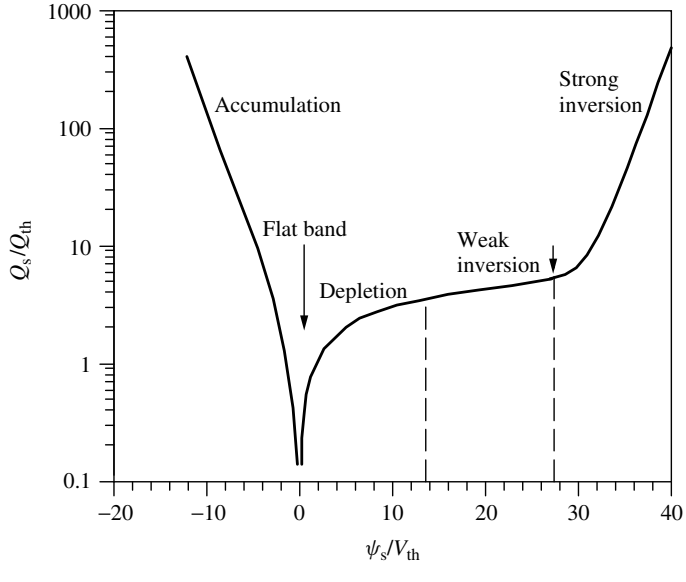

Figure 1.5 Normalized total semiconductor charge per unit area versus normalized surface potential for p-type Si with $N_a = 10^{16}/\text{cm}^3$. $Q_{th} = (2\varepsilon_s q N_a V_{th})^{1/2} \approx 9.3 \times 10^{-9}\,\text{C/cm}^2$ and $V_{th} \approx 0.026\,\text{V}$ at $T = 300\,\text{K}$. The arrows indicate flat-band condition and onset of strong inversion

1.2.2 Threshold Voltage

The threshold voltage $V = V_T$, corresponding to the onset of the strong inversion, is one of the most important parameters characterizing metal-insulator-semiconductor devices. As discussed above, strong inversion occurs when the surface potential ψ_s becomes equal to $2\varphi_b$. For this surface potential, the charge of the free carriers induced at the insulator–semiconductor interface is still small compared to the charge in the depletion layer, which is given by

$$Q_{dT} = -qN_a d_{dT} = -\sqrt{4\varepsilon_s q N_a \varphi_b}, \tag{1.15}$$

where $d_{dT} = (4\varepsilon_s \varphi_b / qN_a)^{1/2}$ is the width of the depletion layer at threshold. Accordingly, the electric field at the semiconductor–insulator interface becomes

$$F_{sT} = -Q_{dT}/\varepsilon_s = \sqrt{4qN_a\varphi_b/\varepsilon_s}. \tag{1.16}$$

Hence, substituting the threshold values of ψ_s and F_s in (1.14), we obtain the following expression for the threshold voltage:

$$V_T = V_{FB} + 2\varphi_b + \sqrt{4\varepsilon_s q N_a \varphi_b}/c_i. \tag{1.17}$$

Figure 1.6 shows typical calculated dependencies of V_T on doping level and dielectric thickness.

For the MOS structure shown in Figure 1.2, the application of a bulk bias V_B is simply equivalent to changing the applied voltage from V to $V - V_B$. Hence, the threshold

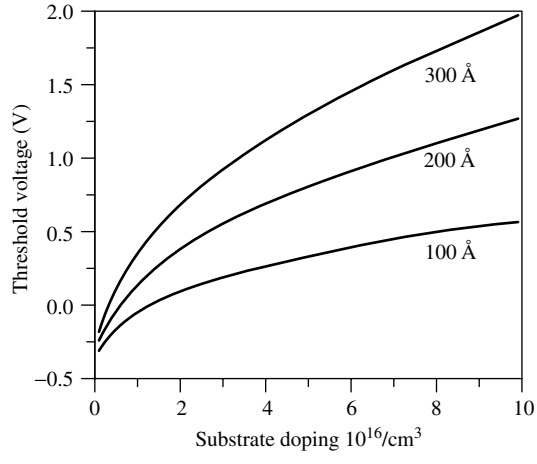

Figure 1.6 Dependence of MOS threshold voltage on the substrate doping level for different thicknesses of the dielectric layer. Parameters used in calculation: energy gap, 1.12 eV; effective density of states in the conduction band, $3.22 \times 10^{25}/m^3$; effective density of states in the valence band, $1.83 \times 10^{25}/m^3$; semiconductor permittivity, 1.05×10^{-10} F/m; insulator permittivity, 3.45×10^{-11} F/m; flat-band voltage, -1 V; temperature: 300 K. Reproduced from Lee K., Shur M., Fjeldly T. A., and Ytterdal T. (1993) *Semiconductor Device Modeling for VLSI*, Prentice Hall, Englewood Cliffs, NJ

referred to the ground potential is simply shifted by V_B. However, the situation will be different in a MOSFET where the conducting layer of mobile electrons may be maintained at some constant potential. Assuming that the inversion layer is grounded, V_B biases the effective junction between the inversion layer and the substrate, changing the amount of charge in the depletion layer. In this case, the threshold voltage becomes

$$V_T = V_{FB} + 2\varphi_b + \sqrt{2\varepsilon_s q N_a (2\varphi_b - V_B)}/c_i. \tag{1.18}$$

Note that the threshold voltage may also be affected by so-called fast surface states at the semiconductor–oxide interface and by fixed charges in the insulator layer. However, this is not a significant concern with modern day fabrication technology.

As discussed above, the threshold voltage separates the subthreshold regime, where the mobile carrier charge increases exponentially with increasing applied voltage, from the above-threshold regime, where the mobile carrier charge is linearly dependent on the applied voltage. However, there is no clear point of transition between the two regimes, so different definitions and experimental techniques have been used to determine V_T. Sometimes (1.17) and (1.18) are taken to indicate the onset of so-called moderate inversion, while the onset of strong inversion is defined to be a few thermal voltages higher.

1.2.3 MOS Capacitance

In a MOS capacitor, the metal contact and the neutral region in the doped semiconductor substrate are separated by the insulator layer, the channel, and the depletion region. Hence, the capacitance C_{mos} of the MOS structure can be represented as a series connection of the insulator capacitance $C_i = S\varepsilon_i/d_i$, where S is the area of the MOS capacitor, and the capacitance of the active semiconductor layer C_s,

$$C_{mos} = \frac{C_i C_s}{C_i + C_s}. \tag{1.19}$$

The semiconductor capacitance can be calculated as

$$C_s = S\left|\frac{dQ_s}{d\psi_s}\right|, \tag{1.20}$$

where Q_s is the total charge density per unit area in the semiconductor and ψ_s is the surface potential. Using (1.9) to (1.12) for Q_s and performing the differentiation, we obtain

$$C_s = \frac{C_{so}}{\sqrt{2} f(\psi_s/V_{th})}\left\{1 - \exp\left(-\frac{\psi_s}{V_{th}}\right) + \frac{n_{po}}{N_a}\left[\exp\left(\frac{\psi_s}{V_{th}}\right) - 1\right]\right\}. \tag{1.21}$$

Here, $C_{so} = S\varepsilon_s/L_{Dp}$ is the semiconductor capacitance at the flat-band condition (i.e., for $\psi_s = 0$) and L_{Dp} is the Debye length given by (1.11). Equation (1.14) describes the relationship between the surface potential and the applied bias.

The semiconductor capacitance can formally be represented as the sum of two capacitances – a depletion layer capacitance C_d and a free carrier capacitance C_{fc}. C_{fc} together with a series resistance R_{GR} describes the delay caused by the generation/recombination

mechanisms in the buildup and removal of inversion charge in response to changes in the bias voltage (see following text). The depletion layer capacitance is given by

$$C_{\mathrm{d}} = S\varepsilon_{\mathrm{s}}/d_{\mathrm{d}}, \tag{1.22}$$

where

$$d_{\mathrm{d}} = \sqrt{\frac{2\varepsilon_{\mathrm{s}}\psi_{\mathrm{s}}}{qN_{\mathrm{a}}}} \tag{1.23}$$

is the depletion layer width. In strong inversion, a change in the applied voltage will primarily affect the minority carrier charge at the interface, owing to the strong dependence of this charge on the surface potential. This means that the depletion width reaches a maximum value with no significant further increase in the depletion charge. This maximum depletion width d_{dT} can be determined from (1.23) by applying the threshold condition, $\psi_{\mathrm{s}} = 2\varphi_b$. The corresponding minimum value of the depletion capacitance is $C_{\mathrm{dT}} = S\varepsilon_{\mathrm{s}}/d_{\mathrm{dT}}$.

The free carrier contribution to the semiconductor capacitance can be formally expressed as

$$C_{\mathrm{fc}} = C_{\mathrm{s}} - C_{\mathrm{d}}. \tag{1.24}$$

As indicated, the variation in the minority carrier charge at the interface comes from the processes of generation and recombination mechanisms, with the creation and removal of electron–hole pairs. Once an electron–hole pair is generated, the majority carrier (a hole in p-type material and an electron in n-type material) is swept from the space charge region into the substrate by the electric field of this region. The minority carrier is swept in the opposite direction toward the semiconductor–insulator interface. The variation in minority carrier charge at the semiconductor–insulator interface therefore proceeds at a rate limited by the time constants associated with the generation/recombination processes. This finite rate represents a delay, which may be represented electrically in terms of an RC product consisting of the capacitance C_{fc} and the resistance R_{GR}, as reflected in the equivalent circuit of the MOS structure shown in Figure 1.7. The capacitance C_{fc} becomes important in the inversion regime, especially in strong inversion where the mobile charge is important. The resistance R_{s} in the equivalent circuit is the series resistance of the neutral semiconductor layer and the contacts.

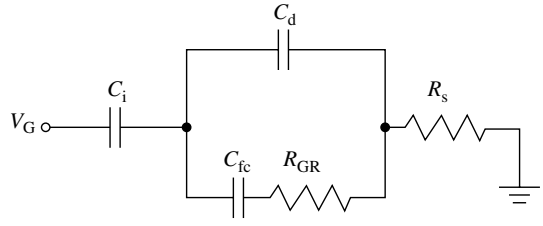

Figure 1.7 Equivalent circuit of the MOS capacitor. Reproduced from Shur M. (1990) *Physics of Semiconductor Devices*, Prentice Hall, Englewood Cliffs, NJ

This equivalent circuit is clearly frequency-dependent. In the low-frequency limit, we can neglect the effects of R_{GR} and R_s to obtain (using $C_s = C_d + C_{fc}$)

$$C^{o}_{mos} = \frac{C_s C_i}{C_s + C_i}. \tag{1.25}$$

In strong inversion, we have $C_s \gg C_i$, which gives

$$C^{o}_{mos} \approx C_i \tag{1.26}$$

at low frequencies.

In the high-frequency limit, the time constant of the generation/recombination mechanism will be much longer than the signal period ($R_{GR}C_{fc} \gg 1/f$) and C_d effectively shunts the lower branch of the parallel section of the equivalent in Figure 1.7. Hence, the high-frequency, strong inversion capacitance of the equivalent circuit becomes

$$C^{\infty}_{mos} = \frac{C_{dT} C_i}{C_{dT} + C_i}. \tag{1.27}$$

The calculated dependence of C_{mos} on the applied voltage for different frequencies is shown in Figure 1.8. For applied voltages well below threshold, the device is in accumulation and C_{mos} equals C_i. As the voltage approaches threshold, the semiconductor passes the flat-band condition where C_{mos} has the value C_{FB}, and then enters the depletion and the weak inversion regimes where the depletion width increases and the capacitance value drops steadily until it reaches the minimum value at threshold given by (1.27). The calculated curves clearly demonstrate how the MOS capacitance in the strong inversion regime depends on the frequency, with a value of C^{∞}_{mos} at high frequencies to C_i at low frequencies.

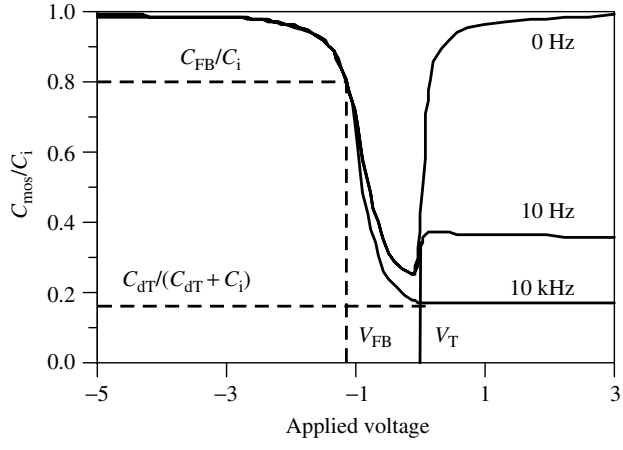

Figure 1.8 Calculated dependence of C_{mos} on the applied voltage for different frequencies. Parameters used: insulator thickness, 2×10^{-8} m; semiconductor doping density, 10^{15}/cm^3; generation time, 10^{-8} s. Reproduced from Shur M. (1990) *Physics of Semiconductor Devices*, Prentice Hall, Englewood Cliffs, NJ

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