RF CIRCUIT DESIGN

RICHARD CHI-HSI LI

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Published by John Wiley & Sons, Inc., Hoboken, New Jersey.
Published simultaneously in Canada.

ISBN 978-0-470-16758-8

Printed in the United States of America.

10 9 8 7 6 5 4 3 2 1

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PREFACE

I have worked on *RF* circuit design for more than 20 years. My motivation in writing this book is to share my *RF* circuit design experience, both successes and failures, with other readers. This book is aimed at *RF* circuit designers, and is organized into three parts, as shown in the figure.

PART I: INDIVIDUAL *RF* BLOCKS (CHAPTERS 1 TO 7)

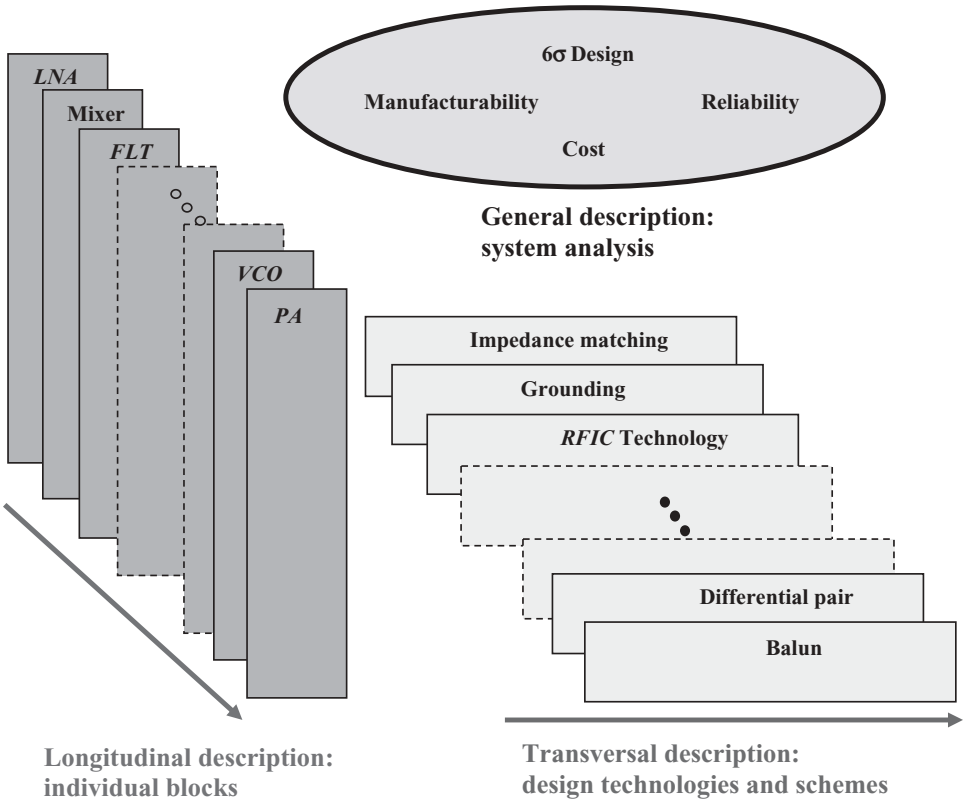
There are many good books about *RF* circuit design on the market. Their arrangement is usually longitudinal, emphasizing the operating principles of individual blocks. These individual blocks include the *LNA*, mixer, filter, *VCO, PA*, and so on.

I have followed the longitudinal pattern shown in the figure:

- *LNA* (Chapter 1);
- Mixer (Chapter 2);
- Differential pair (Chapter 3);
- Balun (Chapter 4);
- Tunable filter (Chapter 5);
- *VCO* (Chapter 6);
- *PA* (Chapter 7).

Rather than emphasizing the operating principles, I provide practical engineering design examples, most of which I designed myself.

In Chapter 1, a new design procedure is presented. During the 1990s, I found that the maximum gain and minimum noise figure can be achieved simultaneously in the *LNA* design. This has been applied in many design products in my engineering projects; however, the positive results have not been previously published. I did



Three kinds of descriptions of *RF* circuit design.

introduce them in my lectures in recent years and received encouraging responses from the audiences.

In Chapter 4, the transformer balun and *LC* balun are emphasized. In past years, I have always used the special transformer balun with a ratio of $1{:}\sqrt{2}$ in my circuitry simulations. In this special transformer balun, I found an advantage. The simulation for a circuit with a differential pair configuration can be replaced and "interpreted" by the simulation for a circuit with a single-ended configuration. In the test lab, I prefer to apply the *LC* balun because of its simplicity, ease, and reliability. I developed the design equations in 1992, and they have been applied in practical engineering designs for many years, although no papers have been presented at conferences or published.

The content of Chapter 5 is abstracted from my U.S. patent. The bandwidth of a tunable filter can be kept unchanged over the entire expected frequency range only if the main coupling element is an inductor, not a capacitor or a combination of an inductor and a capacitor. In addition, a very deep imaginary rejection "zero" can be created by a small capacitor. This work proves that the performance of individual blocks can be greatly improved by means of simple schemes, even though the tunable filter was designed by engineers some 50 years ago.

PART II: DESIGN TECHNOLOGIES AND SCHEMES (CHAPTERS 8 TO 17)

As shown in the figure, the transversal description chapters contain four elements: impedance matching (Chapters 8 to 13), grounding and current coupling (Chapters 14 and 15), *RFIC* and *SOC* (Chapter 16), and 6σ design for manufacturability of product (Chapter 17).

As per my *RF* circuit design experience, understanding the operating principles of *RF* circuit blocks is much easier than developing a 6σ design for an *RF* module or *RFIC* chip; consequently, familiarity with the four basic technologies and schemes, including impedance matching, grounding, *RFIC* and *SOC*, and 6σ design, is essential. They are the basic requirements and "must" conditions for a qualified *RF* circuit designer.

Why is impedance matching technology so important? Because

- The main task of the *RF* circuit block is power transportation or manipulation, while the main task of the digital circuit block is status transportation or manipulation.
- Power transportation or manipulation is directly related to impedance matching. The necessary and sufficient condition for optimized power transportation or manipulation is the conjugate matching of input and output impedance between the *RF* blocks.
- Consequently, impedance matching must be done for almost all *RF* blocks. The only exceptions are:
  - The output of the oscillator or *VCO* and the input of the *VCO* buffer;
  - The *IF* digital input/output of the *RF* modulator/demodulator.

Impedance matching is a challenging task in a *UWB* system today. It is the core of *RF* circuit design technologies. That is why I have devoted one third of the book to this topic. My contribution to impedance matching is the division of the Smith chart into four regions so that the impedance matching network built by two parts can be directly designed in terms of couple equations. Chapter 4, which discusses impedance matching in the wide-band case, is abstracted from my recent research work on the *UWB* system. I think that my methodology for wide-band impedance matching is unique, and, again, it has not been previously published.

Why is grounding so important? Because

- At the *RF* frequency range, a metallic surface with good conductivity is very often not equipotential.
- At the *RF* frequency range, the ground points at two ends of a good *RF* cable are in most cases not equipotential.
- Very often, return current coupling on ground surface is ignored or de-emphasized.
- In today's *RFIC* design, the "zero" capacitor is a bottleneck.

Why are the *RFIC* and *SOC* so important? Because

- Compared with *RF* module design by discrete parts, *RFIC* design has the advantages of low cost, small size, and high reliability.

- The next step in circuit design is to reach *SOC* design. However, there are many barriers to overcome.

Why is 6σ design so important? Because

- The viability of a product on a mass production line depends on its approaching 6σ design or 100% yield rate.
- Prototype circuit design in the lab is not the same as 6σ design for a product in a mass production line. There is long way to go from a prototype circuit design level up to a 6σ design goal.
- 6σ design is the necessary and satisfactory criterion to measure the qualifications of an *RF* circuit designer.

PART III: *RF* SYSTEM ANALYSIS (CHAPTER 18)

As shown in the figure, the third part of this book provides a general description of the basic parameters and the necessary theoretical background of *RF* system analysis to control the individual *RF* circuit block design.

Most of this book is a summary of my design work and therefore may reflect my own imperfect understandings and prejudices. Comments from readers will be greatly appreciated. My email address is chihsili@yahoo.com.cn.

I have found the following books and articles very helpful in my engineering design work:

Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed., John Wiley & Sons, Inc., 2001; Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998; Donald R.J. White, *Electrical Filters, Synthesis, Design and Applications*, Don White Consultants, Inc., 1980; Barrie Gilbert, "The Multi-tanh Principle: A Tutorial Overview," *IEEE* Journal of Solid-State Circuits, Vol. 33, No. 1, January 1998, pp. 2–17; and H. A. Haus et al., "Representation of Noise in Linear Two Ports," Proceedings of the *IRE*, Vol. 48, January 1960, pp. 69–74.

Finally, I express my deepest appreciation to my lovely son, Bruno Sie Li, who checked and corrected my English and designed the front cover.

Richard Chi-Hsi Li

Fort Worth, Texas
March 2008

PART I

INDIVIDUAL *RF* BLOCKS

CHAPTER 1

LNA (LOW NOISE AMPLIFIER)

1.1 INTRODUCTION

In a wireless communication system, the *LNA* is the first circuit block in the receiver. It is one of most important blocks because:

- The sensitivity of the receiver is mainly determined by the *LNA* noise figure and power gain. The noise figure of the *LNA* significantly impacts the overall noise performance of the receiver. On the other hand, the power gain of the *LNA* significantly suppresses noise contributions from subsequent stages, so that it as well impacts the overall noise performance of the receiver.
- The *LNA* plays an important role in the linearity of the entire system. Its nonlinearity must be reduced as much as possible.
- In a *CDMA* (Code Division Multiplex Access) wireless communication system, the *LNA* takes care of *AGC* (Automatic Gain Control) in the entire system as well.

This chapter covers

- Typical design procedures including selection of device size, raw device testing, input and output impedance matching, stability checking, and linearity examination and improvement. This has been important subject since the advent of more advanced wireless communication systems such as 64 *QAM*.
- Cascode *LNA*. As the wireless bandwidth is raised up to *GHz* or tens of *GHz*, the performance of the *LNA* is restricted by the input Miller capacitance. Increasing the isolation between the input and output in a *LNA* would be helpful to an advanced communication system. The cascode *LNA* would improve the performance from single-ended *LNA*.

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- *AGC* (Automatic Gain Control). Without *AGC* capability, it is impossible for the wireless *CDMA* communication system to operate well.

In recent years, the differential *LNA* is specially required for the direct conversion or "zero *IF*" wireless communication system. This will be discussed in Chapter 3, where the differential pair discussed applies not only to the differential *LNA* but also to other *RF* circuit blocks.

The *LNA* has been developed over several decades. However, as the progress of electronic products moved forward, *LNA* design was required to reach higher and higher goals. For example, the voltage of *DC* power supply became lower and lower, from $3V$ to $1V$ in a cellular phone design. The current drain had to be reduced as much as possible so that the standby current of the overall receiver could be just a few mA to conserve battery consumption. It must be small and the cost must be low, and the performance must be maintained at a high level. *LNA* design becomes more complicated if trade-offs must be made between size, cost, and performance.

It is well known that the *LNA* must magnify the weak signal from the antenna and intensify it up to the power level required by subsequent stages. This implies that a *LNA* must have

- A low noise block so that the weak signal will not be "submerged" by noise;
- A high power gain block so that its output can drive the following stage well.

A *LNA* with maximum gain may not be in the state of minimum noise, or vice versa. A trade-off is usually made between maximizing gain and minimizing the noise figure. In past decades, much effort has been put into designing a *LNA* to reach both maximum gain and minimum noise figure simultaneously. This is a great challenge in *LNA* circuit design. This dilemma was solved more than 10 years ago in my designs but has not been previously published. Now I am going to share it with my readers.

1.2 SINGLE-ENDED SINGLE DEVICE *LNA*

In this section, the design procedures and schemes will be illustrated through a design example, in which a *MOSFET* transistor is selected as the single-ended device (it can of course be replaced by other types of devices).

A single-end *LNA* with a single device is the simplest low noise amplifier. Nevertheless, it is the essence or core in all other types of *LNA* designs, including cascode and differential designs. The design procedures and schemes described in this section are suitable to all types of *LNA* design.

The main goals for the design example are

- $V_{cc} = 3.0\,V$,
- $I_{cc} < 3.0\,mA$,
- frequency range = 850 to $940\,MHz$,
- $NF < 2.5\,dB$,
- gain $> 10\,dB$,

- $IP_3 > 0\,dBm$,
- $IP_2 > 40\,dBm$.

1.2.1 Size of Device

The first step in *LNA* circuit design is to decide the size of the device. Many trade-offs must be taken into account between size, cost, performance, and so on. In this sub-section, only performance is counted in the selection of device size.

In digital *IC* circuit design, the *MOSFET* transistor has become dominant in recent years because the size of the device can be shrunk and the current drain can be reduced more than with other devices. Among *MOSFET* transistors, device length therefore becomes the key parameter in the selection of *IC* foundry and processing because it strongly impacts the total area of the *IC* die and therefore the cost, speed of performance, maximum data rate, current drain, and so on. The reason is simple: In digital *IC* circuit design, hundreds and even thousands of transistors are needed. The total area of the *IC* die, and therefore the cost, is significantly reduced as the device length decreases. *IC* scientists and engineers have worked very hard to shrink the size of transistors, which now approach unbelievably tiny sizes. In the 1990s, the length of a *MOSFET* device was in the order of μm; from 2000 to 2005 and the *IC* world entered the so-called "nanometers" era. Many foundries today have the capability to manufacture *MOSFET IC*s with lengths of 0.5, 0.35, 0.25, 0.18, $0.11\,\mu m$. In 2006, the length of a *MOSFET* device was further shrunk to 90, 45, $22.5\,nm$. The progress of *IC* processing is moving forward very fast, and, consequently, *IC* circuit design work becomes more and more challenging.

In the *RF* circuit design, bipolar transistors were applied to *RFIC* development in the 1990s. Meanwhile, the *MOSFET* device has been applied to the *RFIC* as well. The smaller size of *MOSFET* devices brings about the same advantages to *RF* circuit design as to digital circuit design, such as the reduction of cost and the increase in operating frequencies. It must be pointed out, however, that smaller size is not the main objective pursued in *RF* circuit design because the total number of devices applied in *RF* circuits is much smaller than the number of devices applied in digital circuits. Instead of pursuing smaller size, *RF* engineers prefer to select device lengths for which the technology of *IC* processing in the foundry is more advanced and the device model for simulation is more accurate. In addition, there are two important factors to be considered in the selection of the *MOSFET* device's size: the restriction of the device size due to the V_{gs} limitation and another due to the expectations of NF_{min}.

1.2.1.1 Restrictions of W/L *Due to Consideration of* V_{gs}

In *LNA* design, the *MOSFET* transistor is usually operated in its active region. Its *DC* characteristics can be expressed as:

$$I_d = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{gs} - V_{th})^2, \tag{1.1}$$

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th}), \tag{1.2}$$

where

I_d = drain current,
g_m = transconductance of *MOSFET* transistor,
W = width of *MOSFET* transistor,
L = length of *MOSFET* transistor,
V_{gs} = gate-source voltage for n channel *MOSFET*,
V_{th} = threshold voltage for n channel *MOSFET*, the minimum gate-to-source voltage needed to produce an inversion layer beneath the gate,
V_{ds} = drain-source voltage for *n* channel *MOSFET*,
μ_n = channel mobility, typically $700\,cm^2/V\text{-}sec$,
C_{ox} = capacitance per unit area of the gate oxide,

and

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \tag{1.3}$$

where

t_{ox} = thickness of the gate oxide.

From (1.1) and (1.2) we have

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_d}\,. \tag{1.4}$$

$$V_{gs} = 2\frac{I_d}{g_m} + V_{th}. \tag{1.5}$$

Equation (1.4) shows that g_m is related to the ratio W/L. The increase of the ratio W/L is equal to the increase of g_m. On the other hand, from equation (1.5), it can be seen that there are two ways to make I_d reach a certain amount, either by increasing g_m through the increase of the ratio W/L for a given V_{gs} or by increasing V_{gs} through the factor of $(V_{gs}\text{-}V_{th})$. Should the selected value of the ratio W/L be too small, V_{gs} must be increased to an unacceptable value for a given I_d.

In order to illustrate the relationships between g_m, I_d, W/L and the corresponding values of V_{gs}, Table 1.1 lists the calculated V_{gs} values when I_d and the ratio W/L are selected in different levels or amounts and when the basic parameters applied in the calculations are assumed as follows:

$$\varepsilon_{ox} = 3.45\times10^{-13}\ F/cm, \tag{1.6}$$

$$t_{ox} = 23.3\ A^{\circ} = 23.3\times10^{-8}\ cm, \tag{1.7}$$

$$\mu_n = 170\ \ cm^2/V\text{-}sec, \tag{1.8}$$

$$C_{ox} = 14.81\ fF/\mu^2, \tag{1.9}$$

$$V_{tn} = 0.49\,V, \tag{1.10}$$

TABLE 1.1 V_{gs} **limitation in the selection of device size**

I_d **(mA)**	W (μm)	L (μm)	**W/L**	g_m **(mA/V)**	V_{gs} (V)
1.00	0.9	0.09	**10.00**	**2.24**	**1.38**
1.00	9	0.09	**100.00**	**7.10**	**0.77**
1.00	90	0.09	**1000.00**	**22.44**	**0.58**
1.00	180	0.09	**2000.00**	**31.73**	**0.55**
1.00	450	0.09	**5000.00**	**50.17**	**0.53**
1.00	900	0.09	**10000.00**	**70.95**	**0.52**
1.00	1800	0.09	**20000.00**	**100.34**	**0.51**
2.00	0.9	0.09	**10.00**	**3.17**	**1.75**
2.00	9	0.09	**100.00**	**10.03**	**0.89**
2.00	90	0.09	**1000.00**	**31.73**	**0.62**
2.00	180	0.09	**2000.00**	**47.79**	**0.58**
2.00	450	0.09	**5000.00**	**70.95**	**0.55**
2.00	900	0.09	**10000.00**	**100.34**	**0.53**
2.00	1800	0.09	**20000.00**	**141.91**	**0.52**
5.00	0.9	0.09	**10.00**	**5.02**	**2.48**
5.00	9	0.09	**100.00**	**15.87**	**1.12**
5.00	90	0.09	**1000.00**	**50.17**	**0.69**
5.00	180	0.09	**2000.00**	**75.56**	**0.63**
5.00	450	0.09	**5000.00**	**11.19**	**0.58**
5.00	900	0.09	**10000.00**	**158.66**	**0.55**
5.00	1800	0.09	**20000.00**	**224.37**	**0.53**
10.00	0.9	0.09	**10.00**	**7.10**	**3.31**
10.00	9	0.09	**100.00**	**22.44**	**1.38**
10.00	90	0.09	**1000.00**	**70.95**	**0.77**
10.00	180	0.09	**2000.00**	**106.86**	**0.69**
10.00	450	0.09	**5000.00**	**158.66**	**0.62**
10.00	900	0.09	**10000.00**	**224.37**	**0.58**
10.00	1800	0.09	**20000.00**	**317.31**	**0.55**
20.00	0.9	0.09	**10.00**	**10.03**	**4.48**
20.00	9	0.09	**100.00**	**31.73**	**1.75**
20.00	90	0.09	**1000.00**	**100.34**	**0.89**
20.00	180	0.09	**2000.00**	**151.13**	**0.77**
20.00	450	0.09	**5000.00**	**224.37**	**0.67**
20.00	900	0.09	**10000.00**	**317.31**	**0.62**
20.00	1800	0.09	**20000.00**	**448.75**	**0.58**
50.00	0.9	0.09	**10.00**	**15.87**	**6.79**
50.00	9	0.09	**100.00**	**50.17**	**2.48**
50.00	90	0.09	**1000.00**	**158.66**	**1.12**
50.00	180	0.09	**2000.00**	**238.95**	**0.94**
50.00	450	0.09	**5000.00**	**354.77**	**0.77**
50.00	900	0.09	**10000.00**	**501.71**	**0.69**
50.00	1800	0.09	**20000.00**	**709.53**	**0.63**

then

$$\mu_n C_{ox} = 251.72\ \mu A/V^2. \tag{1.11}$$

In Table 1.1, the calculations are conducted for the cases of $I_d = 1, 2, 5, 10, 20$, and $50\,mA$ with the different levels of $W/L = 10, 100, 1000, 2000, 5000, 10\,000$, and $20\,000$.

The underlined values of V_{gs} in the rightmost column in Table 1.1 are unacceptable because they are higher than $0.7V$, which is considered the highest acceptable value of V_{gs} when the DC power supply is low, say, 1.0 to $1.8\,V$. Therefore, the rows containing underlined values of V_{gs} in Table 1.1 must be abandoned in the selection of the ratio W/L. Hence, the values of the ratio W/L are restricted for the given values of I_d and g_m due to the constraint on V_{gs}. All other rows and their candidates in Table 1.1 are acceptable. They will be further narrowed down in consideration of the so-called "power-constrained noise optimization."

It should be noted that Table 1.1 is an example only. The selection of the ratio W/L for the device must be conducted by designers based on the basic parameters, ε_{ox}, t_{ox}, μ_n, C_{ox}, and V_{tn}, which actually apply to the device.

1.2.1.2 Optimum Width W_{opt} of Device

Based on the theoretical derivation (Lee, 1998, pp. 230–232), the size selected for the device in *LNA* design is more reasonably considered from the expectation of a minimum of noise. By explicitly taking power consumption into account, the optimum width of a device W_{opt} for the minimum noise figure NF_{min} can be expressed as

$$W_{opt} = \frac{1}{3\omega L C_{ox} R_S}, \tag{1.12}$$

where

W_{opt} = optimum width of device (*MOSFET* transistor),
ω = operation angular frequency,
L = length of device (*MOSFET* transistor),
C_{ox} = capacitance per unit area of the gate oxide,
R_S = source resistance.

This results from the power-constrained noise optimization.

The value of the optimized width of the device is inversely proportional to the operating frequency, ω, the source resistance, R_S, the capacitance of the gate oxide area, C_{ox}, and the length of the device, L. The designer knows the first two parameters, ω and R_S. The other two, C_{ox} and L, are provided by the *IC* foundry, which may have a couple choices. For instance, device lengths of 0.25, 0.18, 0.13, 0.11, and $0.09\,\mu m$, are available in most *MOS IC* foundries at present. Based on the data that the *IC* foundry provides, the corresponding values of W_{opt} can be calculated from equation (1.12). Then, these W_{opt} and L values can be examined for a reasonable value of V_{gs} as in Table 1.1 and the best set of W_{opt} and L can be determined. Then, the final decision of *IC* processing can be made.

1.2.2 Raw Device Setup and Testing

Raw device testing is the second step in the block circuit design. It should be noted that it is a key step in a good LNA circuit design.

In the circuit design, a "device" is a general name for a transistor. The transistor can be bipolar, or a *MOSFET*, or GaAs, or some other type. The purpose of raw

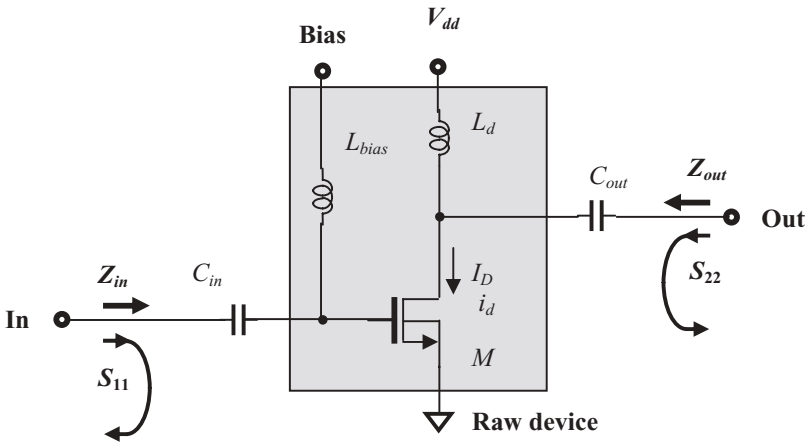


Figure 1.1 Setup for raw device testing, f = 850 to 940 MHz, $I_D = 2.6\,mA$$C_{in}$, C_{out}: "zero" capacitor; L_{bias}, L_c, L_d: "infinite" inductor.

device testing is to determine the operating characteristics only of the device, and nothing else. However, an operating transistor must be provided with the *DC* power supply and bias, and therefore, some additional parts such as the *RF* choke and *DC* blocking or *AC* by-pass capacitors must be connected. The impedance of the additional parts must therefore approach either zero when they are connected in series, or infinity when they are connected in parallel. If so, the tested characteristics of the transistor are not disturbed by the addition of those parts.

Figure 1.1 shows the setup for raw device testing. The capacitors C_{in} and C_{out} are "zero" capacitors, while the inductors L_{bias} and L_d are "infinite" inductors. They are discussed in Chapter 14 where the "zero" capacitor and "infinite" inductor are selected from discrete chip parts. In the actual simulation for *IC* circuitry, the capacitors C_{in} and C_{out} can be large capacitors with a high value of capacitance so that their impedance approaches zero at operating frequencies, while the inductors L_{bias} and L_d can be a large inductors with a high value of inductance so that their impedance approaches infinity at operating frequencies. The desired current drain of the transistor, $I_D + i_d$, can be adjusted by the bias voltage, where I_D is the *DC* current drain portion and i_d is the *AC* current drain portion of the *MOSFET* transistor.

In Figure 1.1, the device is a *MOSFET* transistor with *CMOS IC* processing. Its size has been selected based on the considerations of V_{gs} and NF_{min} as discussed in the previous section. As mentioned above, the *DC* power supply is $3V$ and the drain current, adjusted by the bias, is $2.6\,mA$.

The operating frequency range is from 850 to 940 MHz. Its relative bandwidth is

$$\frac{\Delta f}{f_o} = \frac{940 - 850}{(940 + 850)/2} = 10.05\%. \tag{1.13}$$

This is a narrow-band block. Usually, a block or a system with a relative bandwidth greater than 15% is considered a wide-band block or system. A block or a system

with a relative bandwidth less than 15% is considered a narrow-band block or system.

The purpose of raw device testing is twofold:

1) To create a starting point for impedance matching in order to continue the next design step.
2) To see if the raw device can approach a good *LNA* design. A good *LNA* design suggests that a minimum of noise and a maximum of gain can be obtained simultaneously.

It is easy to understand that the first purpose of raw device testing is to create a starting point for matching input and output impedance. The input and output impedances, Z_{in} and Z_{out}, are approximately related to the S parameters by the following equations:

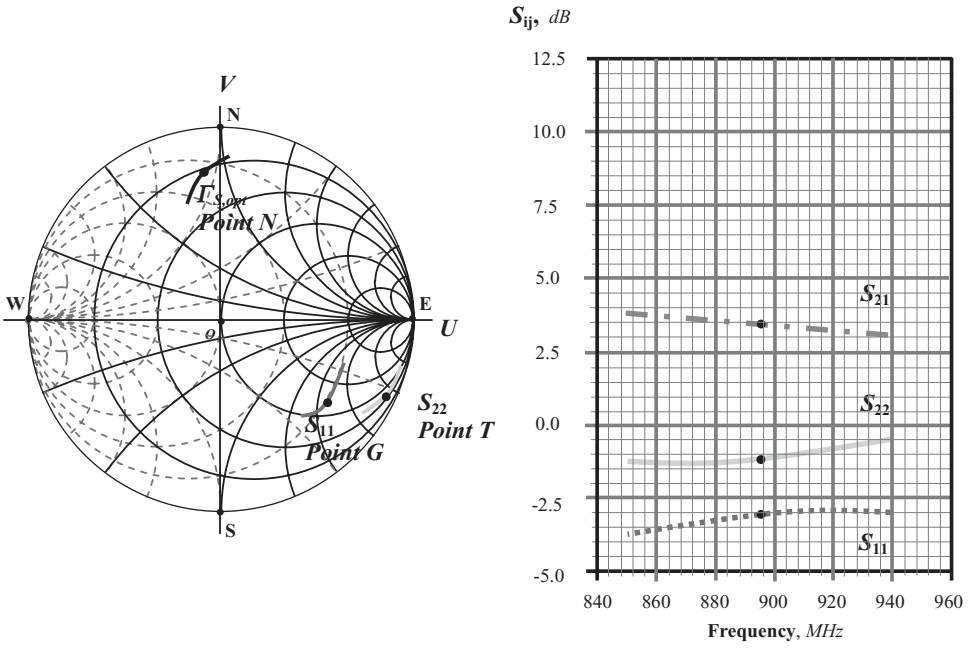
$$Z_{in} = \frac{1+S_{11}}{1-S_{11}}, \tag{1.14}$$

$$Z_{out} = \frac{1+S_{22}}{1-S_{22}}. \tag{1.15}$$

This approximation is usually correct if the transistor's isolation between input and output is good and the testing calibration is well done. Through the testing of S_{11} and S_{22}, the input and output impedances, Z_{in} and Z_{out}, can be read directly from the Smith chart at the same locations of S_{11} and S_{22}, respectively.

Figure 1.2(a) shows the test results of S_{11} and S_{22}, and hence Z_{in} and Z_{out} on the Smith chart. The input and output impedances of a *MOSFET* transistor are usually capacitive and are located in the bottom half of the Smith chart, while the input and output impedances of a bipolar transistor can be either capacitive or inductive, depending on the device size, current drain, and operating frequency. Another difference between the *MOSFET* and the bipolar transistor is that the input and output impedances of a *MOSFET* transistor are usually located in the relatively higher impedance area, while the input and output impedances of a bipolar transistor are usually located in the relatively lower impedance area. This difference implies that impedance matching is more difficult for the *MOSFET* than for the bipolar transistor, and that the isolation between input and output in the *MOSFET* is better than in the bipolar transistor.

Figure 1.2(a) also shows that the location of S_{22} is much farther from $50\,\Omega$ and is in the very high impedance area, while S_{11} is located somewhat closer to $50\,\Omega$ than S_{22}. Correspondingly, Figure 1.2(b) shows that the magnitude of S_{22} is almost close to $-1\,dB$, of S_{11} around $-3\,dB$, and of S_{21} around $3.5\,dB$, which is much lower than expected. We do not mind S_{21} too much because it is tested under an unmatched case. The magnitude of S_{12} is usually around -20 to $-30\,dB$ and therefore disappears from the plot. Likewise, we do not mind S_{12} too much because the isolation in today's devices is usually sufficient unless a feedback circuit is added. A remarkable feature shown in Figure 1.2 is that the frequency response for all the S parameters is flattened, so that one does not need to worry about bandwidth at this point.



(a) S_{11}, S_{22} and $\Gamma_{S,opt}$ on Smith chart (b) Magnitude of S_{ij}, *dB*

Figure 1.2 *S* parameters from raw device testing, f = 850 to 940 MHz, I_D = 2.6 mA. (The intermediate frequency 895 MHz is marked with a dot on each trace.)

The second purpose of raw device testing is to examine the performance of the noise figure.

Based on Haus's theory (1960), the noise figure of a noisy block can be expressed by

$$NF = NF_{\min} + \frac{R_n}{G_s}\left[(G_S - G_{S,opt})^2 + (B_S - B_{S,opt})^2\right]. \tag{1.16}$$

where

NF = noise figure of noisy block,
NF_{min} = minimum of noise figure of noisy block,
R_n = equivalent noise resistance,
Y_S = admittance of input source,
G_S = conductance of input source,
B_S = subceptance of input source,
$Y_{S,opt}$ = optimum admitttance of input source,
$G_{S,opt}$ = optimum conductance of input source,
$B_{S,opt}$ = optimum subceptance of input source.

The noisy two-port block can reach a minimum of noise figure

$$NF = NF_{\min}, \tag{1.17}$$

when

$$G_S = G_{S,opt}, \tag{1.18}$$

$$B_S = B_{S,opt}. \tag{1.19}$$

Equations (1.18) and (1.19) can be written together, that is

$$Y_S = Y_{S,opt}, \tag{1.20}$$

where

$$Y_s = G_s + jB_s \tag{1.21}$$

$$Y_{S,opt} = G_{S,opt} + jB_{S,opt} \tag{1.22}$$

On the Smith chart, the optimum condition (1.20) is usually labeled by the corresponding reflection coefficient, $\Gamma_{\text{S,opt}}$, corresponding to $Y_{S,opt} = G_{S,opt} + \text{j}\ B_{S,opt}$,

$$\Gamma_S = \Gamma_{S,opt}. \tag{1.23}$$

Of course, $\Gamma_{\text{S,opt}}$ is a complicated function mainly determined by the type, size, and trans-conductance of the raw device. It has been formularized in some technical books. Usually, an optimum source reflection coefficient, $\Gamma_{\text{S,opt}}$, is computed by the computer simulation program and can be displayed on the Smith chart as shown in Figure 1.2(a). On the Smith chart, its corresponding parameters, G_{opt}, B_{opt}, R_{opt}, X_{opt}, can be read from the same point.

Noise figure would be expected to be at a minimum if the input impedance were at point N where its input impedance corresponds to $\Gamma_{\text{S,opt}}$. Instead, in raw device testing, the noise figure is tested at point G where its impedance corresponds to its S_{11}. Therefore its value is much higher than the expected minimum. Figure 1.3 shows the tested noise figure. In the entire frequency range, it is around $8.7\,dB$.

At this point, a question may be raised: Through impedance matching, the trace S_{11} can be pulled to $50\,\Omega$, the center of the Smith chart. What would happen to the trace of $\Gamma_{\text{S,opt}}$ then? We expect that the trace of $\Gamma_{\text{S,opt}}$ would also be pulled to $50\,\Omega$, the center of the Smith chart. Can we control the change of the trace of $\Gamma_{\text{S,opt}}$ when the impedance matching network is implemented?

Let's take a look at the performance of the noise figure (*NF*) in the entire frequency range from the raw device testing. Figure 1.3 shows that the noise figure in the operating frequency range is

$$NF = 8.52 \text{ to } 8.77\,dB, \qquad \text{when } 850\,MHz < f < 940\,MHz, \tag{1.24}$$

$$NF = 8.7\,dB, \qquad \text{when} \qquad f = 895\,MHz. \tag{1.25}$$

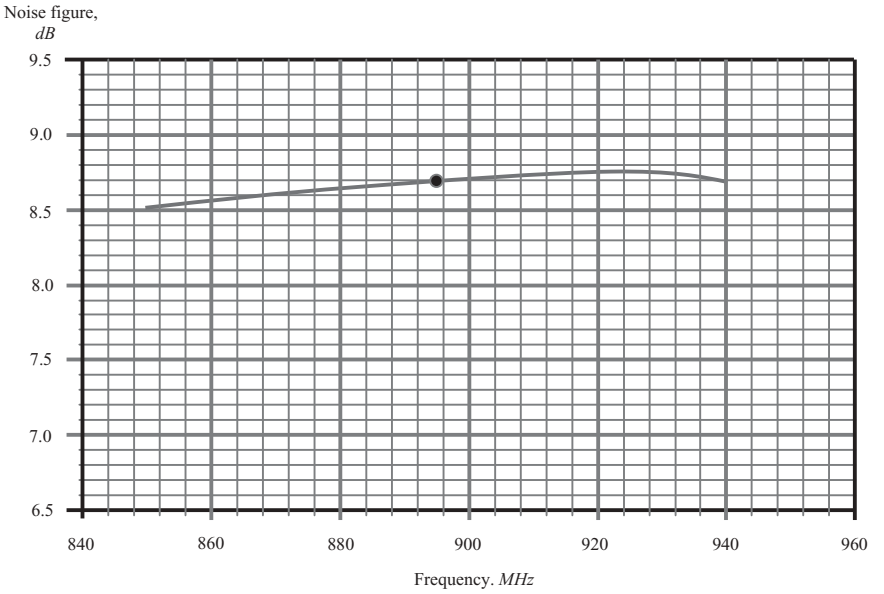


Figure 1.3 Noise figure from 850 to 940 MHz. $I_D = 2.6\,mA$, $NF = 8.7\,dB$ when $f = 895\,MHz$.

The goal is

$$NF < 2.5\,dB, \qquad \text{when } 850\,MHz < f < 940\,MHz. \tag{1.26}$$

It can be seen that in the entire operating frequency range the noise figure is unacceptable.

Now let's examine the gain circles and noise figure circles at one frequency, say, $f = 895\,MHz$, on the input reflection coefficient plane. Figure 1.4 plots both the gain circles and noise figure circles together.

The maximum of gain, $G = G_{max}$, is located at point G, which is $3.0\,dB$, as shown in Figure 1.2(b). However, its noise figure does not reach its minimum $NF_{min} = 5\,dB$ as shown at point N, that is,

At point G,

$$G = G_{max} = 3.0\,dB, \quad \text{and} \quad NF = 8.7\,dB. \tag{1.27}$$

The minimum of the noise figure, $NF = NF_{min}$, is located at point N, which is quite far from point G. Its gain is, of course, much lower than the maximum gain of $3\,dB$ at point G, that is,

At point N,

$$G = -4.8\,dB, \quad \text{and} \quad NF = NF_{min} = 5\,dB. \tag{1.28}$$

The raw device would be operating at point O, the center of the Smith chart, instead of at point G or N, if the internal impedance of the signal source is $50\,\Omega$. Its gain would be higher than $-4.8\,dB$ but lower than $3.0\,dB$, while its noise figure would be

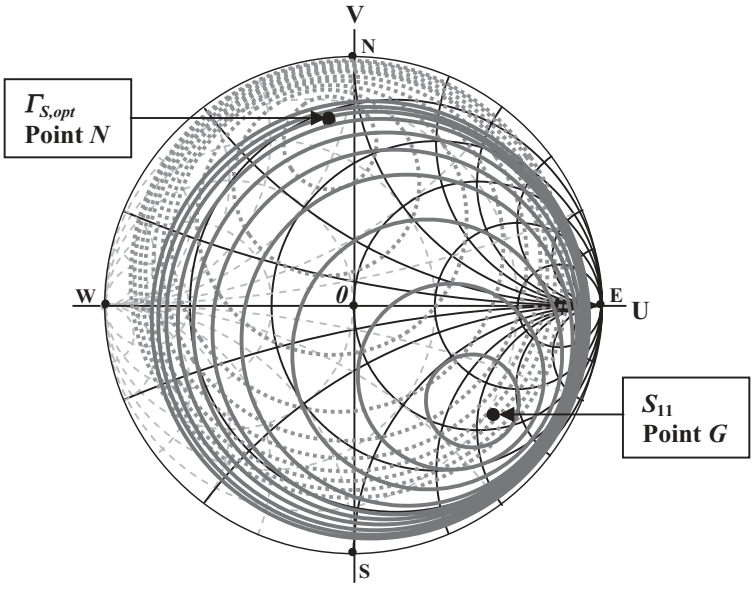


Figure 1.4 Constant gain circles and constant noise figure circles when $f = 895\,MHz$.
Gain circles: $G_{max} = 3.0\,dB$ at point G, step = $-1.0\,dB$.
Noise figure circles: $NF_{min} = 5\,dB$ at point N, step = $0.5\,dB$.

lower than $8.7\,dB$ but higher than $5\,dB$. As a matter of fact, the raw device can be operated with any source impedance. Therefore its impedance can be correspondingly adjusted to any point on the Smith chart. The actual values of gain and noise figure can be read from Figure 1.4. These gains will not be higher than $3.0\,dB$, and the noise figures will not be lower than $5\,dB$. The ideal case is to find a raw device in which the maximum of gain, G_{max}, and the minimum of noise figure, NF_{min}, come together at one point on the Smith chart. This seems almost impossible without a special scheme being involved. However, we should ask the following questions: Might this be a temporary outcome because the design work is in the preliminary stage? The next step is to build the input and output impedance matching networks based on the raw device testing. Is it possible to pull points G and N together after the input impedance matching network is built?

We will temporarily submit the noise figure to the will of heaven, take care of the gain only, and move on to the task of input and output impedance matching as shown in Figure 1.5.

Impedance matching is a special scheme and the key technology in *RF* circuit design. It is discussed in some detail in this book. Because there are many ways to do impedance matching, many different results can be found. Figure 1.6 shows one such result. The point G of maximum gain, along with its gain circles, is moved from its original high impedance location as shown in Figure 1.4 to a location near the center of the Smith chart, $50\,\Omega$. The maximum of gain is increased from the $3.0\,dB$ of Figure 1.4 to $13\,dB$ as a result of the impedance matching. However, its