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On-chip High-Voltage Generator Design

Design Methodology for Charge Pumps

Second Edition

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To the memory of my family

Preface

Accordingly, as silicon technology has been advanced, more and more functionalities have been integrated into LSIs. On-chip multiple voltage generation is becoming one of big challenges on circuit and system design. Linear or series regulator is used to convert the external supply voltage into lower and more stable internal voltages. As the number of gates operating simultaneously and the operation frequency increase, AC load current of the regulators also increases. Low-voltage operation and rapid load regulation are becoming design challenges for the voltage down convertors. Another type of voltage generator is high-voltage generator or voltage multiplier whose output is higher than the input supply voltage. The voltage multipliers are categorized into two, switching convertor and switched capacitor, with respect to the components used. The former uses an inductor, switch or diode, and AC voltage source whereas the latter uses a capacitor instead of the inductor. Even though the switching convertor has been widely used with discrete chip inductor(s) and capacitor(s), there is little report on implementation of an inductor into ICs because of too low quality factor for large inductance fabricated in current silicon technology. This book aims at discussing thorough high-voltage generator design with the switched-capacitor multiplier technique.

The First Edition has focused on integrated DC-DC voltage multipliers where the DC supply voltage is nominally greater than 1.5 V. In the Second Edition, the design of AC-DC charge pump has been added for those who are interested in the design of RFID and energy harvesting where AC input needs to be transformed into DC. In addition to the new topic, the relationship between output voltage and output current of a charge pump has been updated to be available in wide frequency range with three different conditions of switching devices; (1) diodes, (2) MOSFETs in saturation region, and (3) MOSFETs in triode region. Thus, each I-V equation includes slow to fast switching limit, which would be beneficial to those who worked on research and development of extremely low voltage LSI design. Furthermore, major revisions on DC-DC voltage multipliers have been also made to expand the circuit theories for understanding of power efficiency and for comprehensive design of the system including DC energy transducer and charge pump.

The switched-capacitor multiplier techniques originated with H. Greinacher using a voltage doubler structure for measuring the intensity of ionizing radiation in 1919, E. O. Marx using serial-parallel cells for an impulse voltage generator in 1924, and Cockcroft–Walton using serial capacitor ladders for their experiments on nuclear fission and fusion in 1932. Dickson qualitatively pointed out that the Cockcroft–Walton multiplier had too high sensitivity on parasitic capacitance to realize on-chip multipliers and then theoretically and experimentally showed that the parallel capacitor ladders realized on-chip high-voltage generation for programming Metal–Nitride–Oxide–Semiconductor (MNOS) nonvolatile memory in 1976.

After Dickson's demonstration, on-chip high-voltage generator has been implemented on Flash memories and LCD drivers and the other semiconductor devices. Accordingly, as the supply voltages of these devices become lower, it gets harder to realize small circuit area, high accuracy, fast ramp rate, and low power at a low supply voltage. This book provides various design techniques for the switched-capacitor on-chip high-voltage generator including charge pump circuits, pump regulators, level shifters, voltage references, and oscillators. The charge pump inputs the supply voltage and a clock, which is generated by the oscillator, and outputs a voltage higher than the supply voltage or a negative voltage. The pump regulator enables the charge pump when the absolute value of the output voltage of the charge pump is lower than the target voltage on the basis of the reference voltage or disables it otherwise. The generated high or negative voltage is transferred to a load through high- or low-level shifters. Chapter 1 surveys system configuration of the on-chip high-voltage generator.

Chapter 2 reviews various topologies of voltage multipliers. Since the charge pump was invented in 1919, various types have been proposed. After several typical types of charge pumps are reviewed, they are compared in terms of the circuit area and the power efficiency. The type that Dickson proposed is found to be the best one as an on-chip generator.

Chapter 3 discusses DC-DC Dickson charge pump. Design equations and equivalent circuit models are derived for the charge pump. Three types of charge transfer gate are considered; switching diode and switching MOSFET in saturation and triode region. Using the model, optimizations are discussed to minimize the circuit area under the condition that the output current or the ramp time is given and to minimize the power dissipation under the condition that the output current is given theoretically. Guideline for comprehensive optimum design is summarized.

Chapter 4 describes AC-DC Dickson charge pump. Two types of AC input are considered; continuous wave with a single frequency and multi-sine wave with multiple frequencies. An analytical, closed-form AC-DC charge pump voltage multiplier model is described to show the dependency of output current and input power on circuit and device parameters for continuous wave AC-DC charge pump. Then, it is expanded for multi-sine wave AC-DC charge pump. Analysis enables circuit designers to estimate circuit parameters, such as the number of stages and capacitance per stages, and device parameters such as saturation current (in the case of diodes) or transconductance (in the case of MOSFETs). In addition, design

optimizations and the impact of AC power source impedance on output power are investigated.

Chapter 5 overviews actual charge pumps composed of capacitors and transfer transistors. Realistic design needs to take parasitic components such as parasitic capacitance at each of both terminals and threshold voltages of the transfer transistors into account. In order to decrease the pump area and to increase the current efficiency, some techniques such as threshold voltage canceling, stage reconfiguration, and faster clocking are presented. Since the supply current has a frequency component as high as the operating clock, noise reduction technique is another concern for pump design. In addition to design technique for individual pump, system level consideration is also important, since there are usually more than one charge pump in a chip. Area reduction can be also done for multiple charge pump system where all the pumps do not work at the same time.

Chapter 6 is devoted to individual circuit block to realize on-chip high-voltage generator. Section 6.1 presents pump regulator. The pump output voltages need to be varied to adjust them to the target voltages. This can be done with the voltage gain of the regulator or the reference voltage changed. The voltage divider which is a main component of the regulator has to have small voltage coefficient and fast transient response enough to make the controlled voltage linear to the trim and stable in time. A regulator for a negative voltage has a circuit configuration different from that for a positive voltage. State of the art is reviewed.

Section 6.2 surveys level shifters. The level shifter shifts the voltage for logic high or low of the input signal to a higher or lower voltage of the output signal. Four types of level shifters are discussed (1) high-level NMOS level shifter, (2) high-level CMOS level shifter, (3) high-voltage depletion NMOS + PMOS level shifter, and (4) low-level CMOS level shifter. The trade-offs between the first three high-voltage shifters are mentioned. The negative voltage can be switched with the low-level shifter. As the supply voltage lowers, operation margins of the level shifters decrease. As the supply voltage lowers, the switching speed becomes slower, eventually infinite, i.e., the level shifter does not work. Some design techniques to lower the minimum supply voltage at which the level shifters are functional are shown.

Section 6.3 deals with oscillators. Without an oscillator, the charge pump never works. In order to make the pump area small, process, voltage, and temperature variations in oscillator frequency need to be minimized. There is the maximum frequency at which the output current is maximized. If the oscillator is designed to have the maximum frequency under the fastest conditions such as fast process corner, high supply voltage, and low temperature, the pump output current is minimum under the slowest condition such as slow process, low supply voltage, and high temperature. It is important to design the oscillator with small variations for squeezing the pump area.

Section 6.4 provides voltage references. Variations in regulated high voltages increase by a factor of the voltage gain of the regulators from those in the reference voltages. Reduction in the variations of the voltage references is a key to make the

high generated voltages well controlled. Some innovated designs for low supply voltage operation are presented as well.

Chapter 7 provides high-voltage generator system design. Multiple pumps are distributed in a die, each of which has sufficiently wide power ground bus lines. Total area including the charge pump circuits and the power bus lines needs to be paid attention for overall area reduction. Design methodology in this regard is shown using an example. Another concern on multiple high voltage generator system design is system level simulation time. Even though the switching pump models are used for the verification, simulation run time is still slow especially for Flash memory where the minimum clock period is 20–50 ns whereas the maximum erase operation period is 1–2 ms. In order to drastically reduce the simulation time, another charge pump model together with a regulator model is presented which makes all the nodes in the regulation feedback loop analogue to eliminate the hard-switching operation. Design and verification flow of integrated high-voltage generator system is summarized.

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Contents

Abbreviations

AC	Alternate current
bjt	Bipolar junction transistor
BL	Bit-line
C	Capacitance of a pump capacitor
C_B	Parasitic capacitance at the bottom plate of a pump capacitor
clk	Clock
C_{OUT}	Total capacitance of pump capacitors
C_T	Parasitic capacitance at the top plate of a pump capacitor
CW	Cockcroft–Walton pump or continuous wave
DC	Direct current
eff	Current efficiency
FET	Field effect transistor
FIB	A type of pump whose V_{MAX} is associated with a Fibonacci number Fib(N) where N is the number of stages
FSL	Fast switching limit
G_{MAX}	Maximum voltage gain
G_V	Voltage gain
I_B	Base current
IC	Integrated circuit
I_C	Collector current
I_{DD}	Supply current
I_{DS}	Drain to source current
I_{IN}	Input current
I_L	Load current
I_{LOAD}	Load current
I_{OUT}	Output current
I_{PP}	Output current of a positive voltage pump at V_{OUT} of V_{PP}
I_{REG}	Regulator current
ISM	Industry – Science – Medical
K(N)	4-Port K-matrix of N-stage pump

LCD	Liquid crystal device
LED	Light emitting device
LIN	A type of pump whose V_{MAX} is linear to the number of stages
LSI	Large scale IC
MNOS	Metal nitride oxide semiconductor
MOS	Metal oxide semiconductor
MS	Multi-sine
N	Number of stages
N_{MIN}	Minimal number of stage
N_{OPT}	Optimum number of stages
opamp	Operational amplifier
P_{IN}	Input power
P_{OUT}	Output power
PV	Photovoltaic
PVT	Process, voltage, and temperature
Q_{DD}	Total input charge
qout	Output charge per period
RFID	Radio frequency identification
R_{LOAD}	Resistance of a load circuit
R_{PMP}	Output impedance of a pump
R_{PWR}	Parasitic resistance of power and ground lines
SC	Switched-capacitor
SP	Serial-parallel
SRC	Source
SSL	Slow switching limit
T	Clock period of a pump driver clock or temperature
TEG	Thermoelectric generator
T_{OFF}	The period when a switch is being turned off
T_{ON}	The period when a switch is being turned on
UHF	Ultrahigh frequency
UPS	Utility Power Satellite
V_{BB}	Negative output voltage of a charge pump
V_{BE}	Base to emitter voltage
V_{BGR}	Band-gap reference voltage
V_{BL}	Bit-line voltage
V_{BS}	Bulk to source voltage
V_{BV_CAP}	Breakdown voltage of a capacitor
V_{BV_SW}	Breakdown voltage of a switch
V_{CAP}	Capacitor voltage
V_D	Drain voltage
V_{DD}	Supply voltage
V_{DD_LOCAL}	Supply voltage at a local interconnection node
V_{DD_MIN}	Minimum operating supply voltage
V_{DS}	Drain to source voltage
V_G	Gate voltage or voltage gain given by $V_{DD} - V_T$

V_{GS}	Gate to source voltage
V_{IN}	Input voltage
V_k	k-th nodal voltage
V_{MAX}	Maximum attainable voltage
V_{MOD}	Modulation voltage
V_{MON}	Monitored voltage
V_{OD}	Overdrive voltage
V_{OS}	Offset voltage
V_{OUT}	Output voltage
V_{PP}	Positive high output voltage of a charge pump
V_{REF}	Reference voltage
V_S	Source voltage
V_{SS_LOCAL}	Ground voltage at a local interconnection node
V_{SW}	Switching voltage
V_T	Threshold voltage or thermal voltage kT/q
V_{tD}	Threshold voltage of a depletion NMOS transistor
V_{tE}	Threshold voltage of an enhancement NMOS transistor
V_{tI}	Threshold voltage of an intrinsic NMOS transistor
V_{tP}	Threshold voltage of a PMOS transistor
WL	Word-line
α	Parameter representing a body effect of a MOS transistor
α_B	Ratio of C_B to C
α_T	Ratio of C_T to C
β	Multiplication factor of the collector current to the base current of a bipolar junction transistor
η	Power efficiency
γ	Conduction angle
Φ_i	i-th clock phase

Chapter 1
System Overview and Key Design Considerations

Abstract This chapter describes which categories of voltage converters are covered in this book. Various applications of on-chip high-voltage generators such as memory applications for MNOS, DRAM, NAND Flash, NOR Flash, and phase-change memory, and other electronic devices for motor drivers, white LED drivers, LCD drivers, and energy harvesters are overviewed. System configuration of the on-chip high-voltage generator and key design consideration for the building circuit blocks such as charge pumps, pump regulators, oscillators, level shifters, and voltage references are surveyed.

1.1 Applications of On-Chip High-Voltage Generator

Section 1.1 starts with describing which categories of voltage converters are covered in this book. It also overviews various applications of on-chip high-voltage generators such as memory applications for MNOS, DRAM, NAND Flash, NOR Flash, and phase-change memory, and other electronic devices for motor drivers, white LED drivers, LCD drivers, and energy harvesters.

Voltage converters are categorized into two: switching converter (Erickson and Maksimovic 2001) and switched capacitor (Cockcroft and Walton 1932) converter as classified in Table 1.1. Switching converter is composed of one or a few inductors, one or a few capacitors, and one or a few switching devices. Switched capacitor convertor is composed of one-to-many capacitors and one-to-many switching devices. The differences are with or without inductor and single or many stages. From the viewpoint of amount of power, the switching convertor can be used for applications to generate high power typically larger than 100 mW. On the other hand, switched capacitor convertor is used for applications to generate lower power than 100 mW. Presently, degree of integration is all, except for inductors, for switching converter whereas all components for switched capacitor. This is mainly because inductance that integrated inductor can have is much smaller than the value required as well as the input current noise could be much more in switching converter with a single stage. From the viewpoint of voltage gain, that is, the ratio

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Table 1.1 Classification of voltage convertors

	Switching converter	Switched capacitor
Components	Inductor	Capacitor
	Capacitor	Switching device
	Switching device	
Feature	High power and low loss	High voltage and low current or low voltage and high current
Integration	Except for inductor	Fully integrated
$G_v \equiv V_{out}/V_{in} > 1$	Boost	Charge pump/voltage multiplier
$1 > G_v > 0$	Buck	Switched capacitor voltage down convertor
$G_v < 0$	Buck–boost	Charge pump/voltage multiplier

of the output voltage to the input voltage, there are three categories: greater than one, smaller than one and greater than zero, and smaller than zero. For the switching converter, these are, respectively, called boost converter, buck converter, and buck–boost converter. For the switched capacitor, the first and third are similarly called charge pump or voltage multiplier, and the second is called switched capacitor regulator or voltage down converter. Thus, this book covers these two categories with a voltage gain greater than one or lower than zero for fully integrated high-voltage generation among entire voltage converter system.

Following some figures show applications where on-chip voltage multipliers are used in ICs. A nonvolatile metal–nitride–oxide–semiconductor (MNOS) memory has a nitride film between the control gate and substrate where electrons or holes can trap as shown in Fig. 1.1a. Depending on the charges stored in the film, V_{GS}–I_{DS} characteristics are varied as described in Fig. 1.1b. The data in memory cells are read with V_{READ} biased to the control gate. The data is identified as "0" when the memory cell does not flow a sufficient current or as "1" when one flows. To alternate the memory data, the memory needed high voltages of 30–40 V for programming and erasing the data. To significantly reduce the system cost and complexity, an on-chip voltage multiplier was strongly desired. In 1976, Dickson theoretically and experimentally for the first time studied an on-chip high-voltage generator including a charge pump, oscillator, clock drivers, and a limiter, as shown in Fig. 1.1c. The diode is made of a MOSFET whose gate and drain terminals are connected. Dickson used two-phase clock which allowed the clock frequency as fast as possible. Using a seven-stage pump, he successfully generated 40 V from the power supply voltage of 15 V. The capacitors were also implemented using the nitride dielectric available in the MNOS process. Thus, switches and capacitors were integrated in ICs. Design parameters of 2 pF per stage, 7 stages, and 1 MHz realized an output impedance of 3.2 MΩ and a current supply of an order of 1 μA.

Figure 1.1d, e illustrates the image of how the charge pump works. For simplicity, a two-stage pump is shown. As the saying goes, a bucket, water, and the height of the surface of the water are, respectively, used as a capacitor, charge, and the capacitor voltage. V_{DD} is 2 V and V_{OUT} is 4 V. In the first half period (Fig. 1.1d), the current to the first capacitor stops when the voltage of the first capacitor reaches 2 V. The current stops flowing from the second capacitor to the output terminal

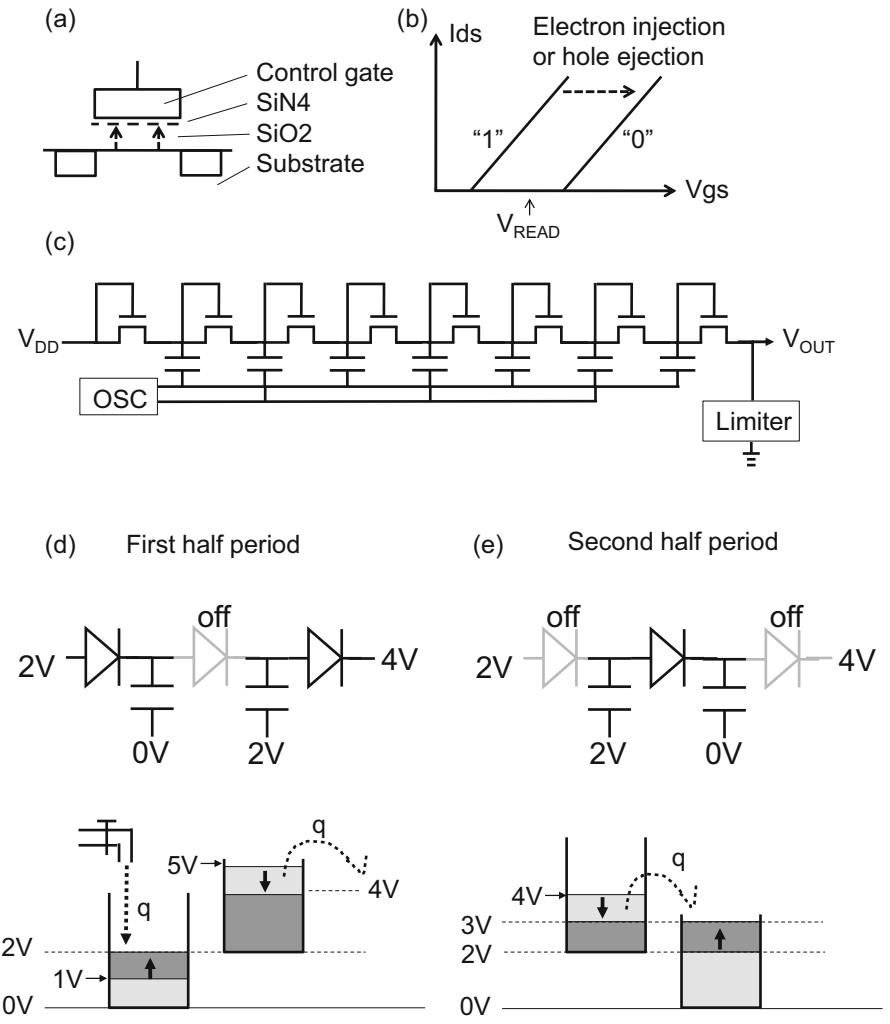


Fig. 1.1 MNOS cell structure (**a**), *I–V* curve of memory cells with data 1 and 0 (**b**), first Si verified on-chip Dickson pump (**c**), the states of the first (**d**) and second (**e**) half periods (Dickson 1976)

when the capacitor voltage reaches 4 V. At the beginning of the second half of the period (Fig. 1.1e), the capacitor voltage of the first capacitor increases to 4 V, whereas that of the second capacitor decreases to 2 V. This voltage difference between the two capacitors forces to flow the current through the second diode. When the threshold voltage of the diode is ignored, the charge transfer stops when the capacitor voltages are equalized. When the two capacitors are same size, an equilibrium state occurs when the capacitor voltages become 3 V. At the end of the second half of period, the capacitor voltages between the two terminals of the first and second capacitors are, respectively, 1 V and 3 V. At the beginning of the first half of period again, the surface potential at the top terminal becomes 1 V and 5 V,

respectively. The water tap again flows until the surface potential increases to 2 V. Charge transfer from the second capacitor to the output terminal stops when the potential of the second capacitor reaches 4 V. Thus, alternate operations back and forth between the first and second half of periods result in charge transfer from the water tap to the output terminal with the same amount of charge q.

A dynamic random access memory (DRAM) cell is composed of one transistor and one capacitor as shown at the right-hand side of Fig. 1.2. The data "0" or "1" is stored as amount of charges in the cell capacitor. To read the data, a word-line (WL) is forced high. The amount of charges stored in the cell capacitor modulates the bit-line (BL) voltage, which is sensed and amplified by a sensing circuit. Thus, voltages at WLs and BLs were toggled between 0 V and 5 V during operations when the supply voltage was 5 V. Such a huge voltage swing could make PN junctions of NMOS transistors into forward bias regime locally due to capacitive coupling where it is far from body contacts if the p-type substrate is grounded. If this happens, stored charges could be flown into the substrate, resulting in degradation in data reliability. To avoid it, another negative voltage of −5 V was needed in addition to the power supply voltage of +5 V. The negative voltage was supplied to the substrate to have sufficient operation margin with such a potential localized forward biasing of junctions eliminated.

The −5 V power supply was eliminated by implementing a back bias generator allowing to reduce the system cost and complexity having the negative voltage supply, as shown at the left-hand side of Fig. 1.2. Lee and Breivogel et al. designed the generator to output −4.2 V back bias at zero substrate current and −3.5 V bias at 5 μA substrate current. The output current was needed to be higher than the impact ionization current due to the memory operation. The power dissipation was 1.5 mW. The power efficiency is estimated to be an order of 1 %. Additional advantages are known to be improving the power and speed with smaller junction capacitance at a back bias and steeping the subthreshold slope of transistors. The back bias generator has one stage. The input terminal is connected with the substrate. During T_1 where the clock is high, the capacitor node is made at about V_T of the switching transistor with the current I_1. During T_2 where the clock is low, the capacitor node is initially pulled down to about $V_T - V_{DD}$. The current I_2 or I_3 flows until the junction or the transistor turns off. Under zero substrate current, the potential of the substrate is made at the lower one of $2V_T - V_{DD}$ and $V_T + V_{BE} - V_{DD}$.

Another application of a charge pump is a motor driver IC, as shown in Fig. 1.3. Because it needs to switch a supply voltage up to 30 V with a peak current of 30 A, a power MOSFET is used. To sufficiently reduce the power dissipation, a channel resistance as low as 40 mΩ is required. A charge pump of the power IC generates an overdrive voltage for the power MOSFET. The supply voltage for the power IC is ranged in 6–30 V, whereas overdrive voltage is targeted at a voltage higher than 10 V, i.e., $V_{PP} > V_{DD} + 10$ V. The clock amplitude is regulated using a Zener diode. The switching diodes are realized by parasitic devices of isolated P-well and N-diffusion, as shown in Fig. 1.3b. The breakdown voltage of the diode is as high as 17 V. The worst-case reverse bias is considered as $2V_{CLK}$ at the beginning of the

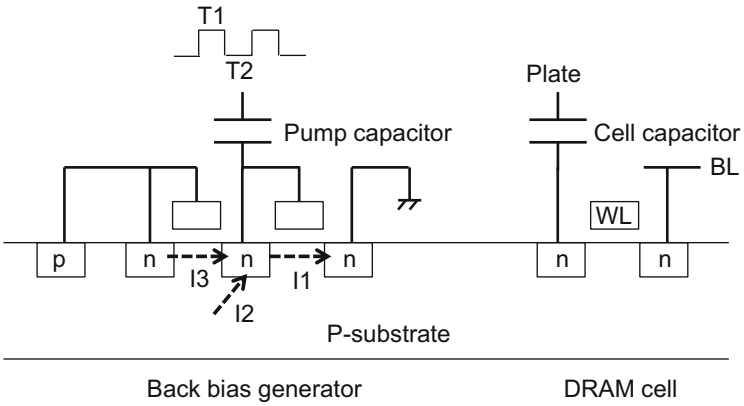
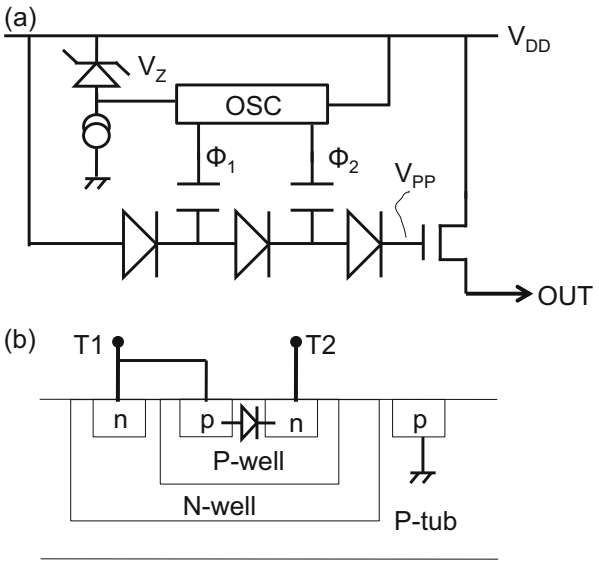


Fig. 1.2 Back bias generator for DRAM (Lee et al. 1979)

pump operation, where V_{CLK} is the voltage amplitude of the driving clocks. Thus, the Zener diode with a breakdown voltage of 8 V is used to meet the requirement for $2V_{CLK} < 17$ V. Considering a sufficient operation margin under an extreme operation temperature range of −40 to 125 °C, three-stage structure is used.

Figure 1.4a, b shows two typical configurations of drivers for white light-emitting devices (LEDs). Figure 1.4c describes *I*–*V* characteristics of the structures in Fig. 1.4b, which have similar *I*–*V* curves as forward *I*–*V* curves of diodes. The current increases exponentially as the voltage across the LED increases. Thus, the operating point in the *I*–*V* plane could vary largely if the LED is controlled based on the voltage applied. To make the illumination or the power more stable against variations in the *I*–*V* characteristics per LED, the LED is controlled on a current basis. Simple addition of a resistor to an LED aims at stabilizing the operating point. Red, yellow, or green LED needs about 20 mA at 2 V, whereas white LED does at 3.2–4 V. When DC/DC converter generates 12 V, 5 red or 3 white LEDs can be connected in series in a path as shown in Fig. 1.4a. If 5 paths are needed to have 15 white LEDs in total, the converter with capability to output a current of 100 mA has to be used. For a miniature single white LED, a charge pump IC with a single Li-ion battery with an output voltage of 2.7–3.6 V can be a solution. Whether external capacitors are added or not depends on the total driver size and cost. When adding one discrete capacitor to reduce the cost of the IC with no large pump capacitor is acceptable in terms of its form factor, one could put more numbers of white LED connected in parallel in the system, as shown in Fig. 1.4b. The LED driver IC only includes components of switches and oscillator except for the capacitor. The number of white LED connected in parallel is up to the output current of the charge pump IC. In case that the driver IC outputs 100 mA, for example, one can connect 5 LEDs in parallel. If the system requires only one or a few white LEDs, all the components including the pump capacitor can be integrated.



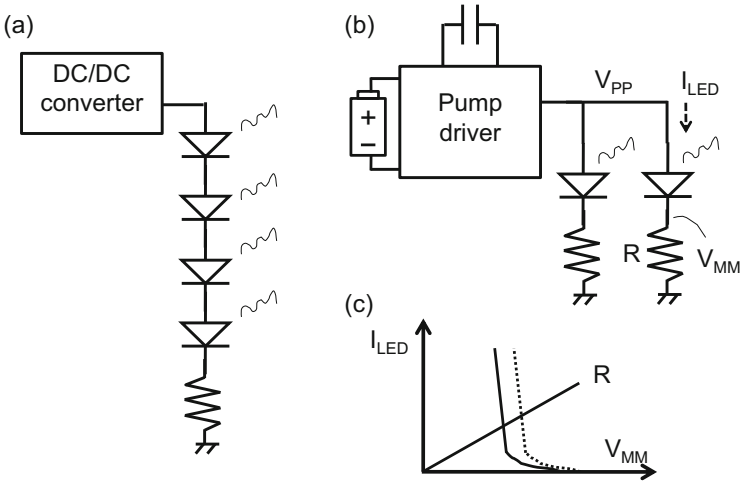


Fig. 1.3 Pump and load MOS (**a**) and diode structure (**b**) of a motor driver IC (Storti et al. 1988)

Fig. 1.4 White LED driver with (**a**) DC/DC converter (Chiu and Cheng 2007) and with (**b**) a charge pump (Wu and Chen 2009), and the operation condition of an LED (**c**)

A liquid crystal device requires two polarities of two positive voltages and two negative voltages to apply sufficiently high positive and negative voltages to each liquid crystal element aiming at improving the lifetime as shown in Fig. 1.5. Requirement for gate oxide of the transistors is sustaining a voltage of 18 V to fully turn on the pass transistors, which is half in case without generating voltages with two polarities. Otherwise, it would need a high voltage such as 36 V. A single-

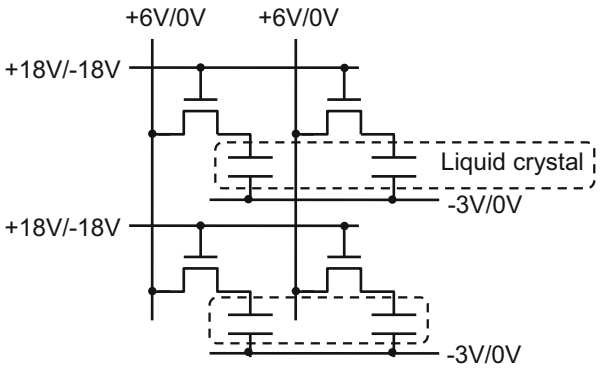


Fig. 1.5 Block diagram of a liquid crystal device (Wu and Chen 2008)

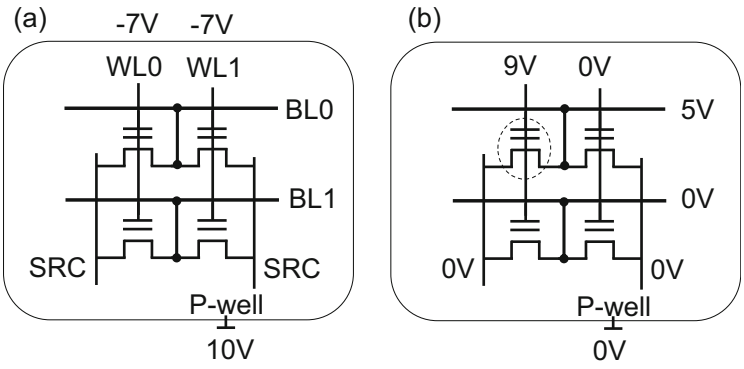


Fig. 1.6 Channel erase NOR flash memory under an erase bias condition (**a**) and under a program bias condition (**b**) (Atsumi et al. 2000)

driver IC generates these four different voltages with a supply current of an order of 10–100 μA because of no direct current to ground.

Another application using dual polarity is a NOR flash memory for erasing the data in a block, as illustrated in Fig. 1.6a. Flash cells are arranged horizontally and vertically, each of which is connected with a common source line (SRC), a bit-line (BL), and a word-line (WL). All cells in a block are placed in a common P-well. A bulk to gate voltage of 17 V needs to generate Fowler–Nordheim tunneling current flowing from the floating gate to the P-well. To allow the switching transistors for SRC and WLs to be scaled for reducing the transistor size, a high erase voltage of 17 V is divided to about half for a positive voltage of 10 V and a negative voltage of −7 V.

Figure 1.6b shows a program bias condition for the NOR flash memory. The cell enclosed by a broken line is under programming with WL and BL supplied by 9 V and 5 V, respectively. Because the scaled flash cell has a relatively low snapback voltage, the bit-line voltage (V_{BL}) has to be well controlled. The lower limit is

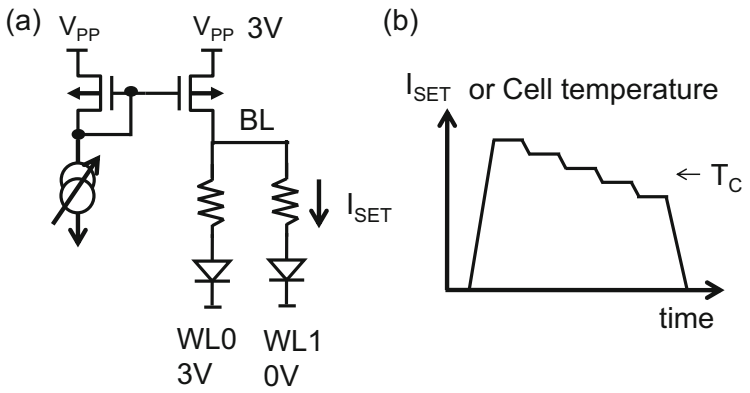


Fig. 1.7 Set voltage and current generator for phase-change memory (Lee et al. 2008)

determined by the programming speed with hot carrier injection. With too low V_{BL}, the flash cell could not have sufficient hot electrons to inject to the floating gate. The upper limit is determined by the snapback voltage. When V_{BL} is directly generated by a pump, a voltage ripple may be so large that the Flash cell can enter the snapback regime. The clamping NMOSFET can control V_{BL} with much smaller ripple voltage because the load current is determined mainly by the gate voltage as far as the load FET operates in saturation region, resulting in much better stability in programming characteristics.

Figure 1.7a shows phase-change memory elements described as the symbols of resistor, switching diodes, and a set current control circuit. To change into phase crystalline, the memory material needs to be heated up to a critical temperature (T_C) and to spend a required time interval at T_C. Because the memory array has quite large parasitic resistance in bit-lines (BLs) and word-lines (WLs), the input power required to individual memory element should have address dependencies. To program multiple memory cells with a few pulses for fast program operation, the set current as shown in Fig. 1.7b is supplied using a current control circuit with a variable current source. Thus, the boosted voltage V_{PP} is supplied to the memory elements with various current levels in a single set pulse.

Figure 1.8a illustrates a memory cell structure of NAND Flash memory. Because the floating gate is surrounded by insulator films, charges in the floating gate stay when the voltage difference between the control gate and silicon substrate is low enough. When there are many electrons in the floating gate of a cell, it has the data "0." When there are few electrons, it has the data "1." To program the data "0," the control gate is biased at a high voltage of 20 V while the substrate is grounded. Tunnel phenomenon under a high electric field is known as Fowler–Nordheim tunneling. When the control gate voltage (V_g) as shown in Fig. 1.8c is applied, the threshold voltage of the memory cell transistor is shifted as shown in Fig. 1.8b. The incremental step program pulse can reduce entire program time with well-controlled V_T of programmed cells using the general relation of $\Delta V_T = \Delta V_{PP}$. Due to the variation in program characteristics, cell A is programmed with two pulses,