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This book is dedicated to Yasmin, Zeina, Aly, Omar and Mohammed Ismail's family

Preface

Substrate noise coupling in integrated circuits (ICs) is the process by which interference signals in the form of voltage and current glitches cause parasitic currents to flow in the silicon substrate to various parts of the IC. The source of such glitches and parasitic currents could be from the switching noise of high speed digital clocks on the same chip. In RF and mixed signal ICs the switching noise is coupled to sensitive analog and RF nodes in the IC causing degradation in performance that could severely impact the yield. Thus, overcoming substrate coupling is a key issue in successful "system on chip" first-pass integration where RF and mixed signal blocks, high speed digital I/O interface are integrated with digital signal processing algorithms on the same chip. This is particularly true as we move to sub-90 nanometer system on chip integration.

In this book a substrate aware design flow is built, calibrated to silicon and used as part of the design and validation flows to uncover and fix substrate coupling problems in RF ICs. The flow is used to develop a comprehensive RF substrate noise isolation design guide to be used by RF designers during the floor planning, circuit design and validation phases. This will allow designers to optimize the design, maximize noise isolation and protect sensitive analog/RF blocks from being degraded by substrate noise coupling.

Several effects of substrate coupling on circuit performance will be identified and remedies will be given based on the proposed design guide. Three case studies are designed to analyze the substrate coupling problem in RFICs. The case studies are designed to gradually attack the problem at the device (Case 1), circuit (Case 2) and system levels (Case 3). At the device level a special emphasis is given to the design of on chip inductors as an important device in today's SOC systems and the impact of substrate noise coupling on the inductor performance is characterized. An accurate model is developed for a broadband fit of the inductor scattering parameters to a lumped macro model that is used in the system analysis of case study 3. This model is shown to be scalable and is proven to be accurate when applied to various frequency bands and inductor geometries. A special emphasis is put on the DFM effects that affect the design robustness. A circuit level case study is developed and results are compared to simulations and silicon measurements to highlight the need for such a flow before silicon fabrication "taping out" to ensure a yielding part. In case study 3 a system level problem is studied on a GSM cellular receiver chain.

The results are used as a demonstration vehicle to debug and resolve a system level substrate noise coupling problem that would otherwise have caused the receiver to malfunction, with adverse implication on yield and profit margin for such a high volume product.

Chapter 1 introduces the work and highlights the motivation, objective and contribution. Chapter 2 discusses the phenomena of substrate coupling. Devices to substrate interface, noise injection, reception and propagation are explained in details. The industry standard algorithms used to model the substrate are studied and compared. The design methodology used to account for and integrate the substrate model in the design flow is highlighted. In Chapter 3 the design experiments are discussed, a test chip is described together with the de-embedding technique and measurement procedure. The design flow is then developed to model the substrate and is calibrated to the measurement data and simulations vs. measurements are reported as a foundation of a design flow that is used in the next chapters. In Chapter 4 a substrate isolation guide is developed based on two main methodologies. First, circuit and layout considerations are presented to maximize isolation, namely floor planning techniques. Supply line distribution and ground rails are also designed to maximize substrate isolation. Secondly, isolation structures are introduced and designed. Biasing and sizing of such structures are discussed; all are based on the calibrated design environment developed in Chapter 3. In Chapter 5 understanding the impact of these isolation structures and the substrate characteristics is used to develop a design flow for on chip spiral inductors. Measurements and simulations are compared to validate the flow and various flavors of on chip inductors are designed to fit the needs of several RF applications. A scalable inductor macro model is developed that is shown to be usable to a very good accuracy across a wide variety of inductor geometries and frequency bands. DFM effects are studied and their impacts are highlighted on the inductor performance. Chapter 6 presents three industrial case studies. The case studies are designed to gradually show the impact of substrate coupling at a device, a circuit and then at a system level. Simulation and measurement results are shown with and without applying the isolation techniques and results are compared. Chapter 7 concludes the work and proposes future work.

This book is intended for RF and mixed signal design engineers, system-on-chip designers and process engineers as well as graduate students and researchers in the fields of integrated circuits and systems on chip design and optimization.

The work has its roots in the Ph.D. dissertation of the first author, completed at the Analog VLSI Lab, the Department of Electrical and Computer Engineering, The Ohio State University. We would like to thank all those who assisted us during different phases of this work including our colleagues at the Analog VLSI Lab and at Intel Corporation. We also like to thank the Semiconductor Research Corporation for partially funding this work. Finally, we would like to thank our families for their help and support.

Columbus, Ohio

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