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Preface

Circuit and interconnect design techniques that tackle many of the greatest difficulties and uncertainties in the development of ICs for RF and high bit-rate applications are the subject of this book. At bit-rates above 10 Gb/s, the impact of on-chip interconnect on circuit performance can be detrimental to the performance of the IC. The bottlenecks in interconnect design, circuit design and on-chip signal distribution for high bit-rate applications are analysed, and solutions for circumventing them presented. These methodologies can be applied to analyse whether target bit-rates and frequencies can be reached in a given IC technology, or to provide guidelines for further IC process optimisation in support of today's and tomorrow's high bit-rate circuit design. It should be noted that specific amplifier requirements such as low noise and intermodulation distortion are not discussed in this book.

The main topics addressed in this book and how they relate to each another are illustrated in Fig. 1. High bit-rate circuit design using advanced SiGe and InP HBT IC technologies is the core subject of this monograph.

The bottlenecks in IC design for high bit-rate applications tackled in this book are:

1. Interconnect design and modelling
2. IC process technology: transistor performance and optimisation; relevant metrics
3. On-chip signal distribution; joint optimisation of circuit and interconnect
4. Reduced breakdown voltage of transistors in next-generation IC processes
5. LC-VCO design at microwave frequencies
6. IC design flow

Several key innovations are presented in this book. For on-chip transmission lines, configurations are proposed that are minimally sensitive to their surroundings (see Fig. 2.20). These configurations enable low loss, low crosstalk and well-controlled line characteristics (e.g., characteristic impedance and delay). Improved performance margins provide flexibility in the layout floorplan of an IC. The floorplan is usually ill defined in the initial phase of an IC design. However, a design library of interconnects that are desensitized to their surroundings enables accurate predictions of the impact of interconnects on circuit performance, simplifying the floorplanning

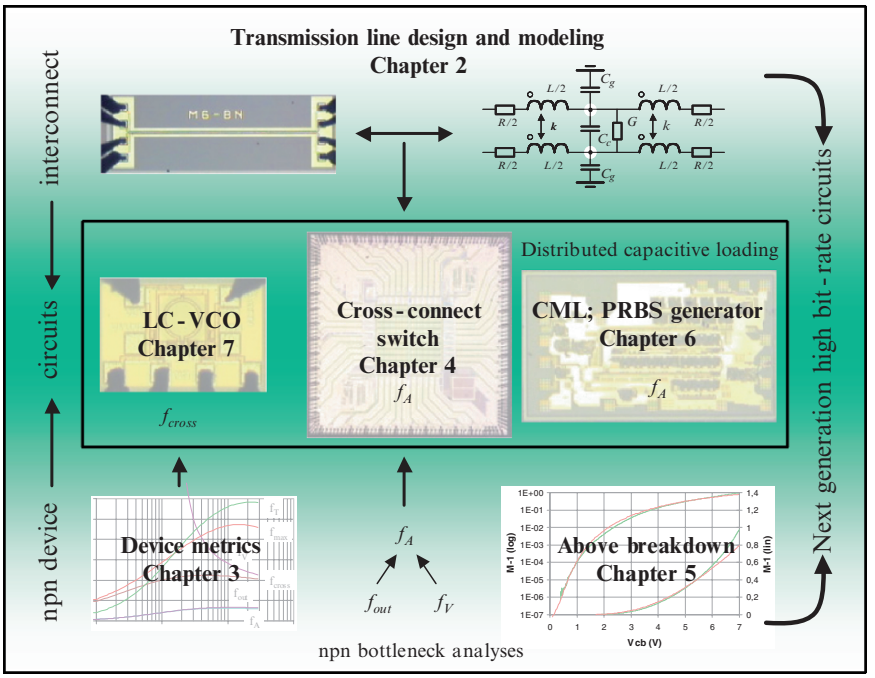

Fig. 1 Structure of the book, showing how the various topics relate to each other

phase. The proposed configurations for single-ended and differential applications can be applied in any IC technology, provided that at least two metal layers are available for interconnections.

Lumped-element transmission line models that capture the characteristic impedance, delay and loss of the lines, and the relationships between element values and the characteristic impedance and time delay are presented. The equivalent circuit model for a differential transmission line (see Fig. 2.6) provides an accurate representation of the differential and common-mode characteristics of the line. As a result, these models can be used during the initial design stages, *before* the physical layout of the transmission lines.

IC technology requirements for various RF and high bit-rate functions are similar. The figure of merit f_A, introduced in Chapter 3, is a valuable parameter when analysing the capabilities of the npn transistor in an IC process for broadband applications. Circuit design supporting bit-rates up to f_A (for highly complex circuits such as a cross-connect switch), and up to $2 \cdot f_A$ (for CML circuits of average complexity such as a PRBS generator) is feasible. Available bandwidth f_A can be further sub-divided in two parameters: the input bandwidth f_V and output bandwidth f_{out}. Analysis of f_V and f_{out} as a function of bias directly reveals which dominates when biasing the transistor at peak-f_T. This information is invaluable for IC process optimisation.

The design of a cross-connect switch IC for optical networking described in Chapter 4 is an excellent vehicle to highlight the topics addressed in this book, since it integrates many of the disciplines that are important to high bit-rate design. The cross-connect demonstrates the feasibility of a complex circuit operating at an aggregated bandwidth of up to 250 Gb/s in a SiGe process with a 12 GHz f_A. However, it also shows that significant improvements in circuit design and IC technology are needed in order to realise a similar function at 40 Gb/s per input.

When higher supply voltages are used, circuit topologies that may enable improved circuit bandwidths become feasible. Moreover, the trend towards lower breakdown voltages in modern IC processes is driven by the fact that a lower breakdown voltage BV_{CEO} usually allows a higher unity-gain frequency, f_T. Chapter 5 deals with the consequences of circuit design at supply voltages above the breakdown voltage of the transistor. When a transistor is operated at a collector-emitter voltage above its breakdown voltage BV_{CEO}, current flows out of the base terminal due to avalanche multiplication from the collector-base junction. The impact of avalanche current on bias circuits is analyzed, and avalanche current compensation techniques are introduced to improve the accuracy of current mirrors when operated above breakdown.

Chapter 6 discusses the design of high bit-rate current-mode logic circuits (e.g., 40 Gb/s and higher). A PRBS generator designed in an InP HBT technology which achieves record performance in terms of output bit-rate is used as a test and demonstration vehicle.

Many high-frequency oscillators use a cross-coupled differential pair to synthesise a negative resistance. The maximum attainable oscillation frequency for such a topology is given by metric f_{cross}, as shown in Chapter 7. Thus, f_{cross} can be used for IC process optimization, in a similar way to the unity-power-gain frequency, f_{max}.

A capacitively loaded emitter follower provides a negative shunt input resistance up to f_{LIMIT}. For practical values of the load capacitance, f_{LIMIT} is considerably higher than f_{cross}, thus enabling oscillator design at frequencies that cannot be reached with topologies based on the cross-coupled differential pair. Moreover, a capacitively loaded emitter follower can be implemented as a double emitter follower with a resistive load. The negative resistance and output buffer functions of an LC-VCO can be combined in this way, as described in Chapter 7.

The work presented in this book has been carried out at the Philips Research Laboratories, Eindhoven, the Netherlands, as part of the Philips Research program. The authors would like to thank the Philips Research management for their support and encouragement. Many colleagues and students contributed to the results presented. We wish to thank all of them, especially the valuable contributions from Fred Hurkx, Edwin van der Heijden, Hans Brekelmans, Dave van Goor, Wei Liat Chan, Jeroen Paasschens, Peter Deixler, Dennis Jeurissen, Johan Klootwijk, Jos Bergervoet, Cicero Vaucher and the Optical Networking team of Philips Semiconductors in Caen, France. We wish to acknowledge Domine Leenaerts for his constructive feedback and proofreading. This work has also been reviewed by Prof. Dr. ir. J.W. Slotboom, Prof. Dr. ir. B. Nauta, Prof. Dr. ir. A.H.M. van Roermund,

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Chapter 1
The Challenge

The advance of modern IC processes has supported increasing bit-rates in many consumer and professional applications, such as hard disk drives and optical networking. Achieving a higher bit-rate by applying a new generation of an IC process for analog circuits and systems is not a simple matter of scaling existing solutions. The reduced feature size of new generations of IC technology drives the improvement of high-frequency performance of transistors and passive elements, but at the same time requires a reduction of supply voltages. This poses significant challenges to the design of high-frequency building blocks. Example applications that highlight these challenges are transceivers and cross-connect switch ICs for optical networking.

In optical networks, bit-rates in the physical layer have increased over the past two decades from 155 Mb/s to approximately 40 Gb/s (see Fig. 1.1).

Network capacity is being increased by two technologies simultaneously. One is higher data processing speeds and electronic time division multiplexing (ETDM), which drives the increase of bit-rates. The second is wavelength division multiplexing (WDM), which allows the use of multiple independent data streams per fibre, each assigned a different colour and thereby multiplying the data transmission capacity per fibre by the number of colours used. The WDM technique will not be further discussed.

Due to its high bit-rate, optical networking has been the driving force behind several generations of bipolar IC technologies. For example, IBM targets $>100\,\mathrm{Gb/s}$ communication systems for their $0.12\,\mu\mathrm{m}$ silicon-germanium:carbon (SiGe:C), $f_T = 207\,\mathrm{GHz}$, $f_{max} = 285\,\mathrm{GHz}$ technology [4].

A block diagram of the physical layer of a typical optical networking system is shown in Fig. 1.2. The operation of this example implementation can be briefly explained as follows.

The transmit path of the physical layer includes a clock multiplier unit (CMU) and a multiplex (MUX) function, usually combined in a single IC. The incoming N parallel data bits are multiplexed into a high bit-rate serial stream. Usually, N equals 4 or 16, due to the hierarchical nature of the format with binary data. The voltage controlled oscillator (VCO), with oscillation frequency f_0 in this example equal to the bit frequency f_{bit}, is locked to the incoming f_{bit}/N-clock using a phase-locked

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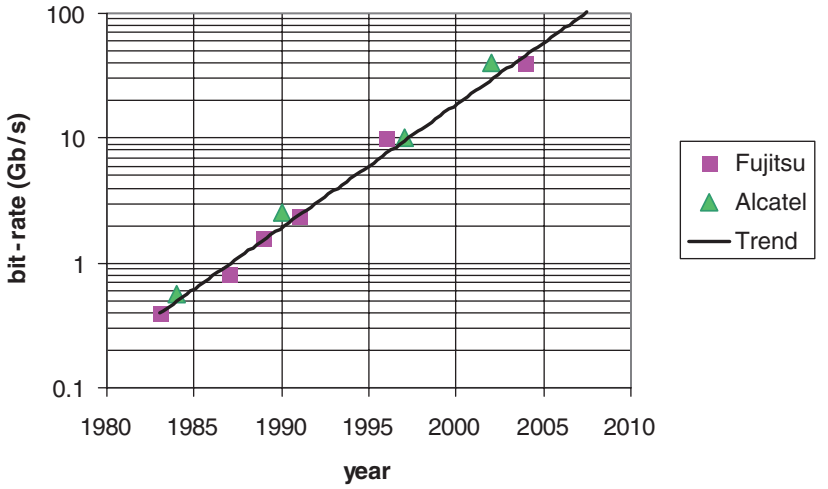


Fig. 1.1 Evolution and extrapolation of the bit-rate in optical networks [1–3]

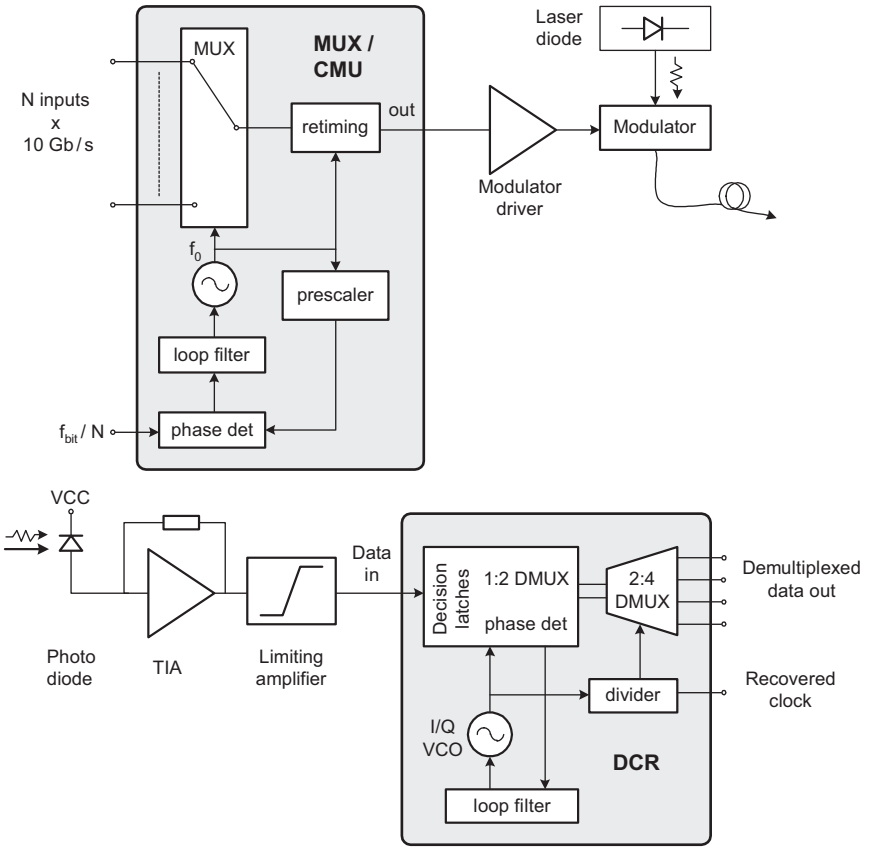


Fig. 1.2 Typical block diagram of the physical layer of an optical networking system. This example shows a full-rate MUX/CMU and half-rate DCR implementation

loop (PLL). The serialised data at the output of the multiplexer is retimed, typically using a data flip-flop (DFF) clocked at f_{bit}. This retiming, important for low jitter in the serial data, requires a full-rate transmit architecture: $f_0 = f_{bit}$. The serial data output stream is amplified by the modulator driver, driving an external modulator of the laser diode light output. This modulates the light coupled to the fibre, thereby performing electrical to optical conversion of the transmit data.

In the receive path, a photodiode converts the incoming light from the fibre into an electrical current. This current is amplified by the transimpedance amplifier (TIA). Usually, the output amplitude of the TIA is further amplified to a fixed amplitude by a limiting amplifier, driving the data and clock recovery (DCR) function. Inside the DCR, the data and the clock are recovered, and the demultiplexing function (DMUX) is usually implemented, too. The VCO inside the DCR unit needs to lock to the incoming bit-rate. Usually, a PLL performs this function.

In some high bit-rate receivers, a high-Q bandpass filter such as a dielectric resonator is used to recover the clock. This avoids the need for a VCO, but results in a receiver that operates at only a fixed bit-rate. The use of high-Q filtering is typically seen only in very high bit-rate circuits [5]. Using a PLL has the advantage of achieving a higher degree of monolithic integration, and enables operation over a wider range of input bit-rates.

The multiplexer of the transmit path is often implemented using cascaded 2-to-1 multiplexer building blocks, clocked at binary scaled frequencies ranging from f_{bit}/N for the input multiplexers to $f_{bit}/2$ for the final multiplexer. A cascade of frequency divide-by-2 circuits generates the required clock frequencies from the VCO frequency. The design of the on-chip clock distribution network is critical to the performance of the IC. The timing alignment between the multiplexers in relation to the data needs to be carefully analysed and optimised. Each of the multiplexers is usually built from current-mode logic (CML), using latches and selectors. The DCR function also uses latches for data recovery, demultiplexing and a (bang-bang) phase detector, as in for example [6, 7]. This makes the design of high-speed CML circuits an important element of high bit-rate circuit design.

For MUX/CMU output bit-rates of 10 Gb/s and beyond, the design of the fully integrated oscillator is a challenging task. The VCO needs to achieve a low phase noise, since phase noise translates into jitter at the data output. Typically, LC-type VCOs are used to meet the phase noise specification.

A half-rate CMU relaxes the required oscillator frequency by a factor of two. In return, however, the duty cycle of the VCO output signal becomes important. In a half-rate DCR system with quadrature VCO, the phase accuracy between in-phase (I) and quadrature (Q) outputs is also an important specification. Also, a large tuning range may be required for DCRs that need to support several transmission standards, operating at different bit-rates.

The DCR is sometimes implemented as full-rate, but often as half-rate, with both the I- and the Q-signals driving a DCR function operating at half the incoming bit-rate. For 40 Gb/s, systems have been published in various IC technologies such as indium-phosphide (InP), silicon-germanium (SiGe) and recently the first CMOS implementation at quarter-rate [8]. Implementing the DCR at half-rate

halves the required oscillation frequency f_0, but requires the availability of in-phase and quadrature oscillator output signals for phase detection. Similarly, the quarter-rate implementation of [8] needs a 10 GHz four-phase VCO output.

The design of the on-chip clock distribution network is critical to the performance of the IC. Distribution is needed to a multitude of latches, implementing the phase detector.

To conclude, there are several critical elements for DCR and MUX/CMU performance including the VCO, CML latch and gates, clock distribution, and input/output signal amplifiers (to operate always at full-rate). The latch performance plays a highly critical role in the DCR decision function and the MUX/CMU output retiming function. In addition, the clock distribution in the transmit and receive functions is critical to the performance of the ICs.

The problems encountered in the design of DCR and MUX/CMU ICs are also involved in the design of many other ICs for high bit-rate applications. High-speed digital functions and GHz VCO circuits are for example part of ICs for high bit-rate optical networking functions with a built-in self-test feature. This book discusses the design of circuits that can be used for high bit-rate applications, for example in a cross-connect switch. In Chapter 4, the design of a cross-connect switch IC with built-in self-test will be described. This cross-connect function will be introduced below.

Optical cross-connect switches (OXCs) are widely used for routing data in optical networks. The basic topology for optical backbone networks is a ring structure with optical add drop multiplexers (OADM) and optical cross-connect switches, as in Fig. 1.3 [3].

Each ring uses multiple fibres to provide protection in the case of cable cuts. Different categories of switches exist [1]. Three example implementations of OXCs are shown in Fig. 1.4. These optical switching solutions are referred to as: electrically

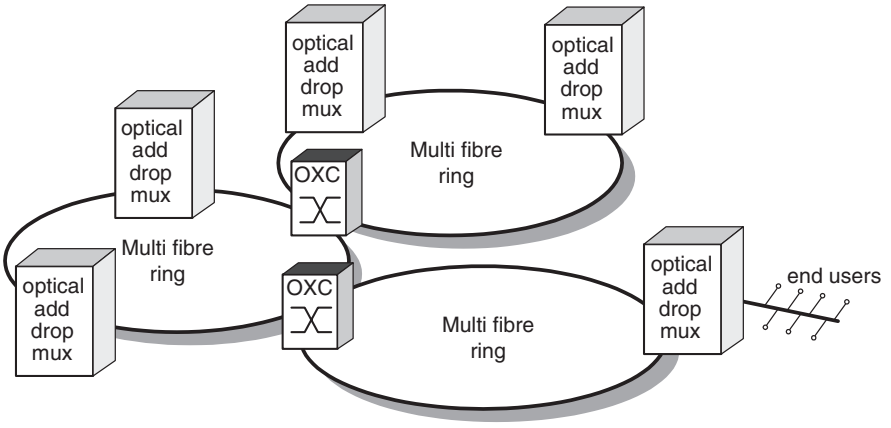


Fig. 1.3 Basic structure of an optical backbone network

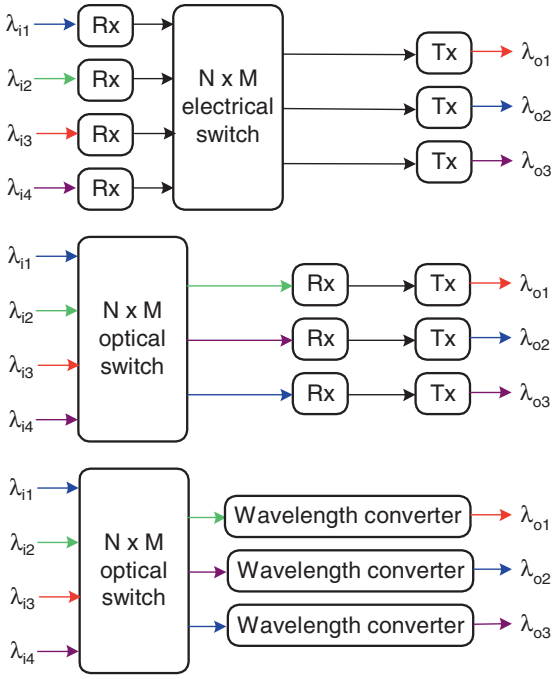


Fig. 1.4 Different solutions for OXCs

switched router/transponder (top), optically switched router/transponder (middle), and all-optical wavelength router (bottom).

Note that an *electrically* switched router/transponder is still referred to as an *optical* cross-connect switch. In all cases, wavelength routing is performed by tuning the wavelength of the output ports.

The electrically switched router/transponder is usually combined with an electrically implemented retiming function [3]. This type of switch dominates the market today. The all-optical switch solution is an interesting vehicle for research, since it allows independent bit-rate and modulation formats for the switches, but makes retiming significantly more difficult. In the following, only the electrically switched router/transponder will be considered.

The bandwidth of a switch is often expressed as aggregated bandwidth, defined as the maximum bit-rate per input multiplied by the total number of inputs. To route the data in the backbone of the network, achieving the highest possible aggregated bandwidth per switch is needed to lower cost, number of components in the switching network and thereby increase reliability. Achieving the highest aggregated bandwidth per switch IC means both achieving the largest possible number of inputs and outputs, and achieving the highest possible bit-rate per input. For many practical applications, the input bit-rate needs to support standard SDH/SONET rates such as 2.5–3.125 Gb/s or 10–12.5 Gb/s [9].

The following challenges need to be addressed for the design of high-speed switch ICs: the design of high-bandwidth input and output buffer circuits, the design of high-bandwidth matrix circuits, and distribution of all input signals through the IC with minimum jitter generation and crosstalk. This includes the design and modelling of RF interconnect.

The two high bit-rate example applications described – transceivers and cross-connect switches for optical networks – involve similar challenges for the design of the ICs, which can be summarised as:

The design of circuits and interconnect for high bit-rate and RF applications, and their combined optimisation.

This is the subject of this book. The following sections introduce the fundamental issues of this subject, relating to interconnect, IC technology, RF building blocks and design techniques.

1.1 Interconnect

In the case of nearly all high bit-rate and RF circuits, the interconnections between circuits require detailed analysis and modelling. This includes routing on printed circuit boards and assessing the effect of bondwires and on-chip interconnect. However, not all on-chip interconnect is of equal importance to the performance of the IC.

A first class of interconnect lines requiring accurate analysis and modelling are the RF signal lines. Several transmission line configurations can be used for RF interconnect. Some widely used examples are shown in Fig. 1.5.

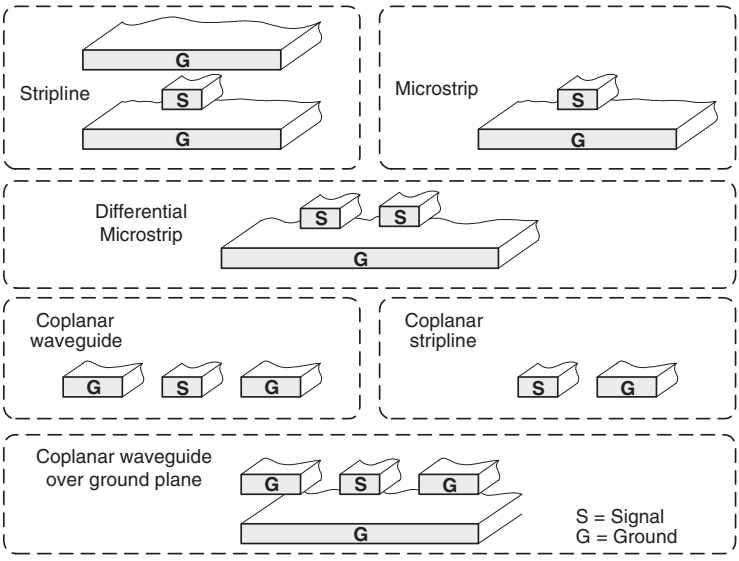


Fig. 1.5 Some widely used transmission line configurations

Transmission line models are required for computer-aided design. The term 'transmission line' in this respect means that the time delay along the line is important, meaning that the line inductance is included in the model, as for example for 10 Gb/s applications in [10] where it is recommended to use such models for all interconnects of >1.5 mm length. At 10 Gb/s, the wavelength λ of the $f = 5$ GHz fundamental of a ...0101010... pattern, assuming a relative permittivity $\varepsilon_r = 4$, equals $\lambda = c/(f \cdot \sqrt{(\varepsilon_r)}) = 3$ cm, while the on-chip physical distance between 2 bits equals 1.5 cm. Thus, the suggested 1.5 mm corresponds to 5% of the wavelength or 10% of the distance between two consecutive bits. It is common practice to use transmission line models for interconnects of length $l > 0.05 \cdot \lambda$, as suggested in [10].

In [16], a cross-connect switch implemented in gallium-arsenide (GaAs) technology is described, in which substrate losses may be ignored due to the high resistivity of the GaAs substrate. The models themselves are lumped element RLC models, describing a single-ended coplanar transmission line. The use of *differential* transmission lines is not considered, although these are widely used in differential circuit design.

In [17], the use of microstrip lines for longer RF interconnects is proposed. Lines are classified as 'critical', 'less critical' or 'non-critical', and the lengths of the 'critical' lines are minimised at the expense of increase in length of the 'non-critical' lines. This approach can also be applied to cross-connect switch ICs, but it needs to be understood which lines are critical and which lines are less critical in such an application. In cross-connect switch ICs, the chip size will readily exceed $0.05 \cdot \lambda$ in two directions and because each signal needs to travel across the complete IC, many signal lines are electrically long. The electrically long lines (including the supply lines) must be considered as transmission lines. Furthermore, other options besides microstrip interconnect are possible (see for example Fig. 1.5) that may be more attractive for cross-connect switch applications, where the transmission line density plays an important role in the chip area.

In [18], interconnect is analysed for digital (microprocessor) applications. Important parameters considered are line inductance, loss and delay. A lumped element model is presented that captures the frequency dependence of series resistance and inductance by using a parallel-network of resistors and inductors per section. Given the application, only single-ended interconnect configurations are considered.

The use of interconnect models that include both differential and common modes is mentioned in combination with RF circuit design in [20]. Here, a pseudo-random binary sequence (PRBS) generator generating a 10 Gb/s output signal is described. Post-layout simulation was done with interconnect models generated from finite element software for RF lines longer than 100 µm. Although this approach is correct, it does not provide a-priori knowledge on how to predict the influence of the RF interconnect on the signal integrity. A more structured approach for the interconnect design and modelling is needed.

Early in the design phase of high bit-rate and RF ICs, accurate (but simple) interconnect models are needed. For most applications, time domain analyses for studying (for example) jitter need to be supported. Lumped element models fulfil this requirement.

The interconnect models described in Chapter 2 will be used in combination with high bit-rate and RF circuit design in the rest of the book. Lumped element models are used for modelling selected single-ended and differential interconnect configurations. These models are only valid for interconnects shielded from the substrate. This shielding is important for minimisation of crosstalk coupled via the substrate, in order to achieve low loss and to obtain a well-controlled line impedance, independent of other interconnect and circuitry near the interconnect under study.

Another class of interconnect that deserves equal attention is the supply routing, a subject that is not very often discussed in high bit-rate and RF circuit literature. For wafer probing this is less important than for wire-bonded ICs, since the supply line inductance is typically lower. Still, supply line inductance in combination with on-chip high-Q decoupling capacitors can cause severe ringing in supply networks. Such ringing typically has a dramatic impact on all the signals in the IC. Even in differential circuits, in which signal energy at the supply line is suppressed by the common-mode rejection of the circuits, it is common practice to *evaluate* the output signals using single-ended measurements.

The decoupling strategy requires a more structured analysis for RF ICs, in order to avoid resonance while applying the best possible on-chip decoupling. The supply network needs to be analysed for potential resonance. If such resonance exists, damping may be applied to avoid ringing of the supply voltage of the circuits. For fully differential circuits, the supply decoupling strategy may differ from the strategy for single-ended circuits [17]. Several supply domains can be used on-chip; each domain requires individual supply decoupling analysis and design.

Transmission line interconnect modelling can also be applied to supply lines, in order to better understand and predict the effect of supply line impedance on circuit performance. The supply line modelling and decoupling strategy should be an integral part of the design of all microwave ICs, and will be discussed for several IC implementations described in this book.

1.2 Device Metrics

The performance constraints of transistors play an important role in fundamental circuit limitations. For example, relating circuit performance to widely accepted technology parameters allows one to predict the impact of a new technology. The most commonly used device metric is the unity current gain bandwidth, or f_T of the transistors, defined as the (extrapolated) frequency where the magnitude of the current gain, $|h_{21}|$, equals 1, as shown in Fig. 1.6.

The curve shows a typical $|h_{21}|$ as a function of frequency, together with the asymptotic response. The f_T value is derived from the asymptotic response, with the extrapolation frequency chosen in the frequency range between f_T/β_0 and f_T, at a frequency where the slope is -20 dB per decade.

Circuit performance is often benchmarked against the peak-f_T of the process. To judge whether an IC process will perform adequately in a certain application,

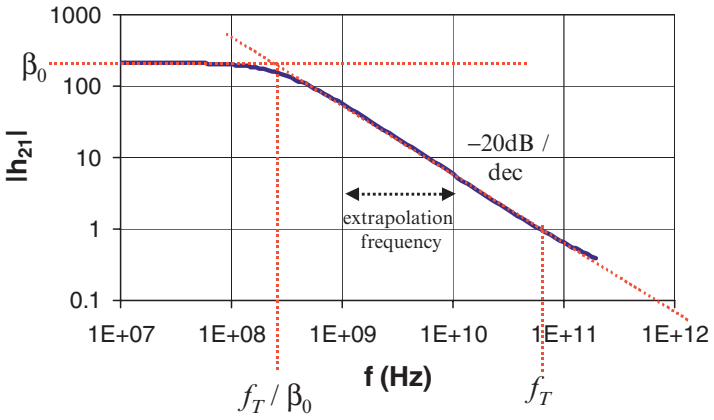


Fig. 1.6 Definition of f_T

representative building blocks such as ring oscillators and frequency dividers can be designed and characterised. CMOS or CML ring oscillators with a large number of inverters are often implemented to demonstrate the capabilities of an IC process because gate delay is derived from simple low-frequency measurements. This gate delay is an indication of the propagation delay that can be expected from more complex (digital) functions.

A more accurate performance indicator is the maximum toggle frequency of a static CML divide-by-2 circuit, because the basic cell of the static divider, the latch, also forms the basic element of many building blocks inside a high bit-rate optical networking system. The maximum toggle frequency of a bipolar CML static divide-by-2 circuit is usually related to the peak-f_T of the process. An often-used benchmark for the maximum toggle frequency of the frequency divider is $f_T/2$, although the $f_T/2$ value is an oversimplified relation [11] and therefore not simply obtained. For example, the static frequency divider described in [11] is realised in a InP bipolar technology with $f_T = 198\,\text{GHz}$ and reached a speed of 72.8 GHz. The f_T is indicative of, but not definitive for the maximum toggle rate of a frequency divider since it does not take into account all the delay contributions in circuits. To be more specific, the input bandwidth of the transistor when driving the base with a voltage source hardly affects the f_T but is important for the maximum speed of CML circuits. The f_T is hence a poor metric for CML circuits. Consequently, f_T is an important, but not the only, performance indicator for RF circuits.

The fundamental maximum frequency of oscillation that can be obtained for a single transistor is by definition equal to f_{max}, defined as the frequency at which the power gain of the transistor equals 1, assuming a conjugate match for input and output ports of the transistor. Since such a power match cannot be assumed for most oscillator circuits, the practical maximum oscillation frequency remains well below f_{max}. The maximum oscillation frequency f_{max} can be approximated by [12]

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi R_b C_{bc}}} \tag{1.1}$$

where R_b is the base series resistance and C_{bc} the base-collector capacitance. In contrast to f_T, metric f_{max} is a function of the base resistance R_b, and consequently a function of the input bandwidth of the transistor, important for the performance of many RF circuits.

In Chapter 3, the device metrics important for RF applications will be briefly reviewed. This will cover f_T and f_{max} as well as the less frequently used metrics f_A, f_V and f_{out}. In addition, a new metric f_{cross} will be introduced that relates the maximum oscillation frequency for oscillators using a cross-coupled differential pair to technology. Trends in recently published bipolar and BiCMOS IC processes targeting RF and microwave applications will be summarised. The overview of this chapter is important for high bit-rate and RF circuit design, because in this book a link is made between these device metrics and the performance of several high speed/high frequency circuits.

1.3 Cross-Connect Switches

In 1974, a monolithic 4-input, 4-output (e.g., 4×4) cross-connect switch based on CML was presented, intended for use in a space-division network for digitised video distribution [13]. Later, cross-connect switches were applied to couple high-speed processors, sharing data in a wideband communication network, as in [14].

Recent high bit-rate switches for optical networking applications are implemented in GaAs or InP technologies [15, 16, 19]. Bit-rates up to 25 Gb/s have been published in InP technology, supporting 2 inputs, achieving an aggregated bandwidth of 50 Gb/s. An aggregated bandwidth of 160 Gb/s, implemented as 16 inputs, each supporting up to 10 Gb/s, has been achieved in GaAs technology with bipolar junction transistors, the highest throughput reported up to the year 2003. These ICs do not include in situ test functionality, such as a boundary scan test or a built-in random data generator and error detector.

Some switch ICs use an architecture in which a demultiplexer is used per input, demultiplexing each input signal to M outputs. A multiplexer is used per output, selecting one out of N possible input signals. A block diagram of such an architecture is shown in Fig. 1.7 [15]. This architecture does not support multicast nor broadcast functionality, since the inputs cannot be connected to multiple outputs simultaneously. Moreover, there are a large number of wires between demultiplexer outputs and multiplexer inputs: $(N \times M)$ signal paths (of which M carry an RF signal). Multicast functionality is desired, since it allows transmission of (for example) advertisements to multiple users simultaneously.

A more favourable switch IC implementation, supporting multicast and broadcast functions, requires distribution of each input signal to the inputs of all MUX circuits, leading to the architecture of Fig. 1.8. In the literature, this switch architecture has

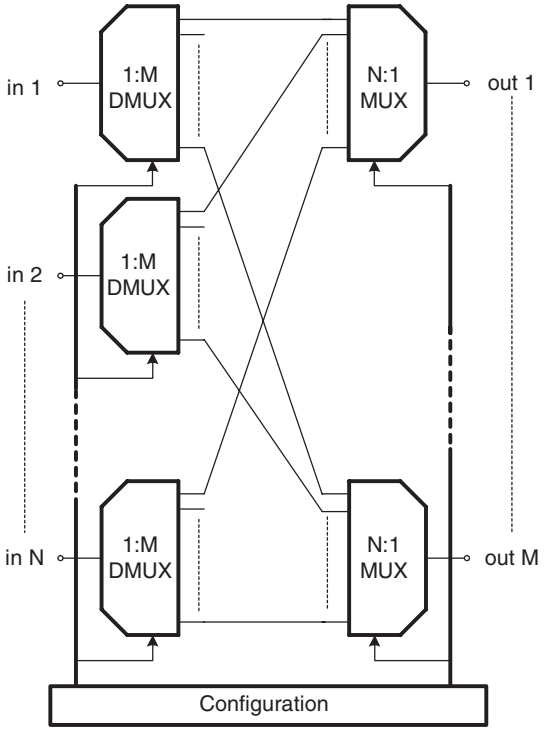


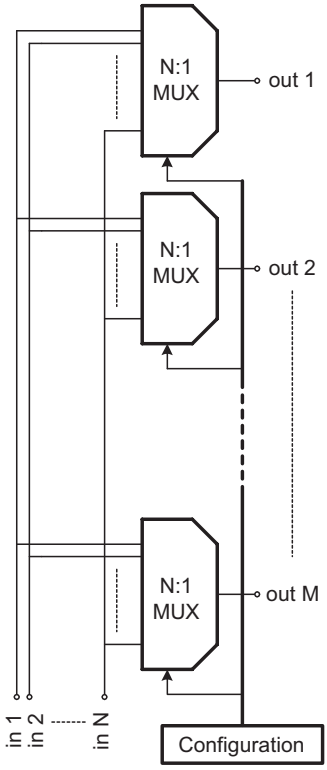
Fig. 1.7 Block diagram of an N × M cross-connect switch based on DMUX–MUX architecture [15]

been referred to as broadcast-and-select architecture [16]. Similar functionality can be achieved with a matrix architecture.

Recently, a 20-input 20-output cross-connect switch supporting up to 12.5 Gb/s per input was presented [21]. A block diagram of this IC, achieving the highest reported aggregated bandwidth to date of 250 Gb/s, is shown in Fig. 1.9. The IC is implemented in a 0.25 µm SiGe process with 70 GHz f_T [22].

The design of a cross-connect switch IC with high aggregated bandwidth poses several challenges, covering many of the subjects described in this book. The circuits of the RF path such as the input buffer, output buffer, and matrix, must be designed with sufficient bandwidth. The RF interconnect from bondpads up to input/output circuits needs to be designed and accurately modelled. The matrix circuits and RF interconnect inside the matrix need to be jointly optimised. Issues requiring attention in this context are (among others): losses in interconnect, characteristic impedance of the interconnect, interconnect configuration for low crosstalk, input/output impedance of circuits connected to the interconnect, signal transfer across loaded interconnect, power supply routing and supply decoupling. The complete RF signal path needs to be verified and optimised. For testability of the IC, a PRBS generator and error detector are included. The design of the on-chip PRBS

Fig. 1.8 Block diagram of an N × M cross-connect switch based on a distribute-MUX architecture



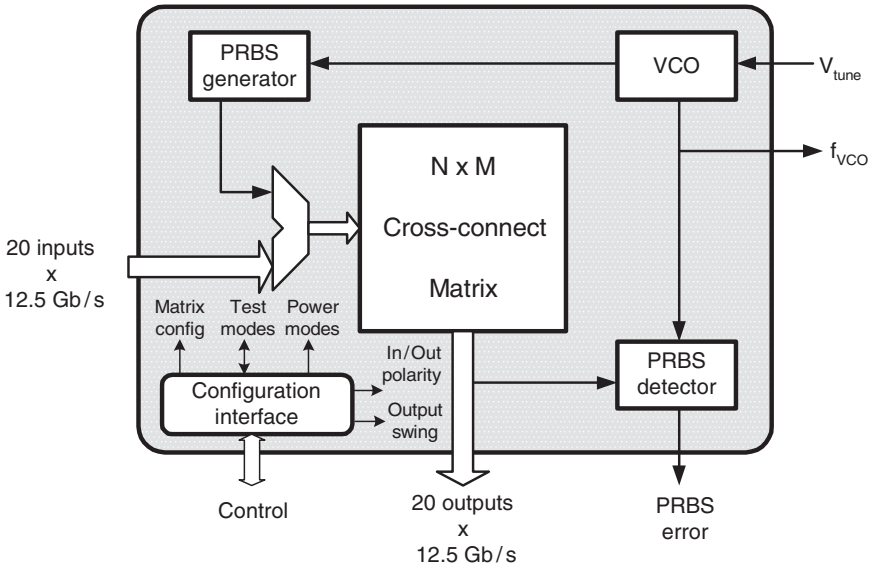


Fig. 1.9 Cross-connect switch based on a matrix architecture

generator and distribution of the PRBS signal to all inputs requires analysis of clock and PRBS data timing and distribution. The IC includes a 12.5 GHz VCO, to drive the on-chip PRBS generator and error detector.

Thus, the 12.5 Gb/s cross-connect switch IC described in Chapter 4 is an example realization of high bit-rate signal distribution and circuit design. It builds on the interconnect design and modelling techniques described in Chapter 2 and the transistor analyses based on device metrics described in Chapter 3.

To implement a similar cross-connect switch function operating at up to 40 Gb/s per input is a major challenge, and forms the framework for the building blocks employed in the rest of this book. A factor of almost 4 in speed improvement is needed in relation to the cross-connect switch described in Chapter 4. This speed improvement will come only partially from IC technology improvements (e.g., increase of f_T). Consequently, improved circuit techniques are needed to achieve 40 Gb/s.

While the cross-connect switch described in Chapter 4 operates from a supply voltage $VCC \approx BV_{CEO}$, achieving the highest possible bit-rate for a given IC technology requires typical supply voltages well above BV_{CEO}. The problems relating to circuit operation at $VCC > BV_{CEO}$ will be addressed in Chapter 5. The challenges relating to the design of high bit-rate digital functions will be discussed within the context of a PRBS generator targeting 40 Gb/s operation in Chapter 6. The challenges relating to the design of a 40 GHz VCO will be addressed in Chapter 7.

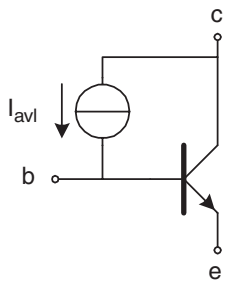
1.4 Transistor Operation above BV_{CEO}

Another critical device parameter for RF circuit performance is BV_{CEO}, defined as the collector-emitter breakdown voltage in the open base configuration. This configuration does not occur frequently, since a relatively low impedance is typically seen from the base terminal to ground in high-speed circuits. Depending on the circuit topology, collector-emitter voltages above BV_{CEO} may be tolerated. Still, BV_{CEO} is an important parameter for the design of such circuits since it is related to the maximum useable collector-emitter voltage and thereby the possible circuit topologies.

Bipolar circuits with a supply voltage VCC above BV_{CEO} are common today. The trend towards lower breakdown voltages of modern IC processes is driven by the fact that a lower breakdown voltage BV_{CEO} usually allows a higher f_T. For a given IC technology and transistor structure, a trade-off between f_T and BV_{CEO} can be realised via the emitter to collector distance L. By approximation, the breakdown voltage scales via $BV_{CEO} \sim L$, while the transition frequency f_T scales via $f_T \sim 1/L$. The theoretical maximum attainable product $f_T \cdot BV_{CEO}$ is for silicon (Si) processes limited to $\approx 200\,\text{GHz} \cdot \text{V}$, often referred to as the Johnson limit [38]. Although modern SiGe:C processes surpass the Johnson limit, the trade-off for a given IC process generation remains valid. The Johnson limit has recently been re-evaluated and is now believed to be $\approx 500\,\text{GHz} \cdot \text{V}$ [39].

The trend towards lower BV_{CEO} of modern SiGe and SiGe:C IC technologies, down to 1.4 V [29] combined with a typical V_{be} of 0.9 V, requires the

Fig. 1.10 NPN with collector-base avalanche current source I_{avl}



use of $VCC > BV_{CEO}$ for many applications. Limiting the supply voltage to $VCC < BV_{CEO}$ results in unconditional circuit safety against breakdown, but limits possible circuit topologies and thereby the maximum attainable speed. High-speed broadband circuits make extensive use of (dc-coupled) emitter followers, and thus require a supply voltage of several Volts.

When a transistor is operated at a collector-emitter voltage $V_{ce} > BV_{CEO}$ (and the base terminal is not open-circuited), the base terminal current flows out of the base terminal. This is due to the avalanche multiplication current from the base-collector junction, indicated as I_{avl} in Fig. 1.10. This avalanche multiplication current is generated due to impact ionisation [30].

From the circuit point of view, base current resulting from avalanche multiplication must be analysed and managed in the design. For example, high-speed current-mode logic such as emitter-coupled logic and double emitter-coupled logic (ECL and EECL) require supply voltages of 3–5 V, depending on common-mode biasing and the number of stacked logic inputs.

In ECL circuits, the (current-mode) logic functions, implemented using stacked and/or cascaded differential pairs, are coupled via single emitter followers. In EECL circuits, the logic functions are coupled via two cascaded emitter followers. Both ECL and EECL circuits are examples of current-mode logic implementations. Due to the low current gain $\beta(f) = i_c/i_b$ of transistors operating close to their f_T, cascading two emitter followers can increase the impedance transformation ratio and thereby reduce the input capacitance of the buffering/coupling function, making the EECL style preferable to ECL for high-speed logic [17].

The EECL current-mode logic buffer circuit shown in Fig. 1.11 demonstrates that some transistors in CML circuits may operate at $V_{ce} > BV_{CEO}$ under certain operating conditions.

In this circuit, $I \cdot R$ equals the logic swing (which is typically 0.2 V), V_{be} equals a base-emitter voltage and V_{deg} equals the degeneration voltage of current mirror Q_7/Q_8.

This circuit can be operated at supply voltages exceeding BV_{CEO}. For transistor Q_1, V_{ce} will not exceed $V_{be} + I \cdot R \approx 1.1\,V$. Similarly, for Q_2 and Q_3, V_{ce} will not exceed $\approx 2.0\,V$ and $\approx 2.9\,V$, respectively. These V_{ce} may exceed BV_{CEO}. To avoid this, diodes may be added in series with the collectors.

The bias current of differential pair Q_3/Q_6 defines the logic swing, and is generated using a bias current source Q_7. The collector-emitter voltage of the bias current transistor Q_7 in Fig. 1.11 equals