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Switched-Capacitor Techniques for High-Accuracy Filter and ADC Design

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ABSTRACT

In this book, switched-capacitor (SC) techniques are proposed which allow the attainment of higher *intrinsic* analogue accuracies than previously possible in such application areas as analogue filter and analogue-to-digital converter (ADC) design. The design philosophy is to create the required functionality without relying on trimming or digital calibration means but instead to develop methods which have reduced dependence on both component matching (especially capacitor matching) and parasitic effects (especially parasitic capacitance).

At a system level, orthogonal design procedures are employed which ensure that artefacts due to expected circuit imperfections are avoided in the system transfer function. For instance, in SC filter design, *orthogonal-hardware-modulation* helps alleviate the effects of *N*-path mismatch through the introduction of an extra degree of freedom, where the number of hardware paths *N* (*hardware modulation*) is decoupled from the *functional modulation* factor *n*, as introduced by the transformation $z \rightarrow z^n$. In algorithmic ADC design, both cyclic and pipelined, conventional techniques make use of multiplying digital-to-analogue converters (or MDACs) which require SC circuits with accurate capacitor ratios to implement accurate signal multiplication. On the other hand, in this book, the ADC function is decomposed into the simple sub-functions of signal addition and level shifting which can be implemented using SC techniques which don't rely on accurate capacitor ratios.

At circuit level, *delta-charge flow* $(\delta\text{-}Q)$ techniques are employed to realize SC circuits with more accurate transfers than their conventional *charge-transfer* (*QT*) counterparts. Unlike *QT* SC circuits, δ-*Q* SC circuits do not require signal charge transfer from capacitor to capacitor via the amplifier virtual earth node. Instead, only a delta charge δQ flows in the virtual earth node due to the presence of parasitic capacitors at the amplifier input terminals. In SC filter design, *delta-charge-redistribution* $(\delta\text{-}QR)$ is a means for the accurate implementation of filter transfer functions using passive charge redistribution between capacitors in the feedback path of an amplifier, instead of active charge transfer between capacitors through the active intervention of an amplifier in *QT* SC filters. In ADC design, a highly accurate method (*C*+*C*) for the stacking of capacitor voltages is proposed which uses a *floating-hold-buffer* for implementation. The accuracy of signal addition is practically insensitive to the matching and linearity of the signal capacitors as well as the presence of parasitic terminal capacitance.

A number of other innovative circuit techniques have been included in the book, such as: a versatile accurate track-and-hold (T&H) which is re-programmable for unipolar, bipolar and

differential modes; clock-skew insensitive sampling; a common-mode-feedback circuit which significantly boosts the common-mode rejection ratio of single-ended amplifiers; high-efficiency dual-input transconductance amplifiers which make use of the level shift properties of switched capacitors; a low-reference dynamic comparator.

The validity of the concepts developed and analyzed in the book has been demonstrated in practice with the design of CMOS SC bandpass filters and algorithmic ADC stages (both cyclic and pipelined). The intrinsic accuracies achieved go beyond those achieved with previous state-of-the-art solutions with a consequent reduction in power consumption for the same speed applications. For example, a 10.7MHz radio IF selectivity filter integrated in standard CMOS, employing the proposed methods, achieves an accuracy greater than ceramic filters. Another example is an ADC with better than 12-bit intrinsic performance, albeit capacitors with only 9-bits matching accuracy were used in the realization. The ADC architecture is also very robust and has proven itself in an embedded digital VLSI application in the very newest 65nm CMOS. The power consumptions and silicon areas of the solutions proposed here are lower than other known solutions from the literature.

CONTENTS

SYMBOLS AND ABBREVIATIONS

Symbols

A_0	Amplifier DC gain
B_x	Spectral bandwidth of x, where x is RF, IF, or ch (channel)
C_{fb}	OTA external feedback capacitance
C_{in}	OTA external input capacitance
C_L	OTA external load capacitance
$C_{L_{fix}}$	Permanently connected amplifier external load capacitance including parasitics
$C_{L_{sw}}$	Switching amplifier load capacitance
C_{Leff}	Effective load capacitance the amplifier sees at its output
C_{ox}	Gate capacitance per unit gate area
f_s	Sampling frequency
f_{sig}	Signal frequency
g_m	The small signal transconductance defined at the bias current
L	Effective gate length of MOST
m	Discrete time variable
Q	Quality factor
QT	Charge transfer (SC circuit), where signal charge is transferred completely from one capacitor to the other through the active intervention of an amplifier
r	Pole radius in z-domain
s	Laplace frequency variable
S	Scaling factor
T	Sampling period
t_{slew}	Slewing time
V_{REF}	Reference voltage
V_{DD}	Supply voltage
V_{on}	The MOST "on" voltage, or gate over-drive voltage, defined as V_{GS} - V_T, required to keep the MOST biased at the edge of saturation with all voltages and currents fixed at their DC bias levels
$V_{ds(sat)}$	Defined as V_{gs} - V_T, it is the minimum instantaneous drain-source voltage required

	to ensure the MOST stays in saturation
V_{margin}	Extra voltage safety margin above V_{on} to ensure MOST stays biased in saturation - generally, $V_{ds(sat)} < V_{on} + V_{margin}$
v_{sat}	Maximum charge carrier velocity in silicon (1.1×10^5 m s^{-1})
$V_{T_p}\left(V_{T_n}\right)$	Threshold voltages for PMOSTs(NMOSTs) - note V_{T_P} is assumed to be positive
W	Effective gate width of MOST
X_Y	DC bias value of x, with y the descriptor - x is generally a current, i, or a voltage, v
x_y	AC value of x with y a descriptor
X_y	Total instantaneous value of x, where $X_y = X_Y + x_y$
z	z-domain frequency variable
β_{fb}	Closed loop amplifier feedback factor
δ-Q	Delta charge flow technique referring to a new class of SC circuit
δ-QR	Delta charge redistribution
Δ	Quantization step size of a data converter (analogue equivalent of 1 LSB)
ε_s	Static settling error resulting mainly from finite amplifier DC gain
ε_d	Dynamic settling error resulting mainly from finite amplifier bandwidth
ε	Total combined settling error of a SC circuit at the end of a clock period
φ_x	Defines a clock phase x
γ	Attenuation factor due to capacitive division from the signal input of a SC circuit to the differential input of the OTA
κ	Ratio of OTA output parasitic capacitance to its input parasitic capacitance
μ_{eff}	Effective inversion layer charge carrier mobility, including the effect of vertical field mobility degradation
μ_0	Inversion layer charge carrier mobility, when low vertical field (typically, 5x10^{10} μm^{2}V^{-1}s^{-1})
θ	Process dependent factor inversely proportional to the oxide thickness (typically, $24\,\text{Å}/d_{ox}$ V^{-1})
$\sigma(\Delta X)$	Standard deviation of ΔX
τ	Time constant of linear step response
ω_{cl}	Closed loop bandwidth in radians/s
ω_{ol}	Open loop bandwidth in radians/s
ω_T	Radial transition frequency
ω_u	Unity gain radial frequency, where the gain of the amplifier is reduced to 1
$\|\|$	In parallel with (used for parallel combinations of resistors or capacitors)

Abbreviations

ADC	Analogue-to-digital converter
ASD	Analogue sampled data
ASIC	Application specific integrated circuit
ATE	Automatic test equipment
BIST	Built-in-self-test
BPF	Bandpass filter
CAD	Computer aided design
CMFB	Common mode feedback
CMOS	Complementary metal oxide semiconductor
CMRR	Common mode rejection ratio
DAC	Digital-to-analogue converter
DEC	Digital error correction
DITO	Dual-input telescopic OTA
DNL	Differential non-linearity
DS	Double sampling
ENOB	Effective number of bits
FD	Fully differential
FOM	Figure of merit
FPGA	Field programmable gate array
FS	Full scale (of ADC)
GBW	Gain-bandwidth (defined in radians per second)
HF	High frequency
HPF	Highpass filter
IC	Integrated circuit
IF	Intermediate frequency
IMD	Intermodulation distortion
I/O	Input/output interface
INL	Integral non-linearity
IP	Intellectual property (block)
ITRS	International Roadmap for Semiconductors
LF	Low frequency
LHP	Left half *s*-plane
LHS	Left hand side
LPF	Lowpass filter
LSB	Least significant bit
MDAC	Multiplying DAC
MOST	MOS transistor
MSB	Most significant bit
OHM	Orthogonal hardware modulation

OSR	Oversampling ratio, f_s/f_{sig}
OTA	Operational transconductance amplifier
PM	Phase margin (in degrees)
PSRR	Power supply rejection ratio
PVT	Process, voltage supply and temperature variations
RF	Radio frequency
RGC	Regulated cascode - this term is used interchangeably with the term active feedback cascode
RHP	Right half *s*-plane
RHS	Right hand side
RMS	Root mean square
S&H	Sample-and-hold
SNR	Signal-to-noise ratio
SC	Switched-capacitor
SE	Single-ended
SEM	Scanning electron microscope
SiP	System in package
SITO	Single-input telescopic OTA
SoC	System-on-a-chip
SR	Slew rate
SS	Single sampling
T&H	Track-and-hold
VHF	Very high frequencies
VLSI	Very large scale integration

CHAPTER 1

INTRODUCTION

Silicon technology, and in particular some variant of CMOS, will be around for many years to come [1],[2]. CMOS is the most appropriate technology for implementation of single-chip solutions, not just because of the ease of combination of RF, analogue, and digital circuits on one substrate but because of the extensive range of intellectual property (IP) available. Analogue processing will always be on chip because of the ever present need of a digital-signal-processor (DSP) to interact with the real analogue world. For example, some 70% of all microcontroller revenue is generated by microcontrollers containing embedded analogue-to-digital converters (ADC) with a resolution of 8-bits or more [9]. Indeed, analogue-digital interfaces are rapidly becoming the performance bottle-neck to the advancement of system-on-a-chip (SoC) solutions in leading-edge CMOS processes. Moore's Law has come to mean that the number of transistors on the same size chip doubles every two years [4] (originally every three years[3]). DSP capability has, indeed, increased by two orders of magnitude in the past decade. On the other hand, ADC resolution, for each application frequency range, has increased by only 2-bits in the same period of time! [5]. Thus, the major analogue IC design challenges are still in the area of analogue-to-digital conversion (ADC) and accompanying analogue signal conditioning circuitry [6]. There continues to be a disparity between what ADCs can deliver and what integrated digital-signal-processing systems demand. According to the latest 2005 ITRS perspective [8], at the current rate of ADC evolution, it will take another 22 years before present day all digital receivers can be fully integrated!

1.1 Cost-Performance Trade-offs in IC Design

The product and/or chip architect needs to adopt appropriate techniques to get the best cost-performance trade-off using the latest available combination of user/market data, technology and best design practices. The product is only viable at a certain cost. For that cost, a minimum combination of user features must be integrated which meet a minimum performance specification.

There is a reciprocity at work in the relationship between cost and performance. For this

reason, cost is placed at the nucleus of the diagram of Fig. 1.1, while performance is represented by the outer bands. Three unique bands are identified which define the processes at work in the definition phase of a new chip product. At each level, there are trade-offs that inter-play at that level. The outer band is the user- or, indeed, human-interface ring in which issues such as functionality, product specification, innovation and time-to-market are pre-dominantly in the hands of the people engaged in the design. The middle ring represents the technologies available for implementation of the product definition distilled out of the outer ring. Finally, the inner ring represents the fundamental design space trade-offs (namely power, speed, accuracy and die area [10]) which are required to be combined in some optimal way to ultimately create a chip product to specification which is cost efficient.

A specific example of the cost-performance trade-off is in the area of IC technology. As technology shrinks, overall digital performance improves (but at the cost, for instance, of new process development, increased power density, increased leakage, etc.), while analogue performance deteriorates. CAD tools need to be updated to cope with the extra complexity and demands of each technology generation and transistor and interconnect models need to be updated with the new process parameters before complex VLSI design can be undertaken. Hence, a sweet-spot needs to be found per product per technology generation for the best balance between cost and performance.

1.2 Modern IC Design Challenges

There is a major drive to single chip solutions for system implementations of many diverse mixed-signal consumer and telecommunications products. These days, it is neither economical, nor indeed robust design practice, to have critical components, such as analogue-to-digital converters (ADCs), filters and digital-to-analogue converters (DACs) off-chip. The first billion transistor chips are coming on to the mass consumer market. This rapid evolution is being fuelled by the rapid advance of deep sub-micron CMOS technologies through aggressive scaling according to Moore's Law [4], [11].

Continual improvement in overall performance of digital VLSI is the driving factor to continual CMOS technology scaling (with scaling factor S). The most direct improvements are:

- Lower cost per transistor - with $\sim S$ - (although transistor density increases with $1/S^2$, wafer processing costs also go up by $\sim 1/S$ per generation);
- More transistors per unit area - with $\sim 1/S^2$;
- Lower power consumption per digital function per unit load - with $\sim S^2$ (mainly due to voltage scaling);
- Higher speed - with $\sim 1/S$ (mainly due to capacitor down-scaling, lower threshold voltages, and lower resistance interconnect).

There are, however, significant limitations to device scaling which are already beginning to impact current CMOS processes (90nm, 65nm). The ability to scale down the lithography through ever smarter mask creation techniques is not at issue. The main concern is the fundamental ability of transistors to continue to operate properly with continued scaling [12]. This affects digital and analogue IC design in different ways.

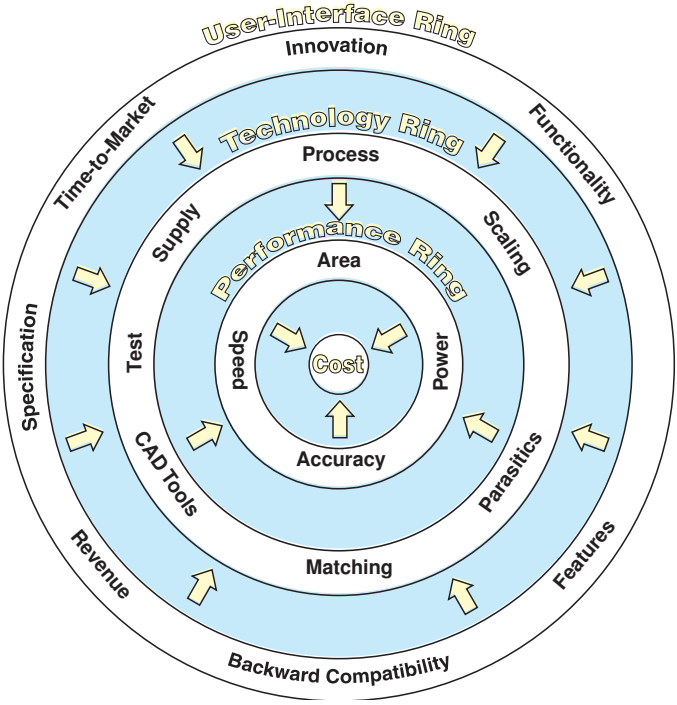

Fig. 1.1 *Cost-Performance reciprocity for new generation products.*

1.2.1 Digital IC Design Challenges

The main challenges in digital IC design come from continued process scaling and these are summarized in the following bullet points:

- One of the major issues for continued digital scaling is soft errors, where the energy stored on a gate is continually scaling to such an extent that extraneous high-energy particles can simply discharge it. Error correction can help alleviate this but at the cost of extra resources and power dissipation.
- Another issue is gate leakage through the inability of a transistor to fully switch off with lowering supply voltages (due to the reducing threshold voltages required to compensate for reduced switching speed with lower supplies), as well as gate leakage caused by the reduction of the thickness of the gate-oxide.
- Power density is increasing with every new technology generation [12]. Increasing transistor densities means that designers can place more functionality on chip every generation. Increased transistor leakage also means that a chip wastes more power in idle mode. Chip area is also increasing per generation due to improved wafer processing. 300mm wafers are now standard for the latest commercially available 65nm technology,

so that die sizes of greater than $1cm^2$ are now easily manufacturable [11]. Hence, increased chip area, combined with increased power density, means that total SoC power is increasing at the rate of 50-100% per CMOS generation [13]. While the overall system/board level solution can have a dramatic reduction in power consumption through the continued integration of key functions on chip, the increased power consumption on chip reduces chip reliability.

- Electromigration (EM) deserves a mention, where decreasing metal width causes increasing current density (with $1/S$) which can cause interconnect to break.

1.2.2 Analogue IC Design Challenges

The analogue designer must usually make do with a CMOS process crafted for digital performance. Only the second point from the previous section is a main point of concern for integrated analogue circuits when subject to device scaling. While high performance digital circuits require switches to be fast with leakage a secondary (power) concern, analogue circuits must have *both* fast and low-leakage switches. In analogue circuits, gate and drain leakage currents contribute to static power consumption *and* leakage from sampling capacitors. This leakage current corrupts sampled signals, degrading analogue performance. The primary concern, though, for analogue IC design, is the scaling down of supply voltage that accompanies device shrinkage in new processes[7]. This has a number of detrimental consequences:

- While digital power consumption reduces quadratically with reducing supply voltage, analogue power consumption increases linearly with reducing supply voltage for the *same* operating precision [section 7.7.2].
- Transistor gain reduces for a given aspect ratio and given V_{margin}. The obtainable gain of the MOS transistor is a factor ~S per generation smaller than predicted using the square-law model [14], [15]. This is primarily due to the lowering of the output resistance from short channel effects, whereas transconductor efficiency $\left(g_m/I_{ds}\right)$ doesn't change much. Note that new wafer processing techniques, such as strained silicon, can offset this effect somewhat.
- Dynamic range reduces, on the one hand because of reduced headroom, and on the other hand because of increased noise (greater device thermal and flicker noise - due mainly to smaller physical sizes - and greater digital noise coupling from faster clock rates), as well as increased device non-linearity.
- Although component matching improves due to the more accurate lithography of each technology generation, it does not directly track the accompanying lowering of supply voltage. Hence, mismatch-induced offsets become an increasing fraction of signal levels, causing a reduction in circuit reliability.

1.2.3 Test Challenges

Test is becoming an increasingly important constituent, and in many cases a gating item, of the overall cost-performance design space for large scale VLSI SoCs. The cost of test does not directly scale with process technology, die size, nor pin count [7]. The use of traditional exter-

nal test methods on automatic test equipment (ATE) is becoming less feasible for SoC devices, since such SoCs have only a limited number of I/O (input-output interfaces) while more and more IP cores are being co-integrated on the same die.

To help improve testability, Design for Test (DfT) methodologies are becoming an inherent part of the IC design process which require consideration at the outset of product planning [17]. While DfT for digital test is firmly established, DfT for mixed-signal test remains a challenge. One approach is model based testing [18] which relies on reduced performance testing of mixed-signal blocks and then extracting complete test information through making use of established models of the analogue block architectures. Another approach is built-in-self-test (BIST), in which mixed-signal parts of the SoC effectively test themselves and create test histograms which can be read from user-defined test registers by a JTAG bus interface to the ATE. Indeed, the value proposition of BIST is becoming more attractive as the cost of implementing complex hardware solutions on chip gets cheaper. Smart on-chip BIST [19] can offer a way forward for testing complex mixed-signal SoCs which can help alleviate the conflicting requirements of shorter test times and increasing test accuracies per mixed-signal function (especially embedded data converters). ASICs require the implementation of dedicated hardware routines for the sake of BIST. On the other hand, programmable general purpose chips, such as DSPs and FPGAs, can make use of their own re-programmable resources to implement very complex test routines for both digital and mixed-signal BIST just for the purposes of speeding up final test.

1.2.4 Process and Design Work-Arounds

Experts are no longer declaring that CMOS will soon hit a brick-wall [4] because every time this appears to be the case, both process and chip designers innovate their way past the current set of barriers. Process improvements include low-*k* dielectric, for reduced interconnect capacitance and increased device efficiency $\left(g_m/I_{ds}\right)$, strained silicon, etc. Process work-arounds include self-adaptive silicon with intelligent voltage regulation of moated n-wells and p-wells, as well as power supplies, in order to “centre” the silicon for the device specification (e.g. [20]). Design work-arounds include error-correction, self-calibration, smart power-down, sleeper transistors, etc.

The increasing cost of manufactured CMOS devices means that extra process options, such as thick-oxide devices and moat isolation, add relatively little to the overall cost. Such extra options are now standard on all leading-edge CMOS processes. In this way, advanced innovative integrated analogue circuitry can co-exist with the latest deep-submicron digital circuitry on the one substrate (e.g. 65nm mixed-signal SoC, Chapter 10 [11]). Not just sensitive analogue circuitry but digital circuitry too benefit from improved performance and reliability. Indeed, most digital ICs need to interface with the real analogue world, which require I/O to work at a voltage much higher than present day digital transistors allow (e.g. 2.5V I/O but standard 1V transistors in the 65nm Xilinx Virtex-5 FPGA [136]). Alternative solutions can be implemented in the packaging arena using System-in-a-Package (SiP) solutions, where a leading edge digital die co-exits with a mixed-signal die from an older technology either on the one

package substrate, or as stacked dice. SiP solutions are still very expensive when compared to dual-oxide, moated leading-edge digital processes.

1.3 Switched Capacitors for Analogue Signal Conditioning

Switched capacitor (SC) analogue sampled-data-processing is a proven excellent candidate for implementing critical analogue functions before entering the digital-signal-processing domain in an embedded mixed-signal environment. SC circuits, for embedding in digital VLSI, are attractive for a number of reasons:

- Implementation is fully compatible with modern digital CMOS, requiring just:
  - Amplifiers (whose only requirement is to reach end-values between clock transitions, so that non-linearities are tolerable: DC gain and bandwidth are the key parameters - see Chapter 4);
  - Capacitors (metal interconnect capacitors are sufficient in most cases);
  - Clocked switches.
- Accuracies of key parameters depend on a stable clock frequency (primary parameters) as well as capacitor *ratios* (secondary parameters) and remain accurate with temperature and aging.
- Easy migration to the latest CMOS processes with only limited small signal parameters and matching data necessary.
- Benefit from technology down-scaling by virtue of the linear down-scaling of capacitors, even if a thick-oxide technology option is used alongside the thin-oxide digital.
- No tuning required.
- Re-configurability and re-programmability which can co-function with re-configurable logic.
- Analogue memory and accurate long time-constants.
- Easier functional self-testing, more aligned to digital functional self-test than pure analogue self-test.

1.4 Key Points for High Performance SC Design

SC circuits come in many forms but a number of key design points should be followed to ensure that the chosen implementation has low distortion and low power and is area efficient, robust, and sufficiently accurate. This is especially important for high-performance SC band-pass filters and SC based Nyquist-rate ADCs which aim to squeeze the best out of the IC process. The main points to consider are summarized here:

- Parasitic-insensitive configurations should always be chosen.
  - Configurations centred around closed loop amplifiers are key to achieving this.
  - Avoid transfer dependency on top/bottom plate capacitors, as well as amplifier input and output capacitance.
- No signal-dependent charge-feedthrough or clock-feedthrough on to signal capacitors.

- Balanced differential design and early clocking (e.g. early switching of amplifier input nodes) are key to achieving this.
- Single charge transfer between stage input and output.
  - Avoid serial connection of capacitors and/or amplifiers. Use parallelization where possible.
- Circuit configuration should not change with clock phase.
  - With no clock phase dependency, the circuit can be optimized to operate in one configuration only.
- Avoid continuous-time paths via the amplifier between SC block input and output.
- For accurate bandpass filters, the sample clock should be used to primarily determine the centre frequency f_0, whereas a simple capacitor ratio should be used to determine the Q.
  - The clock is the highest accuracy design parameter in the system, so that it alone should set the most critical specification, i.e. f_0, The next most accurate design parameter is capacitor matching so that this should be used to determine the next most critical specification, the Q.
- Maximize amplifier settling time to full sample clock period through the use of double-sampled or N-path techniques.
- Optimize SC circuit configuration such that amplifier feedback factor can be maximized and amplifier loading can be minimized - this ensures power efficiency.
- Create error budget and distribute over all error sources such that no one error dominates
  - Establish all static and dynamic error sources (see presentation in section 8.2.1).
  - Establish critical specifications which must be achieved, e.g. f_0 accuracy, signal range, linearity, noise, etc.
- Include all interface circuitry in final modelling and simulation, especially reference generation, bias circuitry, clock circuitry, etc.
  - Simulations should be done across PVT corners and include full RC extraction with Monte-Carlo analysis.

1.5 Scope of Book

Conventional SC circuit techniques are primarily limited in accuracy by a) capacitor matching and b) the accuracy with which a differential amplifier can squeeze charge from one capacitor to another in a given time frame, usually one sample-clock period. Alternative strategies to such conventional SC approaches that achieve higher accuracy is the main focus of this book. The techniques proposed are analogue based and enable the achievement of more accurate system specifications than previously possible. The new techniques are just as amenable to further digital accuracy enhancement via calibration and/or correction as traditional methods. Two popular application areas are explored in the course of this book for exploitation of the proposed techniques, viz. SC filters and algorithmic ADCs - both cyclic and pipelined. Furthermore, efficient system level design procedures are explored in each of these two areas.

1.6 Book Organization

The main ideas used to achieve high-accuracy in SC design are introduced in Chapter 2. Orthogonal design procedures in SC filter and ADC design are introduced. Proposed delta-charge-flow SC techniques are presented at conceptual level and compared against traditional charge-transfer approaches.

The next two chapters deal with the design of amplifiers for SC applications. Chapter 3 presents SC amplifier design at black-box level and homes in on the specific aspects of amplifier design for SC circuits. Chapter 4 examines amplifier architectures and explores design strategies suitable for SC applications.

Chapters 5 and 6 are dedicated to SC filter design. The concepts of orthogonal hardware modulation and delta-charge-redistribution are exploited in Chapter 5 for the design of low-sensitivity and high-accuracy SC bandpass filters. Reduced sensitivities of centre frequency and quality factor to component mismatch is demonstrated and evaluated for the proposed bandpass filters. The realizations of SC bandpass filters in standard CMOS, making use of the concepts developed in Chapter 5, are presented in Chapter 6. Very high accuracies going beyond previous state-of-the-art proposals are demonstrated for TV and radio applications.

The following four chapters are allocated to ADC design with special emphasis placed on the contributions of the proposed concepts to improved ADC performance. Chapter 7 deals with ADC design at black-box level. Models are presented to aid ADC analysis, while minimum theoretical and practical power limits are derived in terms of conversion accuracy and sample rate. Chapter 8 is devoted to the detailed analysis of algorithmic ADCs, both cyclic and pipelined. The effects of errors on the ADC transfer are demonstrated and error bounds derived. The improved overall performance of a pipelined ADC through the use of hardware scaling and a multi-bit front-end stage is analyzed. A model is proposed to estimate the power per stage and overall power consumption of a pipelined ADC. A new implementation for algorithmic ADCs, both cyclic and pipelined, is proposed in Chapter 9. The realization of the floating-hold-buffer is developed and applied to the creation of a new 1.5-bit stage which is the key component of these ADCs. Overall improved performance, including reduced sensitivity to capacitor mismatch, compared to traditional algorithmic ADC design methods is demonstrated. Chapter 10 presents practical realizations of ADC circuits based on the new methodologies. A 12-bit algorithmic ADC requiring no calibration or correction or compensation routines is developed. Included in the ADC system is a versatile track-and-hold based on the floating-hold-buffer, which can handle a number of different types of analogue inputs and transform them into a differential sampled-data signal for further processing by the core ADC. The ADC is embedded in 65nm CMOS in a complex SoC and proven to be very robust. Two pipelined ADCs with hardware scaling have been designed with two separate specifications, namely high-accuracy, medium-speed and medium-accuracy, high-speed.

Finally, in Chapter 11, general conclusions are drawn based on the work presented in this text.

CHAPTER 2

KEY CONCEPTS FOR ACCURATE SC DESIGN

Analogous to noise, it is possible to improve matching by increasing the areas of the devices to be matched [16]. In contrast to noise, though, it is possible to achieve accuracy beyond the effective matching of components through either a) trimming, b) correction/calibration, or c) innovative circuit techniques. This final option is explored in this book in the area of switched-capacitor (SC) design, where the primary block specification is not allowed to be dependent on simple component matching only (here signal capacitors). Two areas are chosen to demonstrate this, viz. high-accuracy bandpass filter (BPF) design and high-accuracy analogue-to-digital converter (ADC) design. For BPFs, the centre frequency f_0 is the primary specification, followed by the Q-value. For the widely used algorithmic ADCs (i.e. the cyclic and pipelined ADCs), the primary block specification is the accuracy with which the functions $\times 2$ and $\pm V_{ref}$ can be realized. The accuracy of realization of these key functions determines the accuracy of the whole ADC (see Chapter 8).

The ability to achieve higher functional accuracy beyond the accuracy of component matching alone through improved analogue means (c), has a direct knock-on effect in lower cost and lower power and area compared to (a) and (b) above. Note that digital calibration means is not advocated against here. Instead, it is advocated that analogue innovation needs to be explored first to obtain a reasonable solution before digital calibration needs to be employed. Undoubtedly, digital calibration will play an increased role in improved overall performance but generally speaking, for any given technology, an analogue solution to an analogue problem will outweigh a digital solution to an analogue problem. The analogue solutions should be portable across process generations and not rely on the vagaries of the particular process the circuits are designed in. In this respect, the solutions presented here for SC design are as portable from technology generation to generation as conventional SC techniques.

The main techniques used to achieve high-accuracy in SC BPF and ADC design are explored at conceptual level only in this chapter. This sets the scene for the rest of the book.