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Koushik Maharatna
Goutam Kumar Dalapati
P.K. Banerjee
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Editors

Computational Advancement in Communication Circuits and Systems

Proceedings of ICCACCS 2014

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Message from Convener

It is our pleasure to introduce the proceedings of the First International Conference on Computational Advancement in Communication Circuits and Systems (ICCA-CCS 2014) in relation to complex issues of communication circuit and system with the analysis of computational techniques. The conference aims to create a forum for further discussion on integrated information in the significant field incorporating a series of issues.

The relevance of the conference theme, to a wide variety of disciplines, is reflected in the diverse range of papers submitted. The link between Electronics and Communication Engineering and Soft Computing strengthens the area of research to be presented and provides the precise information required for assessment. The international delegates like Profs. Christophe Fumeaux, Australia; Arokiaswami Alphones, Singapore; I-Fang Chung, Taiwan; Chia-Feng Juang, Taiwan; and Sajjan G. Shiva, Memphis were highly impressed and have shown a high level of international interest in the subject.

The level of interest in the subject matter of the conference was maintained by submitting 122 suitable papers at the conference. Every submitted paper went through a precise review process. Each paper received at least three reviews; where issues remained, additional reviews were commissioned. Finally, 62 papers were selected by 40 reviewers for presentation in four different tracks like Microwave and Devices, Communication and Networking, Signal and Image processing, and Computations, Mathematics and Control.

Finally, we would like to record our appreciation to the Organizing Committee members for their work in securing a substantial input of papers to make the conference successful. We are also indebted to those who served as reviewers and chairmen; without their support, the conference could not have been the success that it was. We also acknowledge the authors themselves, without their expert input there would have been no conference.

November 2014

Prof. Dr. M.R. Kanjilal
Convener ICCACCS 2014

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Part VIII Advances in Image Processing

About the Editors

Dr. Koushik Maharatna received his B.Sc. in Physics and M.Sc. in Electronic Science from Calcutta University, Calcutta, India in 1993 and 1995 respectively. He received his Ph.D. degree from Jadavpur University, Calcutta, India, in 2002 for his thesis, "CORDIC-based signal processors for biomedical applications".

In February 2000 he joined the Institute for High-Performance Microelectronics (IHP), Frankfurt (Oder), Germany, as a Research Scientist where he was involved in the BMBF-funded projects "Wireless Broadband Networks" (WBN) and IBMS2, both of these projects targeted low-cost low-power implementations of the IEEE 802.11a and Hyperlan/2 standards. His work in IHP resulted into four patents and several research publications in prestigious IEEE journals and conferences. In August 2003, Dr. Maharatna was appointed as a Lecturer in the Dept. of Electrical and Electronics Engineering (EE), University of Bristol, UK and in October 2006, he joined the School of Electronics and Computer Science (ECS), University of Southampton, UK, as a Senior Lecturer where he is a Reader (Associate Prof.) at present. He is currently pursuing his research vision for next-generation mobile healthcare system development applying his several years of experience in VLSI Circuits & Systems design and signal processing. As part of that he took part in several high-profile ARTEMIS and FP7 funded projects.

Dr. Maharatna has been a member of a number of several prestigious conference programme committees and acted as a session chair in conferences such as IEEE ISCAS 2005, 2007, 2008, 2012, VLSI design conference 2006 etc. He is a member of IEEE VLSI System Application (VSA) Technical Committee and IEEE Plagiarism committee. He has published over 90 research papers in internationally reputed Journals and Conferences. He has also edited the book "Systems design for remote healthcare" published by Springer in November 2013.

Dr. Goutam Kumar Dalapati is working as Scientist-II in the Department of Design and Growth at Institute of Materials Research and Engineering (IMRE, A*STAR), Singapore. He has completed his Ph.D. from Jadavpur University, Kolkata, India in 2005. His research interests include Next generation solar cells; Earth abundant materials for Photovoltaic application ($FeSi_2$, CuO, and CuS);

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Prof. P.K. Banerjee retired Professor of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata, completed his undergraduate, post graduate and Ph.D. programme in the same University in the years 1965, 1967 and 1972 respectively. After completion of his master's degree he joined as senior research fellow to undertake research activities leading to the Ph.D. degree. He joined the department as lecturer in the year 1971 and was subsequently promoted to Reader and Professor. His academic interest is in the field of Communication Engineering with special activities in Digital Communication Systems, RF engineering and allied fields. Currently he is working in the field of mobile Ad hoc network (MANET), MIMO system and its use in different environments. Professor Banerjee has guided a large number of students for their Master's project and also four students for their Ph.D. (ongoing) work. He is also actively involved in guiding both M.Tech and Ph.D. students. Professor Banerjee along with his fellow associates and co-workers published more than 100 technical papers in national and international journals and has one patent to his credit.

Prof. Amiya Kumar Mallick joined All India Radio, Calcutta as Assistant Engineer through the UPSC examination after graduation in Electrical Engineering from Jadavpur University and thereafter postgraduation in Microwave Engineering from Indian Institute of Technology, Kharagpur. On completion of exhaustive training under the Technical Teacher Training Scheme, Government of India, Professor Mallick joined the Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology, Kharagpur as Lecturer in 1967. Finally, Prof. Mallick became Professor of the Department and carried out all his responsibilities, with dignity, as the Head of the Centre for Research and Training in Radar and Communication Engineering. He was also a member of the Senate—the highest academic body of the Institute. Apart from teaching, Prof. Mallick provided leadership and took active initiatives in research and development of the Institute. He was Chairman of various Committees connected with a variety of R&D activities—departmental as well as interdisciplinary in nature. Professor Mallick retired in 2000 from IIT, Kharagpur. Professor Mallick obtained his Ph.D. (Engineering) degree from the Indian Institute of Technology, Kharagpur and produced a number of PhDs under his supervision. He is a Fellow and life member of number of Professional Societies like IE (India), IETE, SEMCE and Associate member of IEEE. Professor Mallick published a number of high quality technical research papers in national and international journals.

Dr. Moumita Mukherjee is working as Senior Scientist at Centre for Millimeter Semiconductor Devices and Systems, Defence Research and Development Organisation, Kolkata, India. Besides her R&D job, she likes teaching and out of that interest, she is attached with the Applied Physics Department, Calcutta University as 'guest faculty'. She completed her Bachelor's and Master's (Physics) from Presidency College, Kolkata, University of Calcutta. Dr. Mukherjee completed Ph.D. (Technology) in Radio Physics and Electronics from Calcutta University. She has authored more than 120 research papers in international journals and also in a number of international research papers/book-chapters/books. Dr. Mukherjee received the Visiting-Scientist' offer from Newcastle University, UK and selected as PDF from Germany, and also obtained "National Merit Scholarship" Award from GOI.

Part I
Advances in RF, Microwave and Antenna

Chapter 1
Design and Development of Low-Level RF Digital Feedback Loop

Synthesized Signal Generator

Arnab Das, Bipa Datta and Moumita Mukherjee

Abstract A controlled synchrotron light source is a specialized particle accelerator, typically accelerating electrons required for scientific and technical purposes. To energize charged particles to the final energy and to compensate the synchrotron radiation loss, RF power is used. To do so, RF cavities are used and power to RF cavities is fed using high power amplifiers (like Klystron for Indus-2 and Tetrode tube for Indus-1, at RRCAT, Indore, MP, India). With the advancement in the field of programmable logical devices and the Hardware description language, digital RF feedback control system using FPGAs is adopted for providing better flexibility, reliability and stability. In phase (I) and quadrature phase, (Q) scheme is used here for extracting the amplitude and phase information about RF signal. By processing information, the EM field inside the RF cavity has stable amplitude control loop (ACL) and phase control Loop (PCL). A new, FPGA-based, digital, low-level RF system, based on an analog I/Q modulator and demodulator, is proposed here for development.

Keywords FPGA · In-phase · LLRF system · Quadrature-phase · Stability

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1.1 Introduction

Low-level RF (LLRF) control systems consist of synthesized signal source, 0–360° phase shifter, feedback loops for amplitude, phase and frequency control, and coaxial RF switch to put RF on and off and limiter. Indus-1 synthesized signal generator giving outputs at 31.613 MHz is developed, which will also be used to get synchronized RF drive signal for Indus-2. Amplitude and phase control feedback loops are incorporated to maintain the amplitude and phase of the cavity gap voltage within ±1 % and ±2°, respectively, for proper operation of the machine [1, 2]. Translation of the amplitude and phase information to I/Q is advantageous because of the symmetry of the I/Q signal paths. This analog I/Q RF system also provides a real function structure to verify the working principle, block functions and performance evaluation for the developing digital low-level RF system [2].

This paper, based on analog I/Q and digital FPGA LLRF systems, presents the designed function diagrams, measured results of the characteristics of the main RF vector components and the integration test of the low-level RF digital feedback loop, while maintaining amplitude in suitable range.

1.2 Design Consideration for Digital LLRF Feedback Loop

1.2.1 Scheme of the Digital LLRF Feedback Control System

Figure 1.1 shows a schematic of the digital LLRF control system, where cavity field is directly down-converted to baseband signals, for which I/Q detection is performed using Spartan 3 DSP protoboard. The resulting I/Q baseband signals that describe the cavity field are also processed using VHDL program for getting controlled output, one for the I signal and another for the Q signal.

In this project we only control amplitude, i.e. work as an amplitude control feedback loop. FPGA-based VHDL program helps DSP protoboard work as a broadband quadrature demodulator with an integrated intermediate frequency (IF) after baseband amplifier and controlled clock signal. It is responsible for converting the low-level RF signal into baseband differential in-phase and quadrature components.

The FPGA-based amplitude controller designs with the help of the differences between the two singles (I/Q) with the set point, because for all measurements founded on AD8345, the input level on each baseband input pin is 0.7 V ± 0.3 V peak [3].

The vector modulator module modifies the I and Q components to produce the desired RF drive signal for the klystron according to the PI controller signal. The AD8345 is used to perform I/Q up-conversion [3]. The component provides excellent specifications of amplitude and phase balance and sideband suppression.

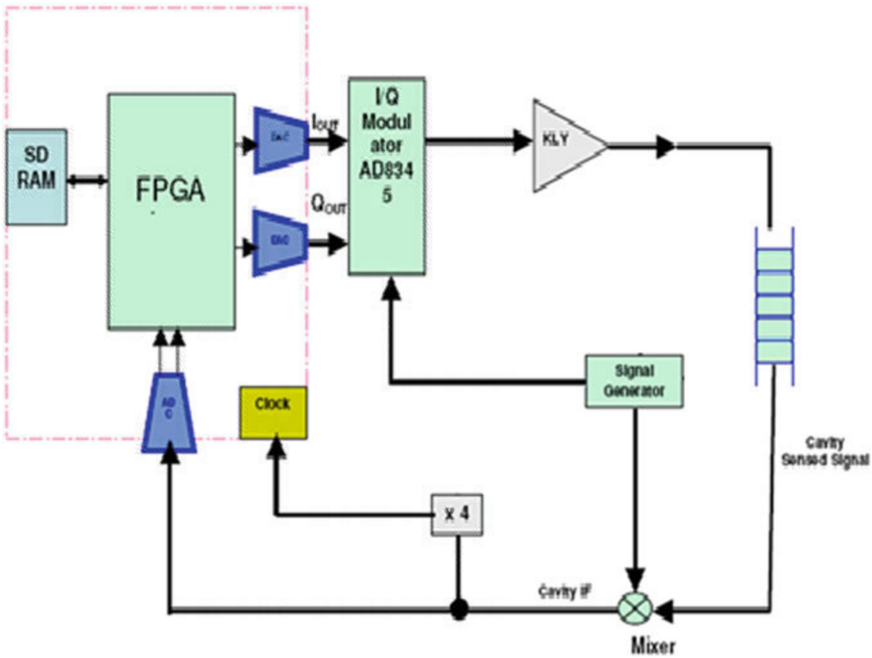

Fig. 1.1 Block diagram of the digital LLRF feedback control system

1.2.2 I/Q Feedback-Control Module

The digital I/Q feedback-control module is the central controller of the feedback system, providing the following controls.

1. Two input variables or predefined data adjust the operational set levels of I and Q for the cavity accelerating voltage; for visualizing a dual scope oscillator, the I set and Q set values can be used.
2. Maintaining the cavity frequency-tuning loop can tune the cavity frequency to a resonant frequency and the cavity-accelerating voltage is controlled by the set values of I and Q.

1.3 Integration Testing

Recent technology in System on Chip (SoC) has enabled to develop high-density FPGA devices that are suited to the needs of high performance real-time signal processing. With the addition of embedded processor cores and powerful IO interfaces they provide a valuable combination of high performance and configurability. At this point in time we process analog and digital boards individually.

Here, down-conversion of the data RF signal from the sensed cavity port is performed using a mixer to the comfortable frequency range and extracting the I, Q, I_n and Q_n information from cavity IF. After comparing the set and sensed value of amplitude an algorithm should be run to generate the new I_{out}, Q_{out}, I_n_{out} and Q_n_{out}. Generated signals are converted into analog format using appropriate DAC and they must be put within I/Q modulator safe range. These signals are fed to the I, Q, I_n and Q_n ports of the I/Q modulator to control phase and amplitude of RF generators signal. Phase and amplitude corrected signal is then fed to amplifying system which in turn corrects the field in side cavity.

The control logic is implemented in the Xilinx FPGA using VHDL coding. The hardware components can be divided into analog parts and digital parts. The analog parts mainly deal with signal mixing, IQ modulation and interlock system while the digital parts contain the control algorithm.

1.3.1 Programming Layout for Digital LLRF Control Loop

With advancement in the field of programmable logical devices and the Hardware description language, digital RF feedback control system using FPGAs is adopted for providing better flexibility, reliability and stability. In phase (I) and quadrature phase, (Q) scheme is used for extracting the amplitude and phase information about RF signal. A block diagram for FPGA-based VHDL programming layout is shown in Fig. 1.2. The development environment for FPGA coding is as follows:

- coding language: VHDL
- synthesis tool: XST in ISE 8.2i from Xilinx
- implementation: ISE 8.2i from Xilinx
- mapping and routing: ISE 8.2i from Xilinx

1.3.2 Working Steps from Programming Point of View

FPGA-based control system in VHDL code will perform the following tasks:

- Spartan-3 DSP protoboard (XC3S-PQ208) by the VHDL code converts input baseband signal (cavity IF signal) into digital format (ADC).
- By adjusting sampling frequency four times of analog input signal, collect I, Q, I_n and Q_n from different output lines with checking phase difference between every neighbour's output channel at 90°, are stored.
- To avoid synchronizing problem, one channel of AFG3102 is used for clock generation for protoboard and another is used for synchronizing the signal generator.
- Stored digital I, Q, I_n and Q_n data in different registers are compared with predefined set values and the operation is performed as desired, i.e. process according to the compared value, if instantaneous value (I, Q, I_n and Q_n) is

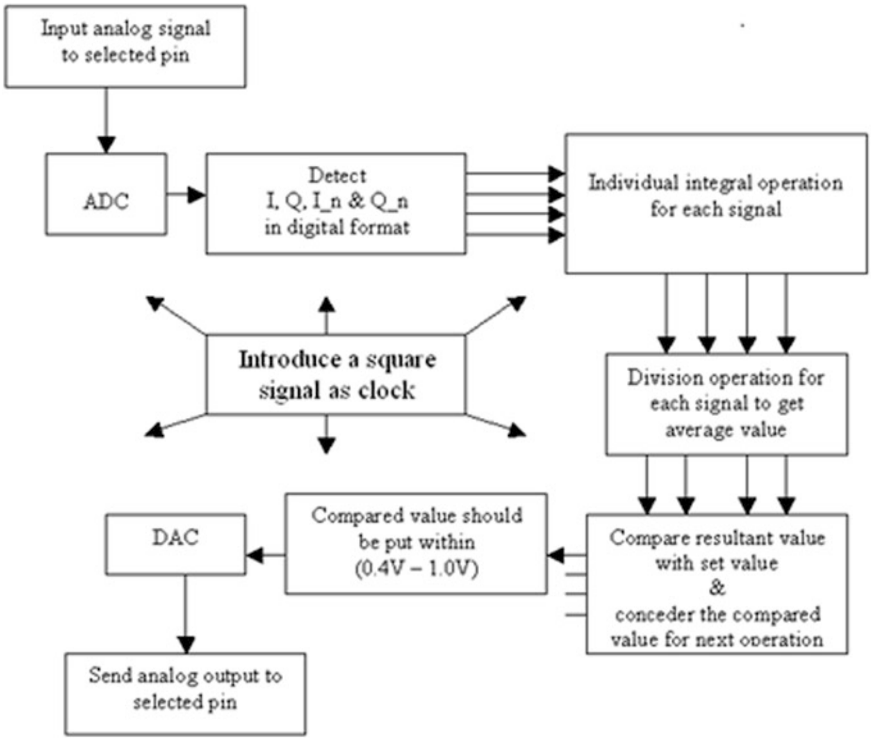

Fig. 1.2 Block diagram for FPGA-based programming layout

(a) = set value then output will be assign position voltage
(b) > set value then output will be in decrement order
(c) > set value then output will be in incremental order

Since the above processed output signals are differential I and Q input to the I/Q modulator (AD8345), their values are limited differentially between 0.4 and 1.0 V with 0.7 V in the middle position [3]. To overcome noise in instantaneous I, Q, I_n and Q_n value, get average result for each, which will compare with set value to get I_{out}, Q_{out}, I_n_{out} and Q_n_{out}.

1.4 Closed Loop Operation with Test Set-up

The main hardware components of the digital RF feedback system are ADC for sampling of the RF signal, FPGA for signal processing and DAC for driving the IQ modulator. An XC3S-PQ208 commercial Spartan-3 DSP protoboard is adopted for the ADC/DAC and FPGA board. The experimental set-up block diagram used is shown in Fig. 1.3.

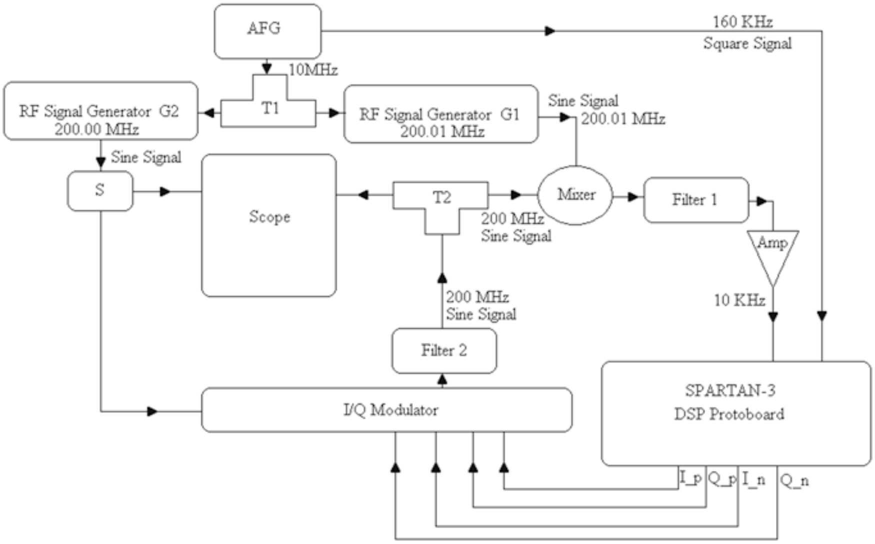

Fig. 1.3 Experimental set-up block diagram (where *T1*, *T2* TEE type BNC connector, *S* 6 dB splitter, *F1* low pass filter (dc—40 MHz): used for filtering sum freq., *F2* harmonic filter (dc—580 MHz), *Amp* Amplifier (for amplifying the IF signal))

The feedback logic based on the PI control is implemented in the FPGA by using VHDL. The I and Q components of the cavity field signal are fed into the FPGA using the ADC, which samples the RF signal four times during one period. The sampled I and Q components of the cavity signals are compared with the set value, which generates the error signal.

1.4.1 Observed Figures

Visualized and stored various waveform patterns [by Scope (TPS2024 (Tektronix) and 54832B DSO (Agilent))] for making the conclusion are shown in Figs. 1.4 and 1.5).

1.4.2 Important Observations

During the testing of complete loop many important observations are listed as:

1. Proposed VHDL program can generate I/Q signal if operating frequency of the protoboard is 16 times that of input signal.
2. After four steps (reset, write, conversion, read) analog to digital conversion occurs, i.e. sampling frequency is four times less than operating frequency.

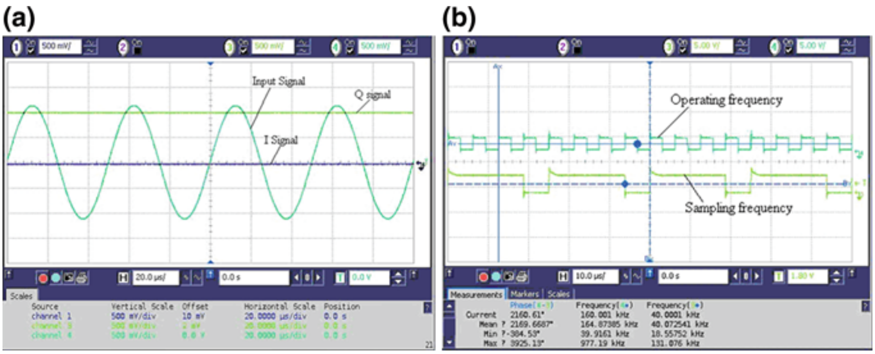

Fig. 1.4 **a** Input signal with I/Q waveform and **b** operating freq. versus sampling freq.

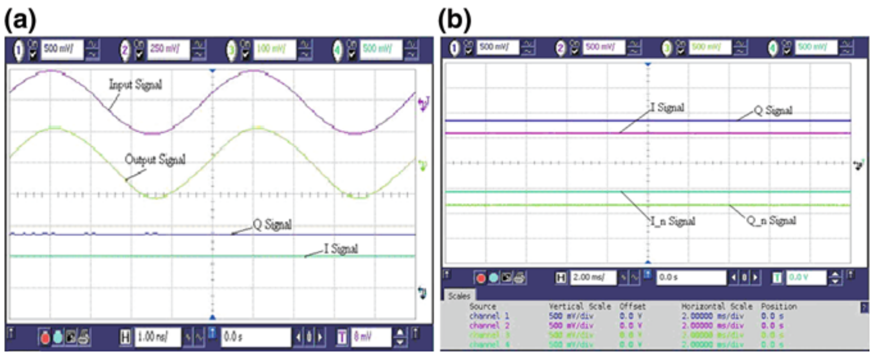

Fig. 1.5 **a** Various signals at a time and **b** I, Q, I_n and Q_n signal (*within limiting value*)

3. We may also follow the ratio between operating frequency and input signal frequency (cavity IF signal) as 16:(1 + 4*n*), where *n* is any counting number.

1.5 Conclusion

FPGA-based LLRF digital feedback loop was realized using Spartan-3 protoboard, I/Q modulator (AD8345), Mixer (SRA1WH), Arbitrary function generator (AFG) where RF cavity signal was simulated using RF signal generator in laboratory. During testing for closed-loop operation, dynamic range of 13 dB for amplitude control and 360° phase control was observed. Overall, it can be concluded that the proper working of digital feedback low level RF control system using Spartan-3 DSP protoboard can be demonstrated.

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