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Arbitrary Modeling of TSVs for 3D Integrated Circuits

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Preface

This book presents a wide-band and technology independent SPICE-compatible *RLC* model for TSVs in 3D ICs. This proposed model accounts for a variety of effects, including skin effect, depletion capacitance, and nearby contact effects. The TSV is modeled like a MOS structure where it is assumed that a full depletion region exists around the TSV. A lumped parameter model is then proposed to model the TSV. The equivalent circuit model includes a single TSV model and coupling model between TSVs. The dimensional analysis method is applied to obtain closed form solutions for the resistance, capacitance, and inductance of the TSV lumped model. The accuracy of the expressions is then verified with the electromagnetic field solver under typical high-density TSV dimensions, and it shows a significant accuracy up to 100 GHz.

Although there are several works in the literature that provide an *RLC* model for a TSV and closed form expressions with different levels of accuracy, this book discusses models that exhibit several additional enhancements as compared to existing literature. The models in this book include: (1) MOS depletion R and C effect. (2) Body contact effect. (3) Model linearization, i.e., single nonlinear or frequency-dependent element can be approximated by multiple linear, and frequency-independent elements. (4) Simulation comparisons (e.g. with full-wave, quasi-static, and device simulation). This book can be very useful in the fast SPICE-compatible parasitic extraction of TSVs for 3D IC design.

Moreover, a proposed architecture based on TSV technology for a spiral inductor is demonstrated and characterized. Also, in this book, and for the first time, a novel inductive coupling interface that uses the magnetic near field induced by TSV-based spiral inductor is demonstrated. The feasibility of using TSV for wireless near field communication is shown. A TSV-based near-field inductive-coupling system offers a high quality factor and a good coupling coefficient. Therefore, the proposed communication system appears to be a promising technology for wireless communication. Moreover, another application for the TSV, which is bandpass filter, is discussed in this book.

This book presents the effects of substrate doping density on the electrical performance of TSV. Moreover, parasitic coupling capacitive between through-silicon vias and surrounding wires is analyzed and studied. Noise coupling between TSVs and CMOS is also investigated.

This book also presents several new directions for TSV fabrication and use in design. It presents performance comparison between Air-Gap Based Coaxial TSV and conventional circular TSV. Air-gap TSVs reduce the energy loss compared to the conventional circular TSV or conventional coaxial TSV. Moreover, SW-CNT bundles as a prospective filler material for TSV are investigated compared to conventional filler materials like Cu, W, and poly-silicon. CNT-filled TSVs have superior performance compared to Cu-filled TSVs, resulting in reduction in transmission loss at high frequency of operation. Moreover, TSV-based ADIABATIC logic based on the adiabatic switching principle is presented and analyzed.

Contents

Chapter 1
Introduction: Work Around Moore's Law

Interconnect dimensions and complementary metal–oxide–semiconductor (CMOS) transistor feature sizes approach their physical limits. Therefore, scaling will no longer be the sole contributor to performance improvement. In addition to trying to improve the performance of traditional CMOS circuits, integration of multiple technologies and different components in a high-performance heterogeneous system is a major trend. This chapter briefly surveys key technology level trends, classified as "More Moore" such as: new architectures (silicon on insulator, SOI; FinFET; Twin-Well) and new materials (High-*K*, metal gate, strained Si), "More than Moore" such as: new interconnect schemes (three-dimensional, 3D; network on chip, NoC; optical; wireless), and "Beyond CMOS" such as: new devices (molecular computer, biological computer, quantum computer).

1.1 Scaling Limitations of Conventional Integration Technology: Work Around Moore's Law

By 2020, the minimum physical gate length of transistors will be close to 7 nm (Fig. 1.1), which is considered by most researchers to be the physical limit of silicon as that limit is the size of the atom and molecule. Clearly, devices cannot be fabricated smaller than the dimension of a single molecule. Also, lithography technology seems unfit for precise manufacturing beyond 7 nm, and if silicon dioxide insulators are reduced to just a few atomic layers, electrons can tunnel directly through the gate. The interconnect congestion bottleneck is also a limiting factor (Fig. 1.2), where interconnect delay dominates with scaling (Table 1.1). These limitations of silicon-based integrated circuits (ICs) are summarized in Table 1.2. These limitations are now causing the industry to identify at least three main research domains (Fig. 1.3), namely: (1) "More Moore," (2) "More than Moore," and (3) "Beyond CMOS" (CMOS, complementary metal–oxide–semiconductor) [1].

The "More Moore" domain traditionally deals with technologies related to further scaling silicon-based CMOS. The "More than Moore" domain encompasses the engineering of complex systems that can combine, by heterogeneous integra-

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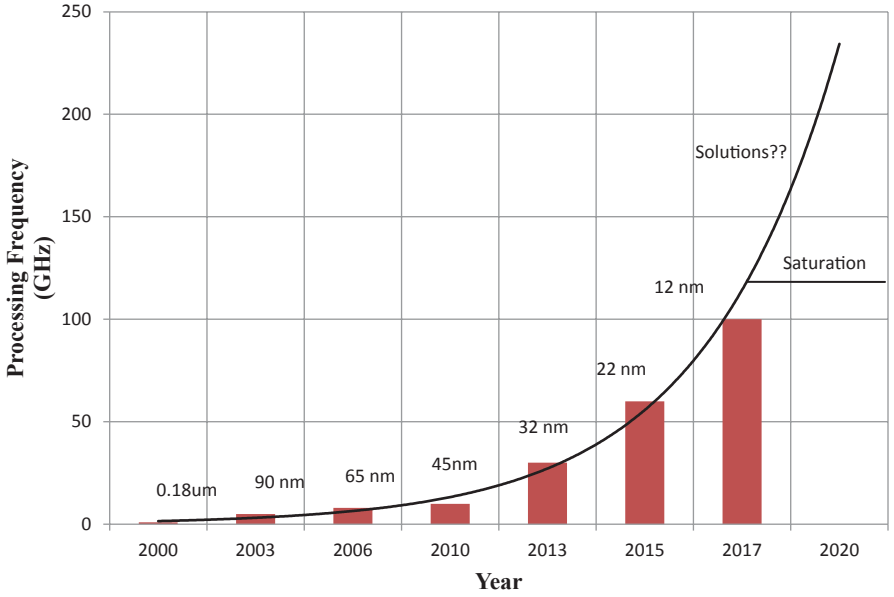

Fig. 1.1 Technology trends show saturation in transistor scaling at 12 nm and the need for working around Moore's law [1]

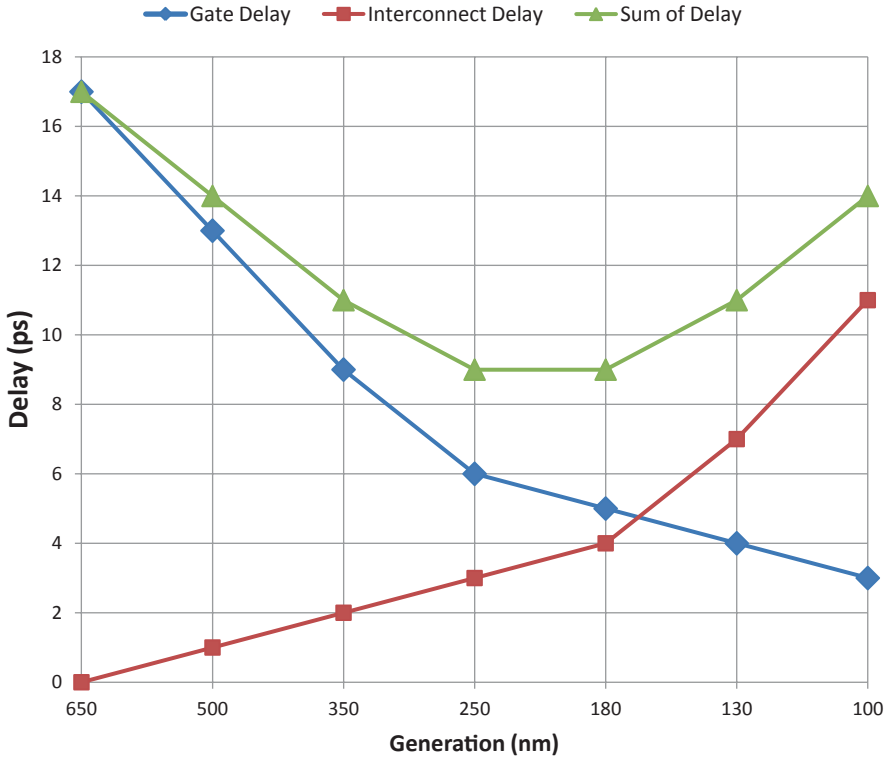

Fig. 1.2 Gate delay, interconnect delay, and sum of delay at different technology nodes, which shows the fast increase in delay time caused by the interconnect [1]

Table 1.1 Interconnects dominate with scaling [1]

	90 nm	45 nm	22 nm	12 nm
Transistor delay (ps)	1.6	0.8	0.4	0.2
Delay of 1 mm interconnect (ps)	5×10^2	2×10^2	1×10^4	6×10^4
Ratio	3×10^2	3×10^3	4×10^4	3×10^5

Table 1.2 Physical limitations of silicon-based ICs

Manufacturing limitations	
Lithography	Lithography technology seems unfit for precise manufacturing beyond 7 nm
Transistor dimensions	Transistor dimensions are approaching a hard limit that cannot be overcome That limit is the size of the atom and molecule. Clearly, devices cannot be fabricated smaller than the dimension of a single molecule [5]
Material limitations	
SiO_2	If silicon dioxide insulators are reduced to just a few atomic layers, electrons can tunnel directly through the gate
Design limitations	
Interconnects bottleneck	Interconnect delay dominates over gate delay

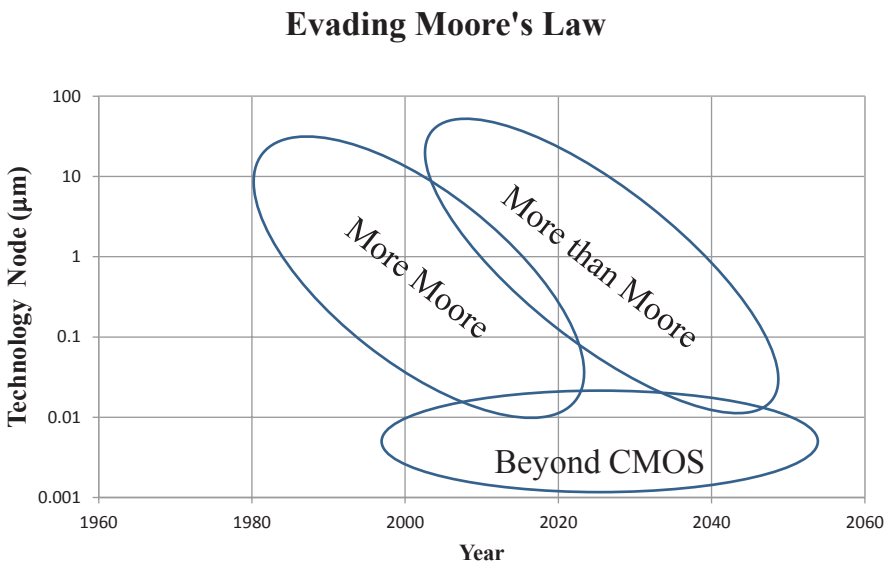

Fig. 1.3 Evading Moore's law: *1* "More Moore," *2* "More than Moore," and *3* "Beyond CMOS" [4]

tion techniques (in SoC or SIP), various technologies (not exclusively electronic) in order to meet certain needs and challenging specifications of advanced applications. The "Beyond CMOS" domain deals with new technologies and device principles (i.e., from charge-based to non-charge-based devices, from semiconductor to molecular technologies).

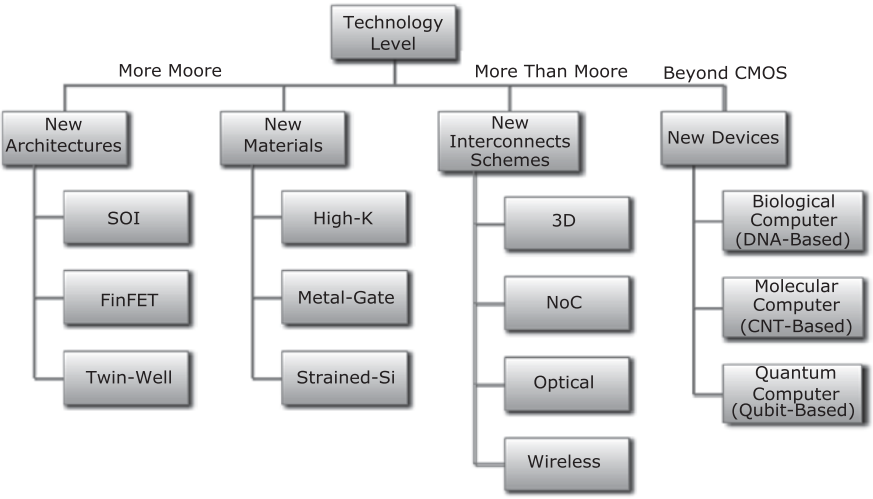

Fig. 1.4 Summary of solutions on the technology level to work around Moore's law, where it presents new architectures, materials, interconnect schemes, and devices

This chapter introduces ongoing trends to work around Moore's law limitations [1–4]. Moreover, it focuses on technology level trends (Fig. 1.4), where it presents new architectures, materials, interconnect schemes, and devices.

1.1.1 More Moore: New Architectures

In this section, examples of the "More Moore: New Architectures" from Fig. 1.4 are given. Silicon on insulator (SOI) is introduced in Sect. 1.1.1.1. FinFET is discussed in Sect. 1.1.1.2. Twin-Well is discussed in Sect. 1.1.1.3.

1.1.1.1 SOI

The basic concept of SOI is fairly simple (Fig. 1.5). Rather than fabricating a transistor whose body is connected to the substrate, which is the normal method, an insulating oxide is deposited on the Si substrate and then the transistor is fabricated on top of that. By doing this, the body is then electrically isolated from its surroundings. This means that the bulk-to-source voltage is now floating which lowers the threshold voltage and capacitance, resulting in a performance increase [5].

1.1.1.2 FinFET

FinFETs have their technology roots in the 1990s, when DARPA funded research into possible successors to the planar transistor. FinFET, which is a double-gate field

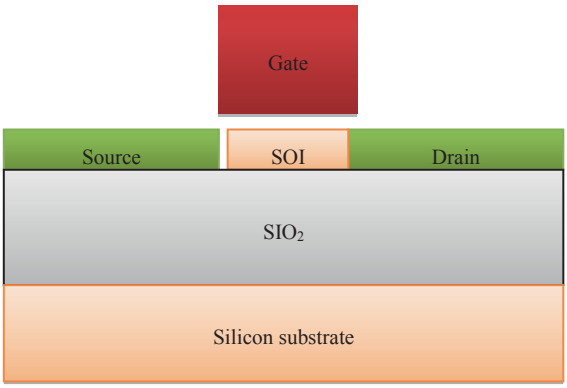

Fig. 1.5 SOI CMOS architecture, where rather than fabricating a transistor whose body is connected to the substrate, which is the normal method, an insulating oxide is deposited on the Si substrate and then the transistor is fabricated on top of that [5]

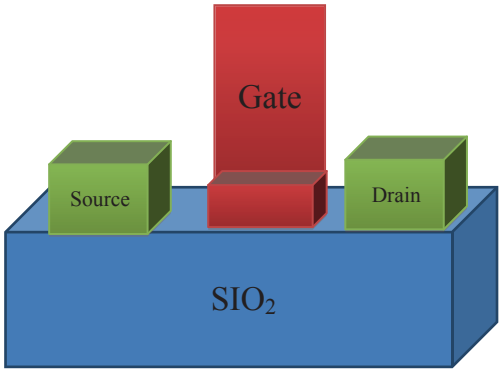

Fig. 1.6 FinFET architecture, where it has two gates that can be controlled independently, usually, the second gate of FinFETs is used to dynamically control the threshold voltage of the first gate in order to improve circuit performance and reduce leakage power [6]

effect transistor (DGFET), is more versatile than traditional single-gate field effect transistors because it has two gates that can be controlled independently (Fig. 1.6). Usually, the second gate of FinFETs is used to dynamically control the threshold voltage of the first gate in order to improve circuit performance and reduce leakage power. Also, a FinFET can be considered a three-dimensional (3D) version of metal–oxide–semiconductor field-effect transistor (MOSFET) that rises above the planar substrate, giving them more volume than a planar gate for the same planar area. Given the excellent control of the conducting channel by the gate, which "wraps" around the channel, very little current is allowed to leak through the body when the device is in the off state. This allows the use of lower threshold voltages, which results in optimal switching speeds and power [6].

1.1.1.3 Twin-Well

For high-performance chips, a low-doped substrate is used, on which two wells are constructed at optimum doping levels. Since the substrate is lightly doped, there

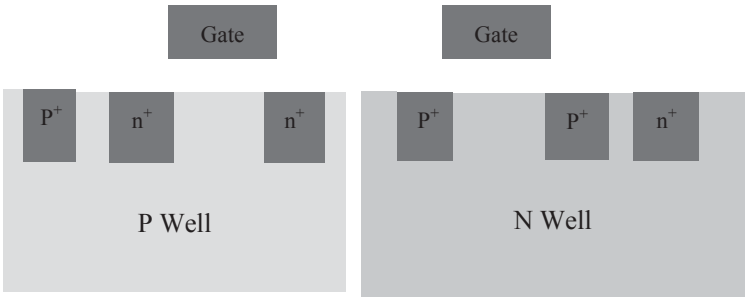

Fig. 1.7 Twin-wells architecture, where the substrate is lightly doped, so there is less chance for latch-up because of the high resistivity [6]

is less chance for latch-up because of the high resistivity (Fig. 1.7) [6]. Moreover, it provides separate optimization of the n-type and p-type transistors and makes it possible to optimize "threshold voltage," "body effect," and the "gain" of n-type and p-type devices, independently. Therefore, balanced performance of n and p devices can be constructed.

1.1.2 More Moore: New Materials

In this section, examples of the "More Moore: New Materials" from Fig. 1.4 are given. High-*K* is introduced in Sect. 1.1.2.1. Meta gate is discussed in Sect. 1.1.2.2. Strained Si is discussed in Sect. 1.1.2.3.

1.1.2.1 High-K Dielectric

The term high-*K* dielectric refers to a material with a high dielectric constant *K* (as compared to silicon dioxide). High-*K* dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of a device. High-*K* dielectrics are designed to address one particular aspect of off-state power consumptions: gate-tunneling currents, as it reduces gate leakage [4].

1.1.2.2 Metal Gate

The doped polycrystalline silicon used for gates has a very thin depletion layer, approximately 1 nm thick, which causes scaling problems for small devices. Others metals are being investigated for replacing the silicon gates, including tungsten and molybdenum to eliminate the polysilicon depletion limitation and also for better thermal stability [4].

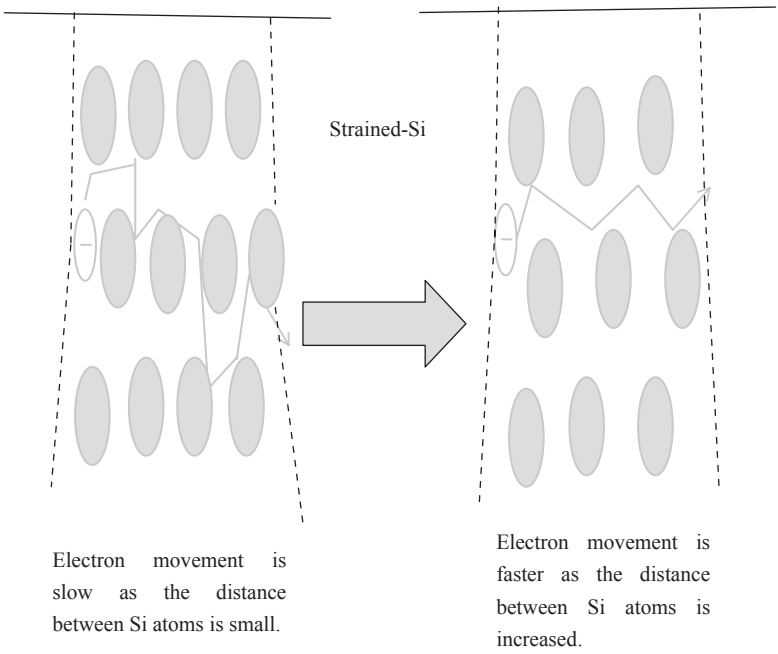

Fig. 1.8 Strained Si is the process of introducing physical strain on the silicon lattice to help improve electron and hole mobility [5]

1.1.2.3 Strained Si

If we cannot make MOSFETs yet smaller, instead move the electrons faster. Strained Si is the process of introducing physical strain on the silicon lattice to help improve electron and hole mobility (Fig. 1.8). This allows the holes and electrons to flow more freely, reducing device resistance and other properties affected by electron/hole mobility [5].

1.1.3 More than Moore (MTM): New Interconnects Schemes

In this section, concepts of "More Moore: New Interconnect Schemes" from Fig. 1.4 are listed. 3D interconnect is introduced in Sect. 1.1.3.1. Network on chip (NoC) is discussed in Sect. 1.1.3.2. Optical interconnect is discussed in Sect. 1.1.3.3. Wireless interconnects are discussed in Sect. 1.1.3.4.

1.1.3.1 3D

Increasing drive for the integration of disparate signals (digital; analog; radiofrequency, RF) and technologies (SOI, SiGe heterojunction bipolar transistors (HBTs),

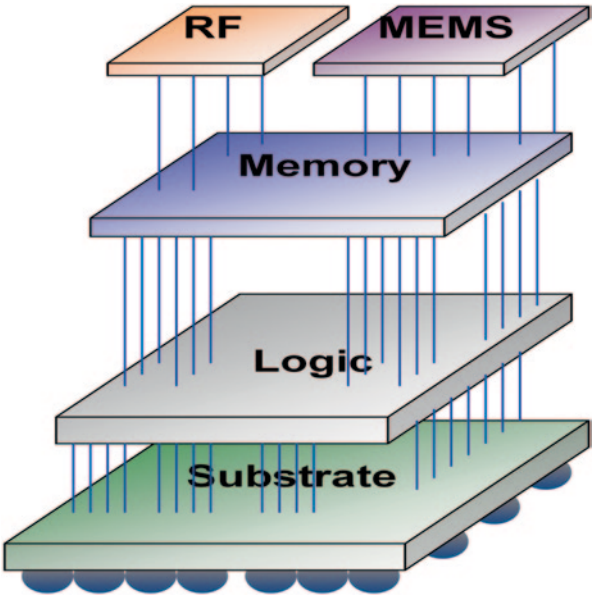

Fig. 1.9 3D technology, where an entire (3D) chip is divided into a number of different blocks, and each one is placed on a separate layer of silicon that are stacked on top of each other [7]

GaAs, strained silicon, and so on) results in introducing various design concepts, for which existing planar technologies may not be suitable; hence, 3D-ICs are introduced (Fig. 1.9).

3D integration technology provides increased performance in many design criteria as compared to the current 2D approaches. 3D-ICs, which contain multiple layers of active devices, extensively utilize the vertical dimension to connect components and are expected to address interconnect delay-related problems in planar (3D) technologies, by the use of short wires in 3D designs. These shorter wires will decrease the average load capacitance and resistance and decrease the number of repeaters which are needed to regenerate signals on long wires; 3D technology also enables the integration of heterogeneous technologies.

In the 3D design, an entire (3D) chip is divided into a number of different blocks, and each one is placed on a separate layer of silicon that are stacked on top of each other. This may be exploited to build a system on chip (SoC) by placing different circuits with different performance requirements in different layers [7].

3D integration provides some unique benefits for processor design, such as packing density, interconnect bandwidth and latency, modularity, and heterogeneity. The packaging density improvement provided by 3D can be used to continue improvements in processing and storage capacity as well as enabling a gradual shift towards integrating the full system in one stack.

3D enables modular design of a variety of systems from a shared set of subcomponents through functional separation of the device layers. As a result, different layers can be independently manufactured in the most cost-effective ways, which can be stacked to compose a wide range of customized systems. Optimizing layer

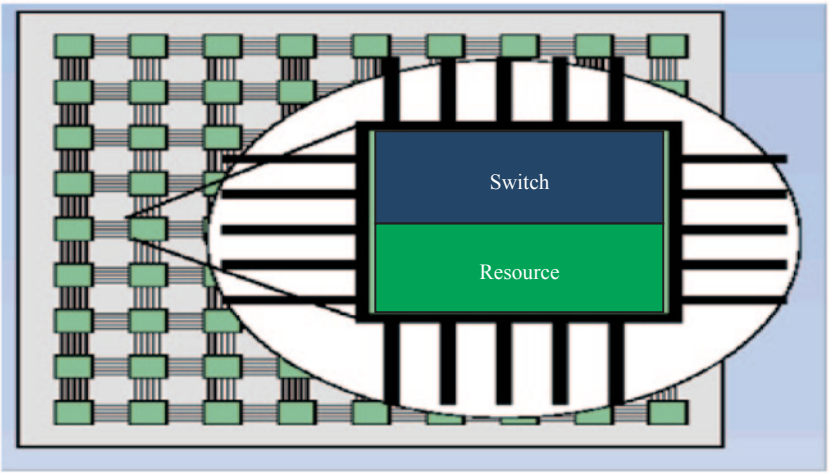

Fig. 1.10 NoC architecture. Instead of having a shared bus, a message passing approach is used [7]

interfaces and infrastructure components, such as power delivery and clocking, can further enhance the inherent modularity advantages.

The system-level benefits of 3D will be determined, to a significant degree, by the effectiveness of novel design methodologies that explore the new design space introduced by the vertical dimension. Design flow optimization is essential in achieving the highest performance gains as well as tackling the more prominent interdependencies among performance, power dissipation, temperatures, interconnectivity, and reliability in 3D.

1.1.3.2 NoC

The NoC is a promising solution to simplify and optimize SoC design. NoCs have been introduced as a shared communication medium that is highly scalable and can offer enough bandwidth to replace many traditional bus-based and point-to-point links [8]. NoC is a communication infrastructure for complex SoC systems with many IPs like a multiprocessor system. Instead of having a shared bus, a message passing approach is used. In analogy to a computer network, each IP acts like a processor, sending and receiving packets (flits) to and from the network. The basic element of a NoC is the switch, which connected to the IP with a network interface (NI), that is in charge of routing flits from the input ports to the output ports, from the source IP to the destination IP (Fig. 1.10). When a flit reaches its destination, it will have crossed several switches, i.e., hops. This kind of communication infrastructure is scalable, making it possible to have a number of parallel communications between different cores.

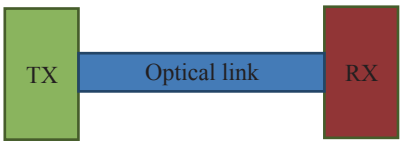

Fig. 1.11 Optical interconnects as a promising solution to reduce the overall power budget [6]

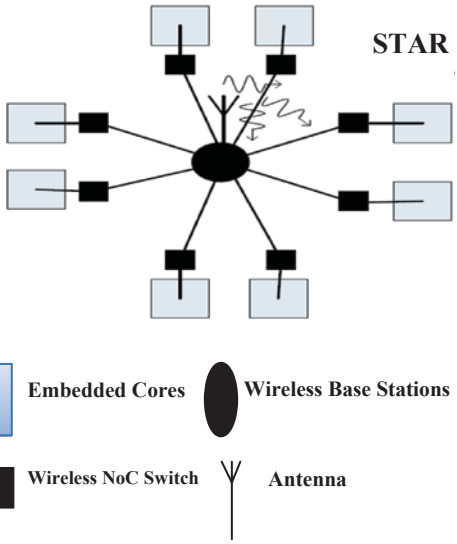

Fig. 1.12 Wireless NoC interconnects, where it can be built using existing CMOS technology [10]

1.1.3.3 Optical Interconnects

Thanks to the unique properties of optical communication, such as bit-rate transparency and low-loss optical waveguides, photonic NoCs have been introduced as a promising solution to reduce the overall power budget (Fig. 1.11) [6].

1.1.3.4 Wireless Interconnects

Unlike 3D and photonic NoCs, NoC with RF interconnects can be built using existing CMOS technology (Fig. 1.12) [10]. Antennas are just on-chip interconnect with transceivers also on-chip enabling full core-to-core communication as well as wireless clocking. Table 1.3 summarizes the main differences between different interconnect technologies.

1.1.4 Beyond CMOS: New Devices

In this section, examples of "Beyond CMOS: New Device Schemes" are discussed. CNT is introduced in Sect. 1.1.4.1. Biological computers are discussed in Sect. 1.1.4.2. Quantum computers are discussed in Sect. 1.1.4.3.