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Abhishek Verma *Editors*

Physics of Semiconductor Devices

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Editors

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Preface

Science and technology of twenty-first century is relying heavily on the development of new materials and their structures. In which the technology of semiconductors is the foundation of modern electronics, including transistors, solar cells, light-emitting diodes (LEDs), quantum dots, and digital and analog integrated circuits. The various fields of semiconductor have continued to prosper and to break new ground. This development has been so fast and may even impact our environment, like by decreasing the amount of fossil fuel used to produce electricity. Therefore, any sort of updated research, latest findings in the area related to semiconductor must be important to all scientific community. The history of the understanding of semiconductors begin with experiments on electrical properties of materials. The properties of negative temperature coefficient of resistance, rectification, and light sensitivity were observed in the early nineteenth century. Since then, a wide variety of techniques were used and discovered to analyze the properties of semiconductors, more than 300 billion dollar sector of the world's economy that designs and manufactures semiconductor devices and many Nobel Prizes have been given in the field of semiconductors. Still, all over the world very intensive work is going on different technologies based on thrust areas of this workshop, and it is essential to keep abreast with the latest developments in advanced fabrication techniques, characterization tools, and also in understanding the physics to enable and produce reliable large volume production of state-of-the-art devices.

About the futuristic optoelectronics, it can be quoted the T. Hiruma's vision that "detecting a single photon cannot be the end point. It is just a starting point. Human kind doesn't know enough even in photonics. We have to find our own direction. God of absolute truth. In-fact we are able to detect a single photon now using a low noise detectors. We have been measuring light from the human body. The body emits about 100 photons per second. His question at the moment is how to measure wavelength and polarity of this light. The purpose is to explore way to apply these photon technologies to study biology and brain."

Now, it's an era of nanotechnology, which can be regarded as the major technological challenge of this century that is stirring people's imagination about its potential use. A new era has already begun, which is changing people's way of life, thinking, and behavior in a very deep manner. Nano scientists can even manipulate objects and forces at the nano scale. At this size, matter behaves differently, light and electricity resolve into individual photons and electrons, particles pop in and out of existence, and other once theoretical oddities of quantum mechanics are seen to be real. Therefore, to give a full exposure and new platform to young scientists and researchers, along with face-to-face discussion with top scientists of particular area, this type of International workshop will highly be beneficial.

The book *Physics of Semiconductor Devices* comprises of scientific contributions from different veins of semiconductor materials, devices, and the related technologies. The contribution has been made by different researchers and eminent scientist from all over the world who presented their paper in the seventeenth International Workshop on the Physics of Semiconductor Devices, 2013 organized by Amity University, Noida. The purpose and objective of this meeting is to spread the vast knowledge of semiconductor physics in every possible field for academia and industry. Through this, every latest finding, research and discovery can go ahead to our scientific world. The chapters include various latest and significant topics, i.e., Optoelectronics, VLSI and ULSI Technology, Photovoltaics, MEMS and Sensors, Device Modeling and Simulation, High Frequency/Power Devices, Nanotechnology and Emerging Areas, Display and Lighting, and Organic Electronics.

The editors wish to place on record our appreciation to Dr. Ashok K. Chauhan, Founder President, Amity University, Noida for his encouragement. Our sincere gratitude goes to Dr. Prashant Shukla, Dr. Abhishek Kardam, Dr. S. S. Narayanan, Dr. Devinder Madhwal, and all the members of seventeenth International Workshop on the Physics of Semiconductor Devices, 2013 for their help in organizing this workshop.

V. K. Jain
Abhishek Verma

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Part I

VLSI and ULSI Technology

Impact of Fin Sidewall Taper Angle on Sub-14nm FinFET Device Performance

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***Abstract*—Recent advances in FinFET technology include fins with tapered sidewalls in addition to conventional vertical sidewall fins. Our 3-D TCAD simulation results suggest that for low to moderately doped fins, vertical sidewall fins have superior electrical performance. Only at extremely high fin doping concentrations could tapered sidewall fins be electrically beneficial.**

***Index Terms*— FinFET, sidewall tapering and TCAD.**

I. INTRODUCTION

Because of the excellent control of short-channel effects, FinFETs have become the main-stream CMOS device in both SOI and bulk flavors [1-3]. SOI FinFETs have improved isolation and simplified processing, but require a more complex starting wafer. Bulk silicon FinFETs use the same starting substrate as planar bulk CMOS but require robust isolation schemes [4] and have more challenging aspect ratio and fill requirements than SOI. Electrical performance of a FinFET is largely dependent on the geometry of the fin. While narrow fins help counter short channel effects, tall fins help reduce device foot print to achieve high drive current density. As the fins are formed using a resist or spacer based dry etch, FinFET process could be made more manufacturing friendly by targeting fins with tapered instead of vertical sidewalls [5].

In this work we have analyzed the electrical impact of fin sidewall taper angle using TCAD simulations of a bulk-Si FinFET. The question we address is: aside from manufacturability, is there any benefit to a tapered fin?

II. SIMULATION DETAILS

A FinFET 3-D TCAD simulation structure created using Sentaurus structure editor is shown in Fig. 1 [6]. The device shown in Fig. 1 has gate length (L), fin width (D) and fin height (H) as 25nm, 10nm and 25nm respectively. The cross-section through the fin of this device is shown in Fig. 2. It can be imagined from Fig. 2 that in the case of fins with tapered sidewalls, less topography will be encountered during all the subsequent process steps, such as dielectric backfill, spacer etch, and gate fill. Comparing Fig. 2(A) and 2(B) it can be seen that while the fin with vertical sidewalls (taper angle TA=0) has the same width D all through the height H, width of the tapered fin (TA=15) is D only at the middle of the fin height. The simulated tapered fin is narrow on the top and wide at the bottom. Typical process steps followed to create a FinFET structure, such as in Fig. 1 are listed in Table 1. DC electrical simulations were performed using IBM device simulator FIELDAY [7]. For this work we utilized a linear drain bias of 50mV, supply voltage (Vdd) of 0.8V and gate overdrive (Vod), where applicable, of 0.7V.

The current generation of FinFETs relies on metal gate work function for threshold voltage (Vt) adjustment. A technology is comprised of various device flavors required for different applications such as low Vt, regular Vt, high Vt-FETs etc. As it is cumbersome to employ multiple work function gate materials; hence despite known disadvantages [4], fin doping is used for Vt adjustment with a single work function gate. In this work we have explored various fin doping concentrations (Nch) to cover the range of applications.

III. RESULTS & DISCUSSIONS

The subthreshold swing (SS) is shown as a function of the fin sidewall taper angle in Fig. 3. It can be seen from Fig. 3 that the SS at zero taper angle decreases with increasing Nch. We attribute this to the increase in effective channel length (Leff) with increasing Nch. For tapered fins (see Fig. 2(B)), Nch controls Vt more effectively in the wider bottom portion of the fin as compared to the narrow top region. Consequently, as Nch increases, Vt of the fin bottom is higher than the top of the fin. In the extreme case, this makes the top portion of the fin determine short channel effects (SCE) of the device. Since the top portion of the fin is narrow where short channel control is better, SS shows slight improvement. Similar trend is observed in Fig. 4, where another short channel parameter DIBL is plotted as a function of the fin taper angle. The net result of SCE can be seen in Fig. 5, where representative subthreshold leakage (Ioff) is plotted as a function of the fin taper angle. Weak SS and DIBL changes seen from previous Fig. 3 and 4, do not seem to impact Ioff enough to explicitly show up on the semi-log plot in Fig. 5. However, there is a small decrease in Ioff of the highly doped fins as taper angle increases.

The impact of fin doping and sidewall taper angle on carrier transport through the channel can be seen from Fig. 6, where linear drain current is plotted as a function of the taper angle. It can be seen from Fig. 6 that Iodlin decreases as both fin doping and taper angle increase. Since Iodlin is simulated at a fixed overdrive, this Iodlin decrease can not be explained by change in Vt. Representative series resistance is plotted in Fig. 7 as a function of taper angle. It can be seen from Fig. 7 that Rodlin increases with increase in taper angle and fin doping. As blanket type fin implant, much like well implant in planar bulk CMOS, is used for doping the fin, background doping in S/D regions also increases along with fin doping. This leads to decrease in S/D doping with increase in fin doping, consequently increasing Rodlin. However, increase in Rodlin with increase in taper angle for highly doped fin is due to narrow low-Vt top portion of the fin being more effective than the wider high-Vt bottom part of the fin. Thus for highly doped and tapered fins, current predominantly flows in the top narrow portion of the fin, encountering higher sheet resistance due to narrow S/D extension regions which explains increase in Rodlin with taper angle. Effective drain current Ieff is plotted as a function of taper angle in Fig. 8. It can be seen from Fig. 8 that Ieff follows the Iodlin and Rodlin trends shown in Fig. 6 and 7. Representative intrinsic transistor performance is shown in Fig. 9, where representative Ioff is plotted as a function of Ieff. It can be seen from Fig. 9 that at a constant Ioff=100nA/um, fin without tapered sidewalls has the highest Ieff. With increase in fin doping, the disadvantage in Ieff of tapered fins is mitigated. However, within usable range of fin doping concentrations up to 8e18 cm^{-3}, fin sidewall tapering is still undesirable.

CONCLUSIONS

The impact of fin sidewall tapering on electrical performance of a bulk Si FinFET is reviewed. It is observed that the device with low-doped, vertical fin sidewalls achieves the best Ieff performance, while fin sidewall tapering could be beneficial in SCE, but only at extremely high fin doping concentrations.

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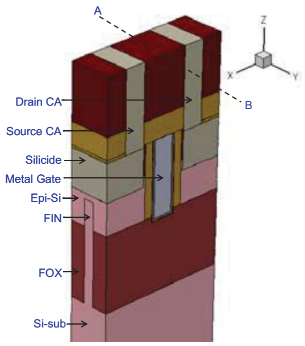

FIG 1: FinFET 3-D simulation structure. A cross-section along the line A-B is shown in FIG 2.

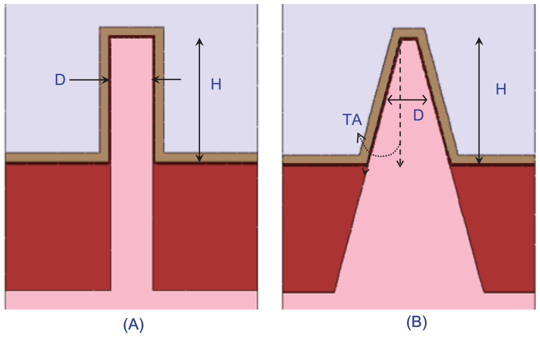

FIG 2: Simulated Fin cross-sections. D, H and TA are fin-width, height and sidewall taper-angle respectively: (A) 0 degree (B) 15 degree.

Serial No.	Process module	Purpose
1	FIN	Litho and patterning of fins
2	Gate	Litho and patterning of dummy gates
3	Spacer 1	Spacer to protect fin channel during Si-epitaxy
4	Si/SiGe Epi	Epitaxial growth of Si/SiGe on fin S/D regions
5	Spacer 2	Spacer to protect S/D extensions
6	Deep S/D implants and activation	Deep S/D implants and activation anneals
7	RMG	Replacement metal gate process
8	MOL: TS, CA	Mid of the line flow, trench Silicide process and deposition of Tungsten to form contacts to S/D and gates
9	BEOL: V0, M1, V1, M2,...	Back end of the line flow to form various levels of metallization

TABLE 1: Process modules in a generic FinFET flow.

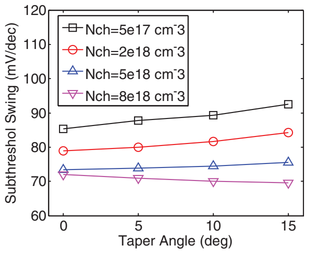

FIG 3: Subthreshold-swing at Vds=Vdd vs. fin sidewall taper angle.

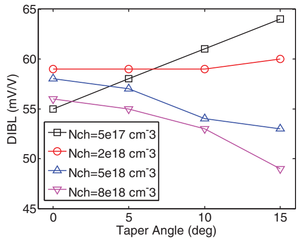

FIG 4: DIBL vs. fin sidewall taper angle.

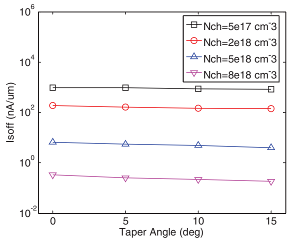

FIG 5: Representative Ioff at Vgs=0 and Vds=Vdd vs. fin sidewall taper angle.

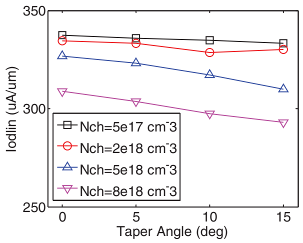

FIG 6: Iodlin at Vgs=Vod and Vds=50mV vs. fin sidewall taper angle.

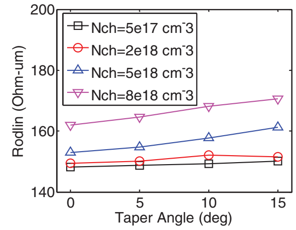

FIG 7: Rodlin at Vgs=Vod and Vds=50mV vs. fin sidewall taper angle.

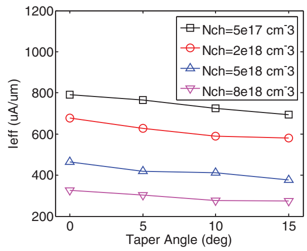

FIG 8: Ieff vs. fin sidewall taper angle.

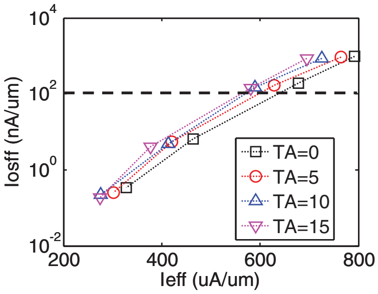

FIG 9: Representative Ioff as a function of Ieff, Nch increases from right to left for each taper angle (TA).

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Capacitance-Voltage measurement of SiO_2/GeO_xN_y gate stack on surface passivated germanium

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***Abstract*-Germanium (Ge) based MOS transistors is possible alternative to silicon based MOS transistors due to high mobility of carriers in Ge. Extensive research is going on for fabrication of high mobility MOS devices worldwide. Here, we have studied the c-v characteristics of Ge based surface passivated MOS structure such as dielectric constant of gate stack, effective oxide charges, density of interface charges at semiconductor oxide interface etc. The interface trap density extracted from the C-V/G-V measurement showed the lowest interface trap density of $7.82\times10^{11}cm^2eV^{-1}$. The minimum leakage current density for SiO_2/Ge_xON_y gate dielectric stack is $1.35\times10^{-7}Acm^{-2}$ at gate bias of 1V.**

***Index Terms* — Germanium, Passivation, Sputtering, SiO_2, D_{it}.**

I. INTRODUCTION

Germanium has attracted great interest as a candidate channel material for nanoscale complementary metal oxide semiconductor (CMOS) devices. It has the highest hole mobility amongst all identified semiconductor materials, being the principal candidate to substitute Si in future PMOS devices [1-2]. However, there are many difficulties in realizing germanium CMOS technology associated with the different physical and chemical properties of Ge compared to Si [3-4]. Unlike SiO_2 thermally grown on Si, GeO_2 is thermally unstable in processing temperatures usually employed in device fabrication [5]. It is well known fact that GeO_2 is water soluble, hygroscopic and exhibits poor thermal stability therefore controlling germanium interfaces is essential for future generation devices. In sight of these characteristics, an apparently trivial solution is the replacement of the Ge native oxide by another dielectric material with intrinsically better physical properties. [6-9]. The fabrication of high speed MOS devices based on Ge requires a high quality gate oxide as an insulating layer and many recent studies on this topic are being reported [10-16]. However, deposition of SiO_2 layer onto germanium is rather rarely reported in the literature. In this work, we focused on formation of ultrathin GeO_xN_y layer and investigated the effects of this interface layer on dielectric/Ge interface passivation and SiO_2 as dielectric.

In this paper, we report the formation of GeO_xN_y interfacial layer for the high-k gate stacks. Thermally grown GeO_xN_y layer has been formed at 550°C for passivation of Ge surface. Silicon dioxide has been deposited as a gate dielectric through RF sputtering. The RF sputtering have been used to attain good quality of thin films as reported previously [16]. The post-deposition annealing of the samples is performed inside the RTP system in nitrogen ambient. The process of annealing refines grains, induces softness and removes strains and stresses from the film. XRD and ellipsometer were used to characterize the GeO_xN_y layer. MOS capacitors have been fabricated using GeO_xN_y with a sputtered silicon dioxide (SiO_2) on top of it followed by growing Pt metal layer as gate contact. The second section of this paper explains the experimental part. The results are discussed in third section and fourth section concludes the paper.

II. EXPERIMENTAL DETAILS

The 2" p-type Ge (100) substrates were used for the fabrication of $Pt/SiO_2/GeO_xN_y/Ge$ MOS structures. The substrates were rinsed in 2% HF and de-ionized water alternately for several times, followed by blowing dry with N_2. Following that, annealing in a NH_3 ambient was performed inside a RTP chamber at a constant temperature of 550 °C for four minutes. Substrates were then transferred to the sputtering chamber for the deposition of SiO_2 thin films. Post deposition annealing (PDA) was performed in N_2 ambient at 500 °C for 60 s at atmospheric pressure using rapid thermal annealing. Thickness of the $GeON/SiO_2$ bilayer dielectric stack was measured to be in the range of 27.69-28.57 nm. The thickness of interfacial GeON layer was approximately 5.52-5.79 nm. The refractive index value for dielectric stack was found to be in the range of 1.46-1.49. To study the electrical properites Platinum metal was deposited as top electrode on SiO_2 thin films through shadow mask with electrode area of $12.56\times10^{-4}cm^2$ by using metal sputtering system (Nordiko) at base pressure of 2.3×10^{-5} mbar where substrate was kept at room temperature. An ohmic contact was formed on backside of Ge substrate to form MOS structures by thermally evaporating the Al metal. These fabricated $Pt/SiO_2/GeO_xN_y/Ge$ MOS structures were post metallization annealed (PMA) at 450 °C for 20 min using forming gas ($90\%N_2$, $10\%H_2$) ambient. The structural characterization of annealed SiO_2 films was carried out by using the ellipsometer (Philips SD 1000), XRD (BRUKER Model D8 ADVANCE) and AFM. The electrical properties were studied by capacitance-voltage (C-V) and Current voltage, I-V (semiconductor characterization system 4200) measurements of fabricated MOS structures.

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