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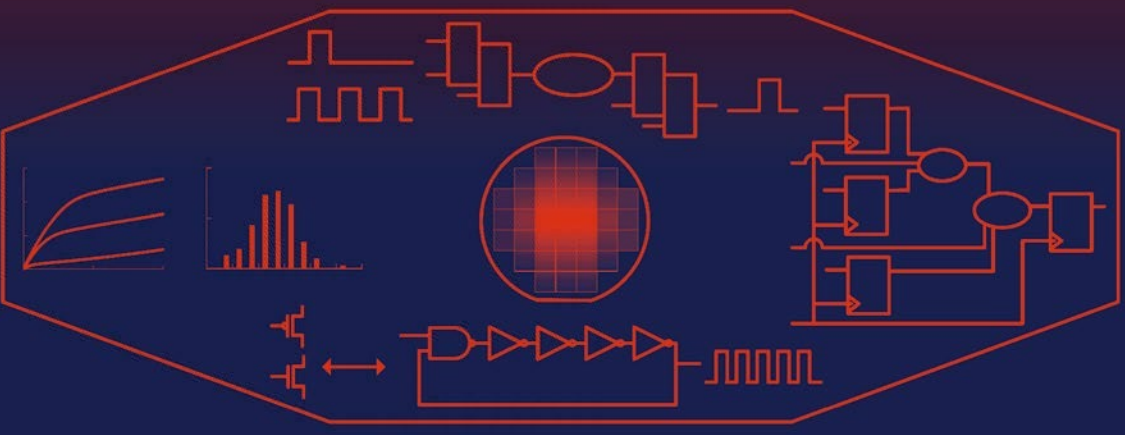
CMOS Test and Evaluation

A Physical Perspective



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Preface

Designing, fabricating, and testing of CMOS chips is a multi-billion dollar industry, spanning a multiplicity of engineering fields. Many of the complex tasks at each stage of design and production are handled with automated tools enabling rapid deployment of semiconductor chips in the marketplace at a low cost. Significant engineering resources are devoted to the development of these tools and in generation of associated software. Often engineers engaged in designing and testing of chips rely on automated tools and have limited exposure to the physical behavior of devices and circuits. Generally well proven and efficient, this approach lacks full utilization of university classroom learning in physics and engineering. Although detailed knowledge of a CMOS product may be daunting, a high-level view of various engineering aspects is extremely desirable when it comes to rapid diagnostics, problem resolution, and optimization of the entire production process.

Working with CMOS design, silicon technology development, and manufacturing teams in IBM's 180 to 32 nm CMOS technology nodes, we began deploying special test structures for DC and high-speed characterization of CMOS circuits. Initially our focus was on developing a methodology for bridging observed circuit behavior at high speeds to constituent component properties. Hardware data collected from the fab were compared to the simulated predictions using design automation tools. If the model-to-hardware mismatch was outside the specified range, silicon processes had to be modified to adjust the hardware to match the model. The alternative approach of updating the compact models to match the latest silicon technology was often not viable, considering the high cost of chip redesign and pressure to meet time-to-market demands. In either approach, it was imperative that the feedback from the test structures be accurate and reliable. Special techniques for design, test, and analysis were developed to quickly assimilate the information and to present it in a clear and concise manner so that experts as well as non-experts could follow the presentations and reports. These test structures have been placed in scribe-lines of CMOS chips and on dedicated test vehicles built at IBM and by IBM's partners in CMOS technology development. This integrated approach to design and test of electrical test structures is covered in our book entitled *Microelectronic Test Structures for CMOS Technology* published by Springer in August, 2011.

Some of these test structures, when embedded in CMOS product chips, proved to be very useful in product performance evaluation and debug. These monitors, primarily ring oscillators, are easier to analyze and model than the complex circuitry comprising the chip design itself. By proper configuration of embedded monitors, chip power and performance can be bridged back to device properties and to the EDA models and tools used for designing the chip circuitry. Changes in circuit characteristics can be monitored throughout the life of the product. Additional applications of such embedded test structures are in the areas of sorting and binning of chips and applying test limits with guardbands to meet warranted performance.

It has been our experience that understanding a complex system can be simplified by either observing the aggregate behavior of its components or by comparing the behavior of its key constituents to the system as a whole. Appropriately designed test structures and monitors can play a very important role in predicting the properties of the system. The knowledge derived is physically intuitive making it easier to detect model, design tool, and other software-related errors. A priori knowledge of physical behavior when applied to statistical data mining can considerably reduce the effort in resolving design and test issues. Cross-checking of data collected from embedded monitors, product chips, and system tests for consistency makes the findings conclusive with a high degree of confidence.

In *CMOS Test and Evaluation*: *A Physical Perspective*, we have attempted to describe the relationship between basic circuit components (resistors, capacitors and diodes, and MOSFETs) and a complex CMOS chip with as many as several billion transistors. Our approach is to provide an overview with examples to link various aspects of CMOS technology, design, and test. Simulated data representative of that acquired during electrical testing in product manufacturing and qualification are used to illustrate concepts and to demonstrate data visualization and presentation. Exercises are included at the end of each chapter. Many of the circuits described and incorporated in the examples and exercises enable observation through simulation of features that are not experimentally assessable, often providing clearer insight into aggregate behavior.

We hope that this book will prove useful in preparing physics and electrical engineering students for building a career in the semiconductor industry as it faces new challenges, as well as serving as a useful reference for practitioners in the field.

We are thankful to our former colleagues in IBM's Server and Technology Group and in IBM's Research Division for close collaborations throughout our tenure in IBM.

How to Use This Book

There are at least two effective ways that this book can be used. The first is by practitioners already confronting real problems on the test floor. As emphasized in the 2013 ITRS Roadmap, the CMOS test arena is in a state of rapid change. While this book cannot possibly address all the known changes or foresee many more to

come, the underlying physics of it all has not and will not change. In each chapter we attempt to present a high-level summary of the subject matter followed by a number of exercises, many of which relate to actual problems encountered in the field. While none of these may be identical to the crisis of the moment, the approach to resolution that we advance in the formulation and solution of exercises is based on physical insight, is very general in nature, and will apply to a wide range of new problems as they arise.

The second way this book can be used is in the education and training of science and engineering students preparing to work in the semiconductor test enterprise. It is in no way an attempt to replace or compete with any of the fine existing texts that focus in great depth on particular areas of design, fabrication, and test. It is assumed that students will have already mastered the contents of a number of these. It is our intent to build on them to provide an integrated technical view of CMOS test as a whole and to provide students with a set of exercises to help them develop physical insight. As mentioned above, the field of semiconductor test is changing rapidly and will continue to do so. Those who desire to enter and prosper in this field must be prepared to evolve with it. It is our goal to help them prepare for this journey through examples and exercises based on real problems encountered in CMOS manufacturing test, with an emphasis on gaining underlying physical insight, along with high-level topical summaries.

The scope of this book and a brief description of chapter contents are covered in Sect. 1.8. The introductory material in the beginning of the chapters can be covered quickly with much of the time and effort devoted to circuit simulations and data analysis. The aim is to help develop an intuitive physical understanding of the material covered without becoming bogged down in the details.

It is essential to have access to compact device models for different technology nodes or from different foundries, together with a SPICE simulation environment. By working through the examples and exercises, students can learn to cross-check the results and quickly spot and correct errors. Presenting conclusions and the line of reasoning in a clear and unambiguous manner is extremely important. Examples of this are presented in the text as well as in solutions to exercises published on the web.

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Introduction 1

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In traditional testing of digital complementary metal-oxide-semiconductor (CMOS) chips, emphasis is placed on functional verification and fault modeling. Push to higher frequencies has led to optimization of circuit properties and chip operating conditions for power/performance and yield. As silicon technology approaches scaling limits, there is a trend towards reducing circuit design margins and product guard-bands to squeeze maximum benefits from higher circuit densities. Such factors have been continually increasing the burden on manufacturing test. Some of these additional test challenges are addressed by examining the underlying physical behaviors and linking silicon technology, circuit design and electrical tests through models and simulations. In this chapter an overview of CMOS test, in conjunction with circuit design methodology and silicon technology performance, is provided as an introduction to the material covered in this book.

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1.1 Simplicity in Complexity

There are many examples in nature where the collective behavior of a large number of units, each interacting with the others while maintaining its unique identity and characteristics at all times, can be expressed in a fairly simple way. This allows us to conduct our lives without having a detailed knowledge of how the world operates. If the collective behavior is cyclic, repeated observations make it ever easier to assimilate and reinforce the information and store in memory for ready retrieval.

One example is Boyle's law for ideal gases stating that in a closed system held at a constant temperature, the pressure exerted by gas molecules on the walls of the vessel is inversely proportional to its volume, or pressure $\times$ volume = constant. The law succinctly describes an observation resulting from the motion of a very large number of molecules and their interactions with the vessel. The molecules themselves may have varying chemical and physical properties and their velocities and relative positions are a function of time, but the aggregate behavior is stated in a simple mathematical expression.

A very large scale integrated (VLSI) digital CMOS chip or die is a complex entity comprising hundreds of thousands to billions of circuit elements. These elements are either physically embedded in or layered on top of a crystalline silicon surface. Instructions received by the chip in the form of voltage signals as strings or "1"s and "0"s are processed within the chip and the results communicated to the external world, also in the form of voltage signals. The connectivity of circuit blocks performing the required functions can be altered with voltage signals generated within the chip. The application conditions such as power supply voltages, temperature and frequency of operation may cover a wide range for a single chip design, and for chips of different designs fabricated at the same silicon technology node.

Rules of simplification can be applied to complex CMOS chips as well. Some of the basic building blocks such as logic gates, memory cells, and other storage elements are replicated millions of times within chip. As illustrated in Fig. 1.1a, periodic "clock" signals control arrival timing of signals at the input of the combinational logic block, and set the capture timing windows for the signal in the following clocked storage element. The minimum clock cycle time of a complex digital CMOS microprocessor chip can be estimated as a multiple of the measured or simulated signal propagation delay through an inverter with fanout of four (FO = 4) shown in Fig. 1.1b, representing the signal propagation delay through a data path like that in Fig. 1.1a.

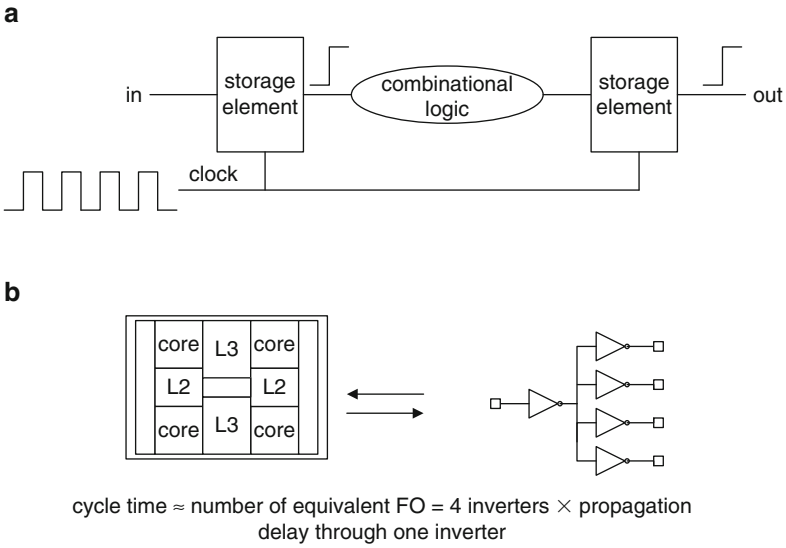

Fig. 1.1 (**a**) Data path with clock signals to control timing, and (**b**) complex microprocessor chip cycle time estimation from logic gate delay

In another example, the aggregate power characteristics of a large number of components, switching at very high frequencies and performing multiple tasks, are expressed with the simple relationship

$$P = V_{\mathrm{DD}} \times I_{\mathrm{avg}}, \tag{1.1}$$

where V_{DD} is the power supply voltage and I_{avg} is the average DC current drawn. In a fashion similar to the first example, an insight into the AC and DC components of power and their dependencies on the properties of circuit components may be developed from modeling a single logic gate.

Knowing and understanding the behaviors of smaller circuit elements proves to be very valuable when moving up the circuit design and test hierarchy. A detailed knowledge of devices, silicon processes, circuit design, logic functions, chip architecture, design for testability features, test and characterization procedures, and staying updated with advances made in all these areas, is daunting even for the most ambitious. However, the learning derived from working with a few smaller representative elements across all the levels mentioned above is extremely useful in developing a methodology for addressing large scale multi-faceted VLSI programs.

1.2 CMOS Design and Test Overview

The major steps in design, fabrication, and test of a digital CMOS chip are illustrated in Fig. 1.2. Starting from the top left corner in the figure, the chip architecture is defined to meet projected product specifications based on market or customer demand. In a digital system, this behavioral description of the design is expressed in a hardware description language (HDL) through abstraction at a register transfer level (RTL). The design is then simulated to verify the logic and converted to a logic gate-level circuit description.

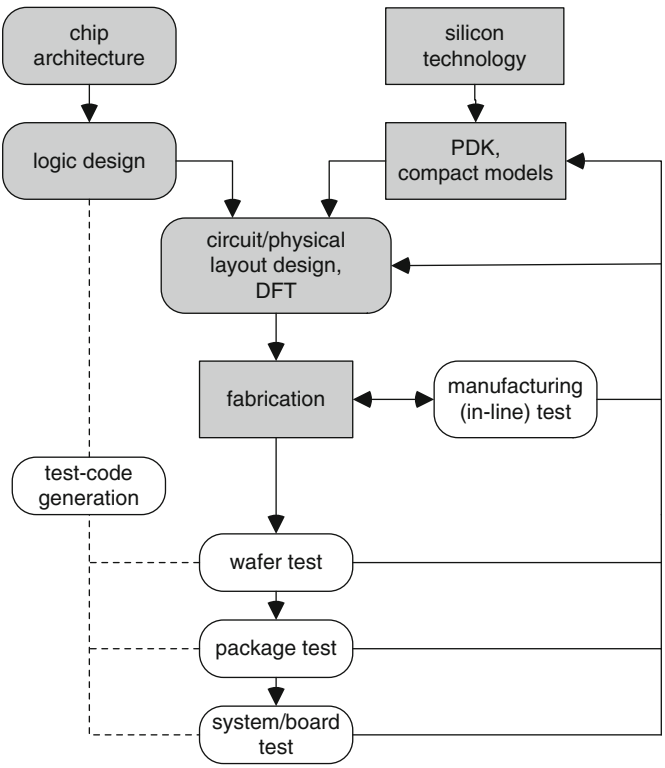

Fig. 1.2 CMOS chip design and test flow illustration

Shown in the top right corner in Fig. 1.2, silicon technology for chip manufacturing is developed by a silicon foundry. Typically, the foundry supplies a process design kit (PDK) containing compact device models for circuit simulations, a parameterized standard cell library and physical design rules for conversion of logic to circuit design, and to enable physical mapping of the circuits onto silicon. Heavy use of electronic design automation (EDA) tools is made

throughout the design flow to automate, synthesize, simulate, and validate the design and physical layout. Analog and other sensitive circuits may rely on custom design tools. Design for testability (DFT) features are added to assist in chip test and debug.

Physical design data are used for building photomasks for chip fabrication. Using a photolithographic exposure tool, the pattern on a mask reticle is transferred to a whole wafer in a step-and-repeat manner. Typical reticle exposure field on a 300 mm silicon wafer is ~850 mm^2. The reticle area can accommodate multiple chips. Additional area (scribe-line) between the exposure fields and also between chips is designated for dicing and separating the chips. Test structures are placed in this scribe-line area for process monitoring and quality control in silicon manufacturing.

Wafers are fabricated in a batch process. Chips are probed on the wafer prior to dicing and limited tests are conducted to identify good chips for packaging. Packaged chips go through more elaborate testing which may include environmental tests and burn-in. Based on the test results, chips may be binned for different products or customer applications. This is followed by product assembly and final test prior to shipment.

1.3 Tests Types and Timelines

CMOS chips are tested to guarantee chip functionality within published product specifications throughout the useful lifetime. Rapid debug of problems and determining the right course of action are key elements in developing an optimized test process. With advances in silicon and packaging technologies chip complexity has been increasing, yet the cost of testing must be contained to assure desired profitability.

Electrical tests begin early in the silicon fabrication cycle and continue on at different stages in production prior to shipping to the customer. Key characteristics may even be monitored in the field throughout the chip lifetime. Additional tests are applied to ensure long-term reliability and mechanical robustness of packaged chips. Chips for military applications are subjected to environmental stress such as temperature, humidity, shock, vibration, acceleration, and resistance to chemicals and radiation. In the USA, these specifications are issued by the US Department of Defense and known as MIL-STD, MIL-Spec, or MILSpecs.

Types of tests and test conditions are optimized to eliminate defective chips in the beginning of a long test sequence, and early in the production cycle. Failing chips are removed from further tests to reduce total test time and cost of handling. These chips are either scrapped or utilized for diagnostics, and to provide feedback for future improvements.

In Fig. 1.3 different aspects of tests and their progression with time are shown. Electrical tests are conducted at several stages during manufacturing as shown in Fig. 1.3a. Test structures for monitoring the silicon process and defect densities, and for technology model-to-hardware correlation of devices and small circuit

blocks are placed in the scribe-line area between chips. Contact to the scribe-line tests structures is made with cantilever probes landing on metal pads, each ~10^3–10^4 μm^2 in area. Data collected from electrical measurements are used for process quality control and to ensure all circuit component properties are within the range described in the compact models supplied by the silicon foundry for chip design.

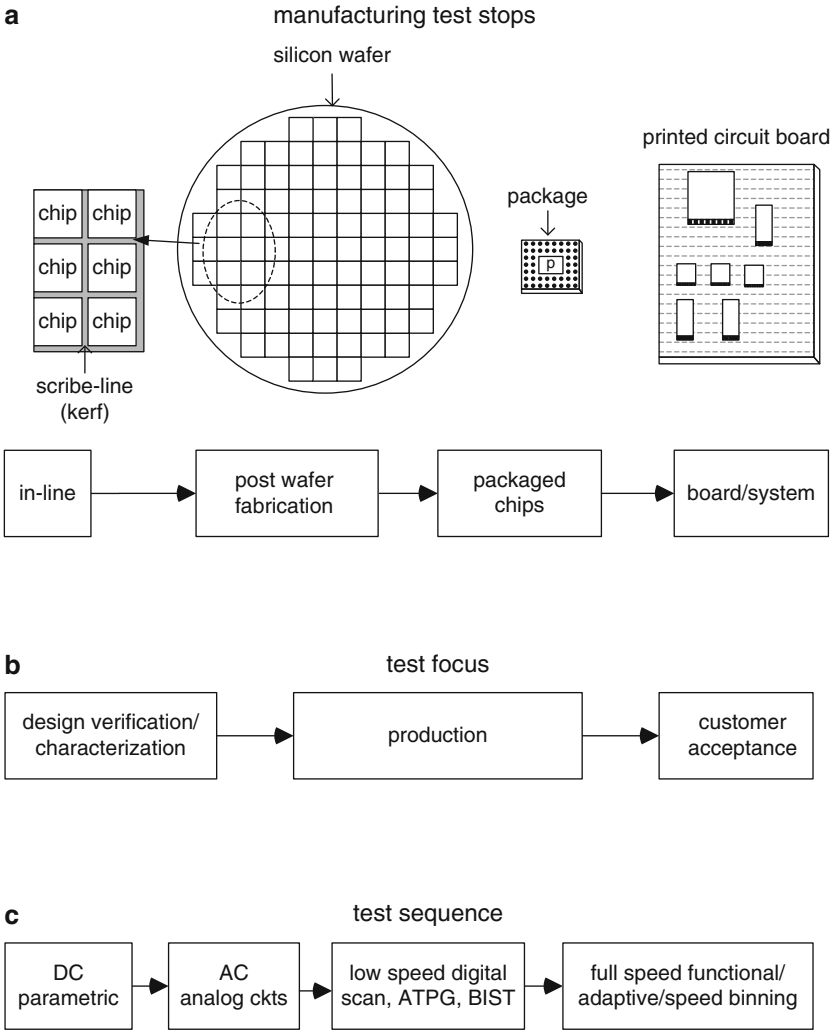

Fig. 1.3 Test timelines for (**a**) manufacturing test stops, (**b**) product development to production and (**c**) test sequence from DC to functional

After completion of the silicon manufacturing process, CMOS product chips are tested on the wafer. Electrical contacts to the chip I/Os may be made via probe pads or solder bumps. Defective chips are isolated and rejected. After dicing, good chips also called known good die (KGD) are individually packaged or placed in multi-chip modules and tested again. These chips may undergo further tests in a printed circuit board assembly or at system level.

The extent to which tests are performed and the type of tests vary as the production program moves from development to the manufacturing phase. Chips delivered to customers may undergo further tests for acceptance. This timeline is illustrated in Fig. 1.3b. The chip function as defined by the architecture, logic and circuit design is validated in the development phase prior to full-scale production. This is to ensure that the chip is performing all of its intended tasks correctly and that it will meet customer specifications over the full operating window of voltage, temperature, and other environmental variables. Chip yield, which is the ratio of the number of good chips to the total number of chips, must also be within an acceptable limit over the full range of silicon process variations. To verify this, the silicon process may be intentionally skewed to cover the range of expected process variations over time.

The number and types of tests conducted during the chip design-verification phase are typically more extensive than in routine production. In the early stages, more resources may be devoted to characterization, diagnostics, and failure analysis. The findings provide feedback to the design and silicon technology teams for making any modifications if necessary. In production mode, the number of tests is reduced while keeping the essential parametric and functional tests in the flow. If the yield falls below the set target, characterization test mode may be turned on to assist with debug. Customers may retest the chips prior to acceptance.

The sequence of different test types at wafer and package levels is outlined in Fig. 1.3c. DC parametric tests include tests for opens and shorts in the power grid and other circuit blocks, I/O pin leakage and drive currents/voltages, and leakage currents in the quiescent state (IDDQ) for different power supply domains. These tests serve to eliminate chips with gross defects from the production flow. The next set of tests is conducted on circuits that provide vital functions, such as clock generators (phase locked loops), I/O interfaces, and monitors for recording the state of the chip.

Functionality is first validated at lower frequencies for clocked storage elements (scan tests), logic and memory. The tests are generated with automated test pattern generation (ATPG), and built-in self-test (BIST) for logic and memory. For each set of input test vectors (strings of "1"s and "0"s), the output signals are compared with expected values obtained from simulation or from a KGD. Mismatches reveal errors in chip logic and design, silicon process skew or defects causing the chip to malfunction. Chips passing all earlier tests are then subjected to functional workloads at full speed and may cover the extreme ranges of operating conditions in the field. The yield may be maximized by binning chips to be operated at different frequencies, voltages, or power levels for different market offerings.

Properties of some circuit elements degrade over time; the threshold voltage of a MOSFET increases with time due to bias temperature instability (BTI), reducing its current drive, and wire resistances may increase due to electromigration. Ensuring chip operability over lifetime requires accelerated stress tests and burn-in (BI) by subjecting the chip to higher voltages and temperatures. Such tests accelerate silicon process induced defects and serve to screen "weak" chips from being shipped to customers where they may potentially fail in the field.

1.4 Test Economics

Chip fabrication is a batch process, with simultaneous processing of hundreds of chips on a wafer and typically 5–25 wafers in a lot. Chips are tested individually. The cost of testing is therefore a significant part of the total manufacturing cost. For many CMOS products, test cost may exceed silicon manufacturing cost. Major contributors to the cost of testing are shown in Fig. 1.4.

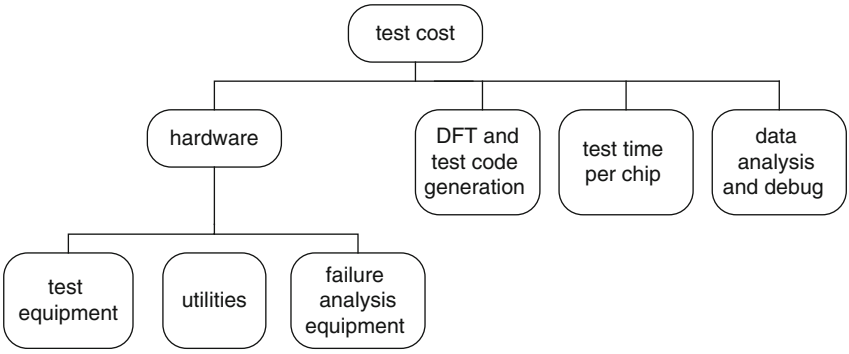

Fig. 1.4 Factors contributing to test cost

Automated test equipment (ATE), probing fixtures, wafer and package handlers, thermal control and the cost of housing and maintaining the equipment are fixed costs which may be shared among different products. Failure analysis facilities feature scanning and transmission electron microscopy, mechanical pico-probing, optical and thermal imaging, and equipment for sample preparation, delayering and materials analysis. This cost may also be shared among product lines or covered by outsourcing to failure analysis service companies.

Costs associated with test-code generation, software support for automated testing and the infrastructure for data handling, storage and analysis are considerable as well. Some of these are shared among products, but cost associated with routine test analysis and custom test-code generation unique to a chip design must

be fully absorbed by each product line individually. The cost of using the test facility and running the tests, such as utilities, is proportional to the test time. Additional resources include engineering support for diagnostics and managing throughput.

It is therefore most economical to reject bad chips early in the manufacturing process and with a minimum number of tests. However, tests conducted at full speed and those involving I/O interfaces with other components may only be conducted at package or board level, so some fallout at later test stops is inevitable. A simple rule of thumb is that the cost of rejecting a bad chip increases by a factor $>10\times$ at each subsequent test stop shown in Fig. 1.3a.

Test structures, sensors, and monitors are placed in the scribe-line and embedded on-chip for early and on-going diagnostics. The cost of design, integration, and testing of these elements is small compared to the benefits derived from their use. Parameters averaged over large circuit blocks, such as leakage current (IDDQ) and AC power give a quick readout of silicon technology and circuit design margins. Characterization and customized data analysis techniques for rapid debug may also provide a large return on investment (ROI).

1.5 Future Test Challenges

The international technology roadmap for semiconductors (ITRS) document issued once every 2 years devotes one full section to test and test equipment [1]. Advances in silicon technology and shorter time-to-market demands have generated additional challenges in high volume manufacturing (HVM) test. Some of the new key challenges in test and diagnostics as outlined in the 2013 ITRS roadmap, and related to the material covered in this book, are listed below:

- Test data feedback to tune silicon manufacturing
- Detecting systematic defects from CMOS technology, design model limitations, and changing circuit sensitivities
- Detecting variability induced defects and device degradation over time
- Adaptive testing using in-situ, feed-forward and feedback in test flow
- Incorporating on-chip test structures and sensors in the test flow to set test content and test limits
- Managing large data volumes and data traceability

The recognition and addition of these difficult challenges in the semiconductor test roadmap highlights the upcoming changes in the test arena beyond the traditional go/no-go methodology used in digital testing.

1.6 Silicon Technology and Models

The characteristics of a specific silicon technology are described through compact electrical device models, and through ground rules for mapping the devices and circuits into planar physical layers for photomask generation. In digital circuit designs, to better manage circuit simulation time, a significant level of simplification and abstraction of compact models is introduced in EDA tools for chip timing and power analysis. Design margins are imposed to account for many sources of variations in devices, silicon processes, voltages, temperatures and environmental conditions, along with aging of CMOS chips.

How well do the models and design assumptions represent the production hardware? Such questions are frequently raised when chip power/performance or yield fall below expectations, directly affecting product delivery or profit margins. To answer these questions, it is necessary to know if the models describe correct physical behavior over the entire process and application space, that this accuracy is maintained in abstractions used in EDA tools, that the design margins cover all other sources of variations such as noise and clock jitter, and that the silicon process has remained within the parameter ranges included in the models for all of the hardware.

Some of the issues mentioned above can be resolved proactively. Accuracy of models installed in the circuit design environment can be checked prior to their incorporation in more sophisticated EDA tools, and tools and design assumptions can be scrutinized before design activity begins. Model-to-hardware correlation with appropriately designed test structures may be conducted throughout the production cycle. By identifying or eliminating any existing technology or design issues first, focus can then be placed on possible test issues. With this approach the root cause of yield loss in test can be quickly and correctly ascribed.

In selecting a CMOS technology node for a particular product or in selecting a foundry for manufacturing, customers want to evaluate relative merits of the technologies being offered. Such comparisons are typically based on compact models supplied by the foundries. Hardware-to-hardware comparisons of CMOS chips manufactured in different technology generations or foundries can only be carried out if appropriately designed monitors are embedded on-chip and tested under the same conditions to bridge between technology and chip functional characteristics. A modest investment in building an infrastructure for model evaluation and model-to-hardware correlation on an on-going basis goes a long way towards making the right decisions.

1.7 Data Analysis and Characterization

Analysis, evaluation, and characterization of large volumes of electrical test data are integral parts of the test methodology. First, data collected on individual chips are analyzed. Digital test data may be automatically filtered using pass/fail criteria by matching the output vector patterns with expected signatures. Analog

measurements of currents and voltages, maximum frequency of operation of the chip, and data collected from embedded monitors and test structures placed in the scribe-line need to be correlated with design model predictions.

Statistical analysis is carried out on data collected from a large number of chips. The data are charted for visualization. Some of the charting techniques are illustrated in Fig. 1.5. These include parameter distributions, trends in parameter spreads over time, correlating parameter Y with X, and wafer maps to relate parameter variations with the geographical locations of chips on wafers. Commercial statistical analysis tools can be adapted to routinely generate a set of standard charts. Warning and alarm levels are set to alert the test team of potential or real problems. Early in the product manufacturing cycle, and when unexpected problems arise, a more detailed hands-on analysis becomes necessary. In this arena, characterization, test, chip design, and silicon manufacturing teams work together to find a solution. Cross-disciplinary knowledge is valuable in guiding the collective team to achieve rapid resolution.

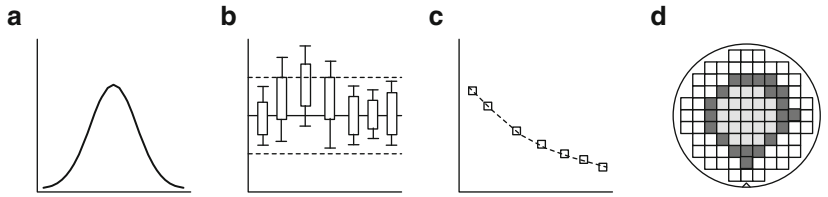

Fig. 1.5 Example charts used in characterization showing (**a**) statistical distribution, (**b**) parameter trend, (**c**) *XY* scatter plot and (**d**) gray-scaled wafer map of a parameter measured on each chip

1.8 Scope of the Book

University courses in CMOS circuit design and fabrication and VLSI testing are included in electrical engineering curricula. There are a number of excellent textbooks on VLSI design and test [2–7]. Advances in silicon technology and further miniaturization have added more complexity to design and test. There is now a greater need to combine silicon process data with chip test data to improve manufacturing efficiency and to assist in debug. This knowledge is spread across many books and publications. These serve well for in-depth views of different aspects of this multi-faceted topic, but make it challenging to get an integrated view.

Our aim in writing this book is to provide a single source for an overview of test and data analysis methodology for CMOS chips, covering circuit sensitivities to MOSFET characteristics, impact of silicon technology process variability, applications of product representative test structures and monitors, product yield, and reliability over the lifetime of the chip.

The organization of this book is similar to our book *Microelectronic Test structures for CMOS Technology* [8]. There are ten chapters, covering a full range of topics, from characteristics of circuit building blocks and impact of variability and reliability, to CMOS chip test methods and statistical data analysis. Examples are provided with circuit simulations using a simulation program with integrated circuit emphasis (SPICE). By including the full range of device parameter variations in circuit simulations, the examples emulate electrical test data typically seen in hardware.

Exercises at the end of the chapters feature practical examples of the material presented. A strong emphasis is placed on the physical behavior of circuits and on statistical methods. Knowledge derived from the physical behaviors of CMOS logic gates and memory elements can be extended to complex circuits ranging in transistor count from a few thousand to several billion.

We have used MOSFET predictive technology models (PTM) released by Arizona State University for 45, 32, and 22 nm technology nodes, and LTspice available from Linear Technology as a circuit simulator. These models and tools are freely available to all. Although the PTM models serve well to exemplify the concepts and methodologies presented for digital circuits, they have limited accuracy beyond the nominal operating range and for analog applications. Readers with access to silicon foundry models and CMOS circuit design and tool infrastructure are encouraged to use their own environment for the exercises.

Device and circuit basics are covered in Chap. 2. A methodology for setting up SPICE simulations for characterizing MOSFETs and logic gates is described. Key device and circuit parameters which can be measured during electrical testing are extracted from circuit simulations. By observing the impact of variations in these MOSFET parameters on logic gate delays, one begins to correlate device and circuit behaviors. This sets the stage for relating electrical test data back to circuit design models and tools.

Chapter 3 gives an overview of CMOS chip building blocks, from I/O and clock signal distribution to clocked storage elements (latches) and static memory arrays, emphasizing the repeated nature in circuit design and operations. Circuit simulation examples include static noise margins of SRAM cells and extraction of minimum clock cycle time and minimum operating voltage of a logic data path. We now begin to connect CMOS chip test data to characteristics of latches, logic gates, and memory elements.

In Chapter 4 MOSFET leakage current components and defect generated contributions to the measured current in the quiescent state (IDDQ) are described. Circuit simulations are carried out to model DC and AC components of power. Strategies for reducing power and on-chip power management schemes are discussed.

Embedded monitors for tracking variations in silicon process and in local power supply voltage and silicon temperature during test and operation are described in Chap. 5. Circuit simulation examples and sensitivity analysis to select an optimum set of silicon process monitors are included. Data collected from these monitors are used in variability analysis described in the next chapter. A description of sources of

variations and methods for characterizing, minimizing and accommodating variability in CMOS chips are covered in Chap. 6.

Basics of CMOS test from DC parametric to logic verification tests are covered in Chap. 7. Manufacturing yield and characterization methods to optimize chip power and performance are discussed. Adaptive test methods and binning as a means of improving chip yield are introduced.

Chapter 8 deals with reliability models and degradation mechanisms in MOSFETs and interconnects. Methods of eliminating defective chips from the manufacturing test flow by accelerated tests and burn-in, and thereby improving the CMOS chip reliability, are discussed. Strategies for guard-banding during test to assure product functionality throughout specified lifetime are included.

Basic statistics and methods for effective data visualization are presented in Chap. 9. Although some knowledge of normal statistical distributions is assumed in the examples presented in other chapters, the treatment here includes deviations from normality, small sample sizes, probabilities of multiple events and relative parameter sensitivities. Examples presented are those typically encountered in CMOS circuit simulations and product test.

In Chap. 10, methodologies for setting up device and circuit performance metrics based on models and hardware data are described. This is an essential part of evaluating both technology and product performance and comparing different products, technology nodes and technology enhancements. A methodology for evaluation of BSIM MOSFET models and circuit design tools, based on physical behaviors, highlights the need to ensure correctness of design assumptions. Circuit performance has been the subject of many debates in the industry, and it is important to have the correct measures in place for such evaluations.

Working through the examples and the exercises in each chapter with device models and simulation tools will provide readers a broadened and more detailed view of the material and reinforce a physical approach and methodology to problem resolution. We hope that engineering students as well as professional engineers working in silicon manufacturing, circuit design, and test will find this book a helpful resource in preparing to confront existing and emerging challenges in these fields.

1.9 Summary and Exercises

A brief overview of CMOS design and test is provided along with the various stages in development and production testing of CMOS chips. Economic constraints in the face of silicon process variability and shrinking design margins dictate growing emphasis on accurate device models, model-to-hardware correlation, and rapid feedback from electrical test data analysis as described in the semiconductor test roadmap. Examples provided at the beginning of the chapter relate the importance of obtaining physical insight from low complexity product representative circuit blocks that capture aggregate chip behavior. The scope of the book and contents of each chapter are described.

The following exercises are designed to develop an appreciation for modeling of complex behavior, test flow and economics, and upcoming challenges in the CMOS test arena.

1.1. A microprocessor chip with an area of 4 cm^2 consumes an average power of 100 W when running a full workload. An appreciation of how some aggregate properties of a multi-billion transistor chip relate to the properties of domestic and laboratory equipment can be gained by considering the following:
   (a) Compare the average power density of this chip under the above conditions to that of the surface of a 100 W incandescent light bulb.
   (b) If the power supply voltage V_{DD} is 1.0 V, what is the average current that must be delivered to the chip by the power supply?
   (c) What is the effective resistance of the chip as viewed from the power supply?
   (d) If the total device and interconnect capacitance between V_{DD} and ground is 1.0 μF how much charge Q is stored on the chip with $V_{DD} = 1.0$ V?
   (e) Assuming that that the microprocessor is operating at a frequency of 2 GHz, how does Q compare with the charge provided by the power supply during one machine cycle?

1.2. The fabrication cost per wafer for a product with 1,000 chips per wafer is $10,000. The test cost is $2.0 per chip. The number of chips/wafer increases by 2× per technology node, the cost of fabrication increases by 20 %, and the cost of test increases by 10 %. At this rate, after how many technology generations will the cost of test per chip exceed its cost of fabrication? Illustrate your findings graphically in one chart (assume 100 % yield).

1.3. A new EDA tool is released to measure power consumption of CMOS circuits from SPICE simulations at different voltages, temperatures, and operating frequencies. The tool developer suspects there is a bug in the software. Describe a test suite with resistors and capacitors to validate the tool without requiring complex circuit simulations.

1.4. Manufacturing decisions are often closely tied with the economic model for the product. Such decisions should always be consistent with physics based models and sound engineering judgment.
   (a) Macroeconomics is a branch of economics dealing with the aggregate behavior of the economy at the national and global levels. List fundamental differences between building a national economic model and an aggregate physical model of a CMOS chip. Can the growth in consumption and national wealth be as precisely predictable as power consumption of a CMOS chip?
   (b) A silicon foundry is consistently yielding 98 % of the wafers processed for a specific product. Management would like to increase profits and throughput by eliminating electrical tests at intermediate steps during processing. Is this a good choice? If not, build a case in favor of intermediate test stops.

1.5. The test and test equipment chapter in the ITRS roadmap describes key drivers and challenges in the test industry [1].
   (a) Select two focus areas covered in this book from Sect. 2.2.3 (Detecting Systematic Defects) and Sect. 3.1 (Electrical Test Based Diagnostics) of the 2013 roadmap.
   (b) If later ITRS roadmaps are available, i.e., ITRS 2015 and beyond, note the changes in these two focus areas over time.

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CMOS Circuits Basics

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Contents

Although a CMOS chip is a complex object comprising logic, memory, analog, and I/O functions, significant insight can be gained from the simulated and measured behaviors of circuit elements and small circuit blocks. The basic components and building blocks of digital logic circuits and their electrical properties are described. Circuit simulations are set up with BSIM models for plotting *I–V* and *C–V* characteristics of MOSFETs and extracting their key parameters. A methodology to characterize logic gates typically found in a standard cell library is introduced using an inverter as an example. Lookup tables for computing signal delays in combinational logic circuits with different input signal waveforms and load capacitances are generated, highlighting their interdependencies. Delay chains and ring oscillator configurations used for model validation in silicon hardware are described and simulated to extract delay parameters of logic gates. The foundations laid here including Monte Carlo analysis for determining parameter spreads are used throughout the book.

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