Cosmin Radu Popa

Synthesis of Computational Structures for Analog Signal Processing

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ISBN 978-1-4614-0402-6 e-ISBN 978-1-4614-0403-3
DOI 10.1007/978-1-4614-0403-3
Springer New York Dordrecht Heidelberg London

Library of Congress Control Number: 2011934510

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

This book is dedicated to my beloved daughter Ilinca Maria.

Preface

Signal processing represents an important domain of electronics, in the last years many efforts being directed for improving the performances of these structures.

The approach of the signal processing from an analog perspective presents the advantage of allowing an important reduction of the circuits' power consumption. The compact implemented structures are compatible with ultimate low-power designs and find a lot of applications such as portable equipments, wireless nano-sensors or medical implantable devices. Even the power consumption is continuous for analog circuits comparing with digital structures that consume only in the switching intervals, the possibility of an important reduction of designs' complexities and of the number of their constitutive active devices strongly decrease the medium power consumption per unity of time for analog designs. Moreover, low-power analog signal processing circuits are often implemented using subthreshold-operated MOS transistors, having extremely low values of drain currents, this fact producing an additionally lowering of the total power requested by the analog computational structures. The original approach of designing analog signal processing circuits using multifunctional structures also contributes to the decreasing of power consumption per implemented function.

Another important advantage of analog signal processing is that the speed of circuits is usually greater than the speed of digital computational circuits, allowing a real time signal processing.

Two important classes of analog signal processing circuits can be identified. The first class corresponds to linear structures, such as differential amplifier structures, multiplier circuits or active resistor structures, being necessary to develop particular linearization techniques in order to improve their general performances. The second class of analog signal processing circuits covers the area of nonlinear structures: squaring or square-rooting circuits, exponential structures or vector summation and Euclidean distance circuits. In this case, the most important goal is to minimize the approximation error of the implemented function. In order to improve the circuits' frequency response, a part of analog signal processing circuits are implemented using exclusively MOS transistors biased in saturation region. In cases in which the low-power operation is crucial, the subthreshold operation of MOS active devices represents the single choice for the designer.

In order to obtain an important reduction of design costs and of power consumption for the designed circuits, multifunctional computational structures can be implemented. Their principle of operation is based on the possibility of a multiple use of the same functional cell that is named multifunctional circuit core. As the design effort is mostly focused on the improving of the core performances and because the most important silicon area is consumed by the multifunctional core, the reutilization of this part of the multifunctional structure for all circuit functions will strongly decrease the complexity and power consumption per implemented function. The multifunctional structures present the important advantage of a relatively simple reconfiguration, small changing of the design allowing to obtain all necessary linear or nonlinear circuit functions.

The first chapter is dedicated to the presentation of linearization techniques for improving the performances of CMOS differential structures, fundamental circuits in VLSI analog and mixed-signal designs. The mathematical fundamentals are structured in eight different elementary mathematical principles, each of them being illustrated by concrete implementations in CMOS technology of their functional relations.

As it exists a relative limited number of mathematical principles that are used for implementing the multiplier circuits, the first part of Chap. 2 is dedicated to the analysis of the mathematical relations that represent the functional core of the designed circuits. In the second part of the chapter, starting from these elementary principles, there are analyzed and designed concrete multiplier circuits, grouped according to their constitutive mathematical principles. Both current and voltage multiplier circuits are presented, their operation being extensively described in Chap. 2.

The squaring function can be relatively easily obtained considering the intrinsic squaring characteristic of the MOS transistor biased in saturation region. Referring to the input variable, the squaring circuits can be clustered in two important classes: voltage squarers and current squarers, for both of them, the output variable being, usually, a current. The first part of Chap. 3 is dedicated to the analysis of the mathematical relations that represent the functional core of the designed circuits, while, in the second part of the chapter, starting from these elementary principles, there are analyzed and designed concrete squaring circuits, clustered according to their constitutive mathematical principles.

An important class of VLSI computational structures is represented by the square-root circuits. Frequently implemented using a translinear loop, they exploit the squaring characteristic of MOS transistors biased in saturation region. The presented design techniques are based on five different elementary mathematical principles, each of them being illustrated in Chap. 4 by concrete implementations in CMOS technology.

Exponential circuits represent important building blocks with many applications in VLSI designs. In CMOS technology, the exponential law is available only for the weak inversion operation of MOS transistor, the circuits designed using subthreshold-operated MOS active devices having the disadvantage of a poor frequency response. Thus, circuits realized in CMOS technology that require a good frequency response can be designed using exclusively MOS transistors biased in saturation region. The first part of Chap. 5 is dedicated to the analysis of the mathematical relations that represent the functional core of the designed circuits. In the second part of the chapter, using these elementary principles, there are analyzed and designed concrete exponential circuits, grouped according to the mathematical principles they are based on.

Chap. 6 is dedicated to the analysis and design of Euclidean distance circuits, classified (depending on their input variable), in computational structures having current-input or voltage-input vectors.

Functionally equivalent with a classical resistor, but presenting many important advantages in comparison with them, active resistor structures are extensively analyzed in Chap. 7. The goal of designing this class of active structures is mainly related to the possibility of an important reduction of the silicon area, especially for large values of the simulated resistances. The techniques presented for designing active resistor structures are based on six different elementary mathematical principles, each of them being illustrated by concrete implementations in CMOS technology.

A multitude of fundamental linear or nonlinear analog signal processing blocks can be realized starting from the same core, the optimization techniques implemented for the core being efficient for all derived circuits. The structures that can be realized starting from an improved performance multifunctional core are: differential amplifiers, multiplier circuits, active resistors (having both positive and negative controllable equivalent resistance), squaring, square-rooting or exponential circuits. Additionally, developing proper approximation functions, multifunctional structures are able to generate any continuous mathematical function. The circuits shown in Chap. 8 are based on four different elementary mathematical principles, being also presented concrete implementations in CMOS technology of these complex computational structures.

Bucharest, Romania Cosmin Radu Popa

Contents

Chapter 1
Differential Structures

1.1 Mathematical Analysis for Synthesis of Differential Amplifiers

Elementary mathematical principles represent the functional basis for designing differential structures [1–55], each theoretical principle corresponding to a class of differential amplifiers. Usually, the proper operation of these circuits uses a biasing in saturation of MOS active devices. The notations of variables are: V_1 and V_2 represent the input potentials, I_{OUT} signifies the output current, while, usually, V_O, V_{O1} and V_{O2} constant voltages are introduced for modeling a voltage shifting. In order to obtain a differential structure able to amplify with small distortions an input signal, a linear behavior of the circuit must be implemented.

1.1.1 *First Mathematical Principle (PR 1.1)*

The first mathematical principle used for implementing differential amplifiers is based on the following relations:

$$\begin{aligned}
&I_{OUT} = A\left(\sqrt{I_2} - \sqrt{I_1}\right) \\
&I_1 = \frac{K}{2}(V_{GS1} - V_T)^2 \qquad \Rightarrow I_{OUT} = A\sqrt{\frac{K}{2}}(V_2 - V_1) \\
&I_2 = \frac{K}{2}(V_{GS2} - V_T)^2 \\
&V_{GS2} - V_{GS1} = V_2 - V_1
\end{aligned} \tag{1.1}$$

The differential amplifiers based on the previous relation compute a current proportional with the differential input voltage, $V_2 - V_1$

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1.1.2 Second Mathematical Principle (PR 1.2)

The mathematical relation that models this principle is:

$$
\begin{aligned}
&\left(\frac{V_1}{2}-V_{O1}\right)^2-\left(\frac{V_2}{2}-V_{O1}\right)^2+\left(V_{O2}-\frac{V_2}{2}\right)^2-\left(V_{O2}-\frac{V_1}{2}\right)^2\\
&=\frac{V_1-V_2}{2}\left(\frac{V_1+V_2}{2}-2V_{O1}\right)+\frac{V_1-V_2}{2}\left(2V_{O2}-\frac{V_1+V_2}{2}\right)\\
&\qquad=(V_{O2}-V_{O1})(V_1-V_2)=ct.\,(V_1-V_2)
\end{aligned}
\tag{1.2}
$$

The circuits that use this principle generate a current proportional with the differential input voltage, $V_1 - V_2$.

1.1.3 Third Mathematical Principle (PR 1.3)

This principle is illustrated by the following mathematical relation:

$$
\begin{aligned}
&\left[A(V_1-V_2)^2+B(V_1-V_2)+C\right]-\left[A(V_1-V_2)^2-B(V_1-V_2)+C\right]\\
&\qquad=2B(V_1-V_2)
\end{aligned}
\tag{1.3}
$$

The output current will be also proportional with the differential input voltage, $V_1 - V_2$

1.1.4 Fourth Mathematical Principle (PR 1.4)

The mathematical relation that models this principle is:

$$
\begin{aligned}
&\left(V_C-V_O-V_T+\frac{V_1}{2}\right)^2+\left(V_O-V_T+\frac{V_1}{2}\right)^2-\left(V_C-V_O-V_T-\frac{V_1}{2}\right)^2\\
&\qquad-\left(V_O-V_T-\frac{V_1}{2}\right)^2=V_1(2V_C-2V_O-2V_T)\\
&\qquad\qquad+V_1(2V_O-2V_T)=2V_1(V_C-2V_T)
\end{aligned}
\tag{1.4}
$$

The output current of the differential amplifier is linearly dependent on the input voltage, V_1.

1.1.5 Fifth Mathematical Principle (PR 1.5)

The fifth mathematical principle can be written as follows:

$$I_{OUT} = \frac{V_1 - V_2}{2}\sqrt{4K\left[I_O + \frac{K}{4}(V_1 - V_2)^2\right] - K^2(V_1 - V_2)^2}$$
$$= \sqrt{KI_O}(V_1 - V_2) \tag{1.5}$$

1.1.6 Sixth Mathematical Principle (PR 1.6)

The method modeled by this mathematical principle, used for linearizing the transfer characteristic of differential structures, uses an anti-parallel connection of two differential amplifiers, the controlled asymmetries between their biasing currents, also between the aspect ratios of their transistors fulfilling this desiderate.

1.1.7 Seventh Mathematical Principle (PR 1.7)

This principle is useful for obtaining a rail-to-rail operation of a differential structure, based on a parallel connection of two complementary differential amplifiers. The mathematical relations of this principle are shown in the following lines:

$$I_{OUT} = \sqrt{2K}\left(\sqrt{I_{Op}} + \sqrt{I_{On}}\right)(V_1 - V_2) \tag{1.6}$$

$$\sqrt{I_{On}} + \sqrt{I_{Op}} = 2\sqrt{I_O} \tag{1.7}$$

resulting:

$$I_{OUT} = \sqrt{8KI_O}(V_1 - V_2) \tag{1.8}$$

1.1.8 Different Mathematical Principle for Differential Amplifiers (PR 1.D)

There are some circuits based on different mathematical principles that are useful for linearizing the behavior of differential amplifiers.

1.2 Analysis and Design of Differential Structures

The classical MOS differential presents a strong nonlinear behavior, as a result of the quadratic characteristic of their constitutive transistors biased in saturation region. In order to improve the linearity of the structure, it is necessary to develop efficient linearization techniques, functional mathematical principles being elaborated for fulfilling this desiderate.

Based on the previous presented mathematical analysis, it is possible to design different types of differential structures, included in eight classes, corresponding to the previous presented eight mathematical principles (PR 1.1 – PR 1.7 and PR 1.D).

The MOS differential amplifier represents a fundamental block in analog design, having a large area of applications. The analysis of the large signal operation for the classical MOS differential structure (Fig. 1.1) [1, 2] can quantitatively evaluate the circuit's nonlinearity, being possible to determine the weight of each superior-order distortion introduced by the structure nonlinearity.

The $V_I = V_1 - V_2$ differential input voltage can be expressed as follows:

$$V_I = V_{GS1} - V_{GS2} = \left(V_T + \sqrt{\frac{2I_1}{K}}\right) - \left(V_T + \sqrt{\frac{2I_2}{K}}\right) = \sqrt{\frac{2}{K}}\left(\sqrt{I_1} - \sqrt{I_2}\right) \quad (1.9)$$

Squaring and replacing the sum $I_1 + I_2$ with I_O, it results:

$$2\sqrt{I_1(I_O - I_1)} = I_O - \frac{KV_I^2}{2} \quad (1.10)$$

The resultant second-order equation will be:

$$I_1^2 - I_O I_1 + \frac{1}{4}\left(I_O - \frac{KV_I^2}{2}\right)^2 = 0 \quad (1.11)$$

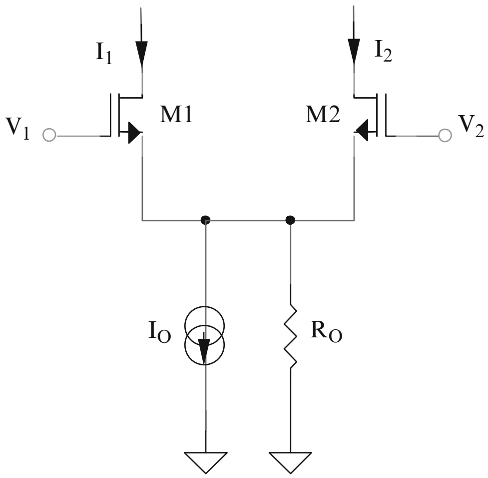

Fig. 1.1 Classical MOS differential structure

having the following solutions:

$$(I_1)_{1,2} = \frac{I_O}{2} \pm \frac{I_O}{2}\sqrt{\frac{KV_I^2}{I_O} - \frac{K^2V_I^4}{4I_O^2}} \tag{1.12}$$

so:

$$I_1 = \frac{I_O}{2} + \frac{I_O}{2}\sqrt{\frac{KV_I^2}{I_O} - \frac{K^2V_I^4}{4I_O^2}}; \quad I_2 = \frac{I_O}{2} - \frac{I_O}{2}\sqrt{\frac{KV_I^2}{I_O} - \frac{K^2V_I^4}{4I_O^2}} \tag{1.13}$$

The output differential current will be:

$$I_2 - I_1 = -I_O\sqrt{\frac{KV_I^2}{I_O} - \frac{K^2V_I^4}{4I_O^2}} = -\frac{V_I}{2}\sqrt{4KI_O - K^2V_I^2} \tag{1.14}$$

The $(I_2 - I_1)(V_I)$ function is strongly nonlinear, the quantitative evaluation of its nonlinearity being possible using a Taylor series expansion. So, it is necessary to compute the superior-order derivates of the following function:

$$f(V_I) = \sqrt{4KI_O - K^2V_I^2} \tag{1.15}$$

and their values for $V_I = 0$ The first-order derivate is:

$$f'(V_I) = -K^2V_I\left(4KI_O - K^2V_I^2\right)^{-1/2} \tag{1.16}$$

while the second-order one has the following expression:

$$f''(V_I) = -4K^3I_O\left(4KI_O - K^2V_I^2\right)^{-3/2} \tag{1.17}$$

resulting:

$$f'(V_I)|_{V_I=0} = 0 \tag{1.18}$$

$$f''(V_I)|_{V_I=0} = -\frac{1}{2}K^{3/2}I_O^{-1/2} \tag{1.19}$$

The Taylor series expansion of the function (1.14) gives:

$$(I_2 - I_1)\,(V_I) = -K^{1/2}I_O^{1/2}V_I + \frac{K^{3/2}}{8I_O^{1/2}}V_I^3 + \frac{K^{5/2}}{128I_O^{3/2}}V_I^5 + \cdots \tag{1.20}$$

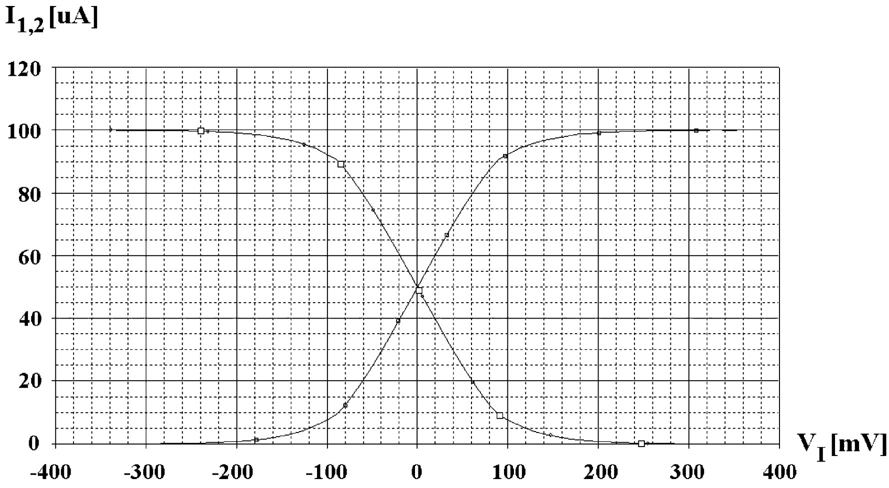

Fig. 1.2 The $I_1(V_I)$ and $I_2(V_I)$ dependencies for the classical differential amplifier

or:

$$(I_2 - I_1)(V_I) = a_1 V_I + a_3 V_I^3 + a_5 V_I^5 + \cdots \tag{1.21}$$

The first term is linearly dependent on the input voltage, while the last two terms model the third-order and fifth-order nonlinearities of the differential structure.

The dependencies of the drain currents I_1 and I_2 on the differential input voltage V_I for the differential amplifier from Fig. 1.1 are presented in Fig. 1.2.

Considering a load resistance $R_L = 10\,\mathrm{k}\,\Omega$, the simulation of the transfer characteristic $V_O(V_I) = R_L(I_2 - I_1)(V_I)$ for the differential amplifier presented in Fig. 1.1 is shown in Fig. 1.3.

The simulation of the transfer characteristic $V_O(V_I)$ for a maximal input range between -0.4 V and 0.4 V and a biasing current I_O having the values 0.1 mA, 0.2 mA and 0.3 mA is shown in Fig. 1.4. It could be remarked an increasing of the differential-mode voltage gain for an increasing of the biasing current I_O (using relation (1.20)), the doubling of the biasing current generating an increasing of $\sqrt{2}$ of the voltage gain.

The voltage gain is -10.95 (using relation (1.20)), while the simulated value is -10.43.

Fig. 1.5 presents the simulation of the transfer characteristic of the differential amplifier for different values of the common-mode input voltage $V_C = (V_1 + V_2)/2$ (between 1 V and 1.3 V), showing a minimal value of V_C of about 1.2 V. The simulation was made considering a passive load attached to the differential amplifier from Fig. 1.1, having $R_1 = R_2 = 10$ k Ω and a supply voltage $V_{DD} = 9$ V.

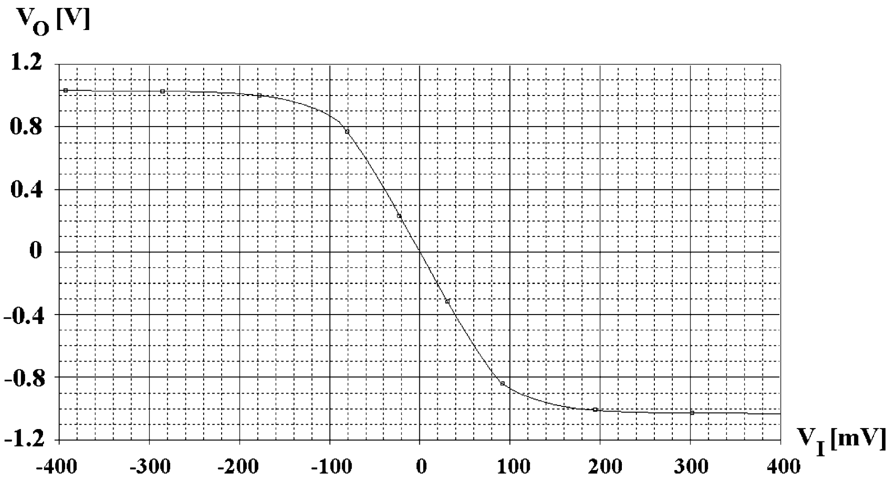

Fig. 1.3 The $V_O(V_I)$ dependence for the classical differential amplifier

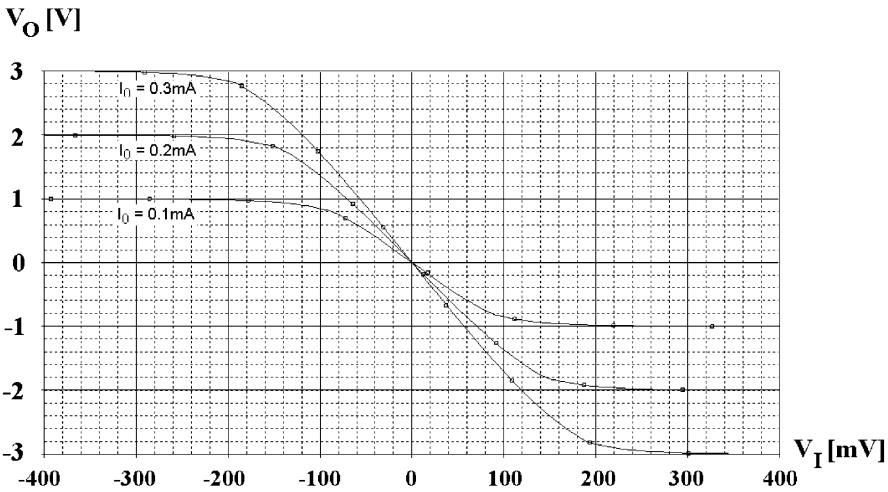

Fig. 1.4 Parametric $V_O(V_I)$dependence for the classical differential amplifier

Figure 1.6 represents the simulation of the transfer characteristic of the differential amplifier for different values of the common-mode input voltage $V_C = (V_1 + V_2)/2$ (between 8.9 V and 9.1 V), showing a maximal value for V_C of about 9 V. The simulation was made considering a particular implementation of the current source I_O from Fig. 1.1 using a classical current mirror.

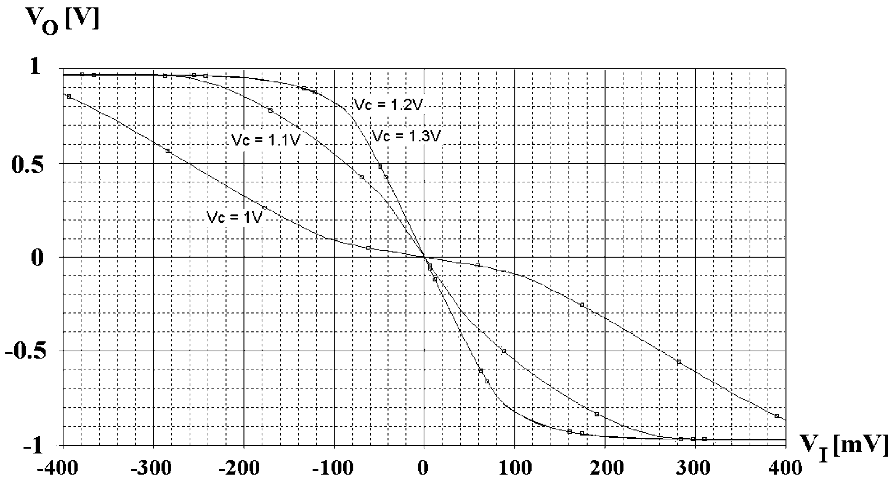

Fig. 1.5 The $V_O(V_I)$ dependence for multiple common-mode input voltages (1)

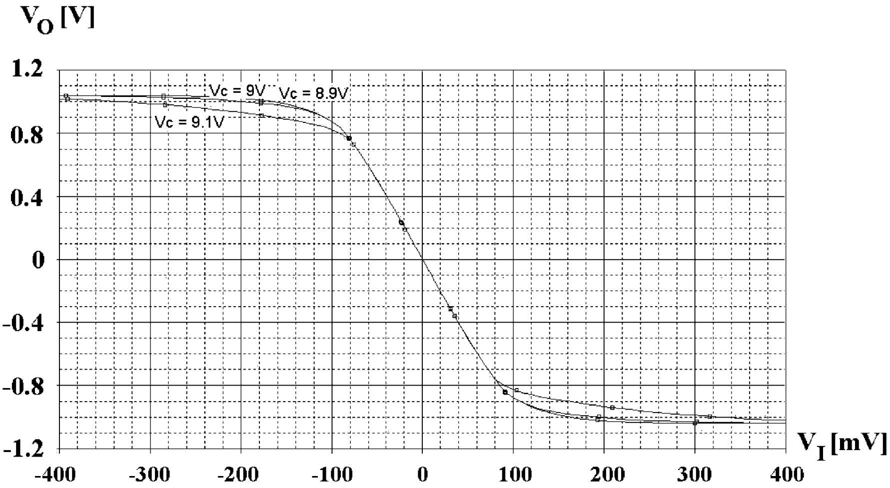

Fig. 1.6 The $V_O(V_I)$ dependence for multiple common-mode input voltages (2)

1.2.1 Differential Structures Based on the First Mathematical Principle (PR 1.1)

The method for obtaining a linear transfer characteristic of the differential amplifier based on the first mathematical principle (PR 1.1) uses the compensation of the squaring characteristic of the MOS transistor biased in saturation using complementary square-root circuits.

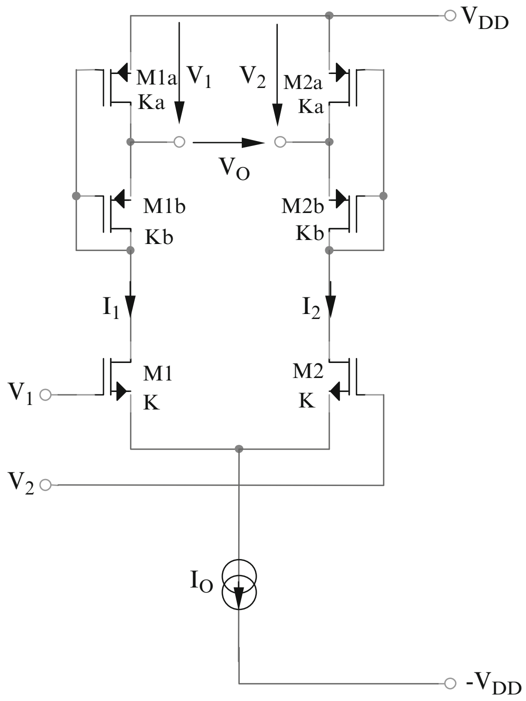

Fig. 1.7 Differential structures (1) based on PR 1.1

The first circuit using this method is shown in Fig. 1.7 [3] and it uses two square-root circuits for improving the linearity of the differential amplifier.

Using relation that describes the operation of M1a–M1b and M2a–M2b square-root circuits, the output voltage of the differential amplifier from Fig. 1.7 will be:

$$V_O = V_2 - V_1 = \sqrt{2I_2}\left(\sqrt{\frac{1}{K_a} + \frac{1}{K_b}} - \sqrt{\frac{1}{K_b}}\right) - \sqrt{2I_1}\left(\sqrt{\frac{1}{K_a} + \frac{1}{K_b}} - \sqrt{\frac{1}{K_b}}\right) \quad (1.22)$$

Because:

$$\sqrt{I_2} - \sqrt{I_1} = \sqrt{\frac{K}{2}}(V_{GS2} - V_{GS1}) = \sqrt{\frac{K}{2}}(V_2 - V_1) \quad (1.23)$$

it results:

$$V_O = \sqrt{K}\left(\sqrt{\frac{1}{K_a} + \frac{1}{K_b}} - \sqrt{\frac{1}{K_b}}\right)(V_2 - V_1) \quad (1.24)$$

equivalent with a linear dependence of the output voltage on the differential input voltage.

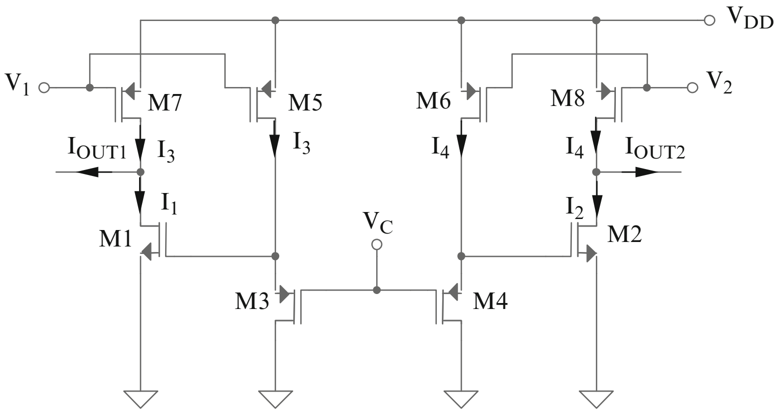

Fig. 1.8 Differential structures (2) based on PR 1.1

The principle of operation for the differential amplifier shown in Fig. 1.8 [4] is based on the compensation of the squaring characteristic of parallel-coupled differential amplifiers M5–M6 and M7–M8 by two square-rooting circuits, M1–M3 and M2–M4. The principle of operation is similar with the principle of the circuit presented in Fig. 1.7, the advantage being the exclusively biasing in saturation of all MOS transistors.

The differential output current of the circuit can be expressed as follows:

$$I_{OUT1} - I_{OUT2} = (I_3 - I_1) - (I_4 - I_2) \tag{1.25}$$

The constant potential V_C is equal with the difference between two gate-source voltages. Supposing a biasing in saturation of all identical MOS transistors, it results:

$$V_C = V_{GS1} - V_{SG3} = \sqrt{\frac{2I_1}{K}} - \sqrt{\frac{2I_3}{K}} \tag{1.26}$$

So:

$$\sqrt{I_1} = \sqrt{I_3} + \sqrt{\frac{K}{2}} V_C \tag{1.27}$$

resulting:

$$I_1 = I_3 + \frac{K}{2} V_C^2 + \sqrt{2KI_3}\, V_C \tag{1.28}$$

and, similarly:

$$I_2 = I_4 + \frac{K}{2} V_C^2 + \sqrt{2KI_4}\, V_C \tag{1.29}$$

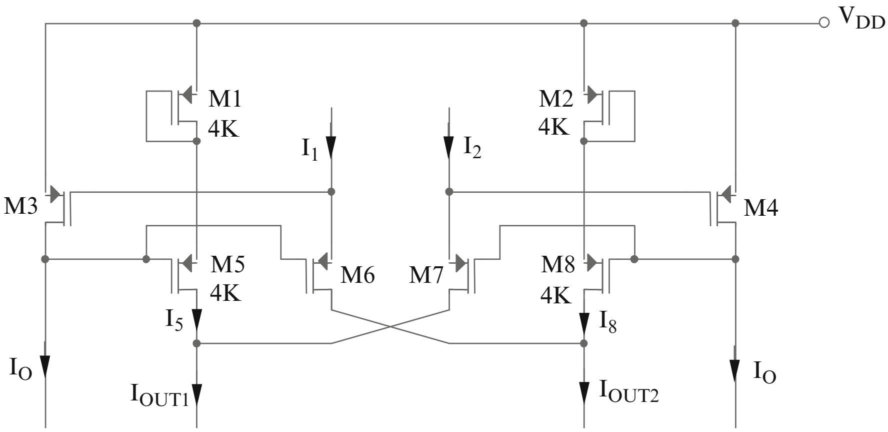

Fig. 1.9 Current-mode square-root circuit (1)

From (1.25), (1.28) and (1.29), it results a square-root dependence of the differential output current on the input currents:

$$I_{OUT1} - I_{OUT2} = \sqrt{2K}\, V_C \left(\sqrt{I_4} - \sqrt{I_3}\right) \tag{1.30}$$

The differential expression $\sqrt{I_4} - \sqrt{I_3}$ is a function of the input potentials V_1 and V_2, as follows:

$$\begin{aligned}\sqrt{I_4} - \sqrt{I_3} &= \sqrt{\frac{K}{2}}(V_{SG6} - V_T) - \sqrt{\frac{K}{2}}(V_{SG5} - V_T) \\ &= \sqrt{\frac{K}{2}}(V_{SG6} - V_{SG5}) = \sqrt{\frac{K}{2}}(V_1 - V_2)\end{aligned} \tag{1.31}$$

From (1.30) and (1.31), it results a linear dependence of the output current on the differential input voltage:

$$I_{OUT1} - I_{OUT2} = KV_C(V_1 - V_2) \tag{1.32}$$

Alternate implementations of square-root circuits used for linearizing the transfer characteristic of the classical differential amplifier are shown in Figs. 1.9–1.13 [4].

For the square-root circuit shown in Fig. 1.9, the translinear loop realized using M1, M3, M5 and M6 transistors has the following characteristic equation:

$$V_{SG3} + V_{SG6} = V_{SG1} + V_{SG5} \tag{1.33}$$

So:

$$\sqrt{I_O} + \sqrt{I_1} = \sqrt{I_5} \tag{1.34}$$

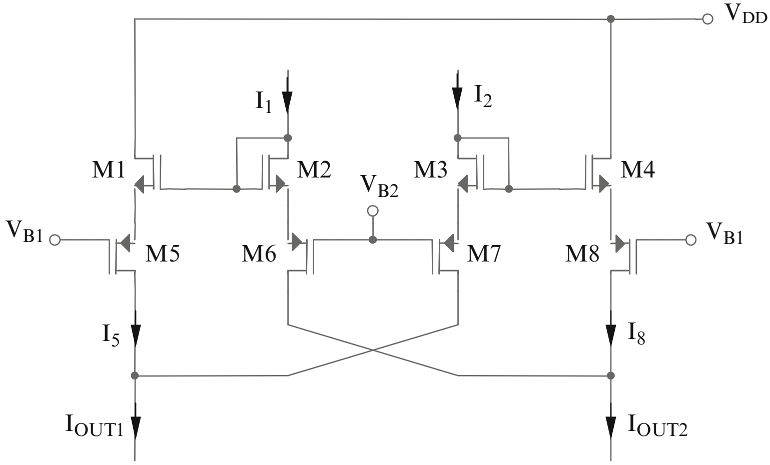

Fig. 1.10 Current-mode square-root circuit (2)

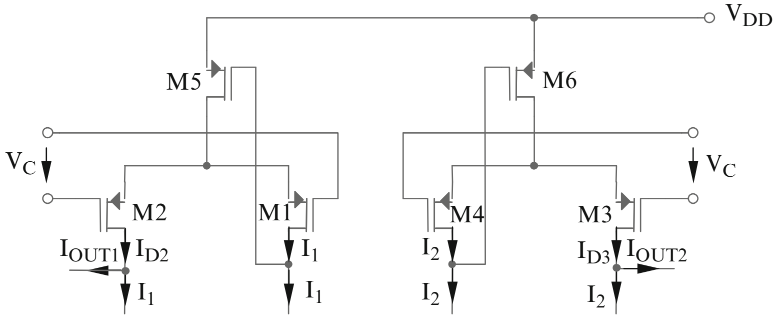

Fig. 1.11 Current-mode square-root circuit (3)

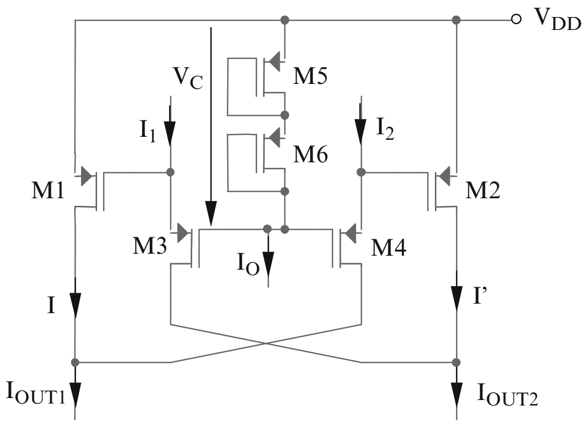

Fig. 1.12 Current-mode square-root circuit (4)

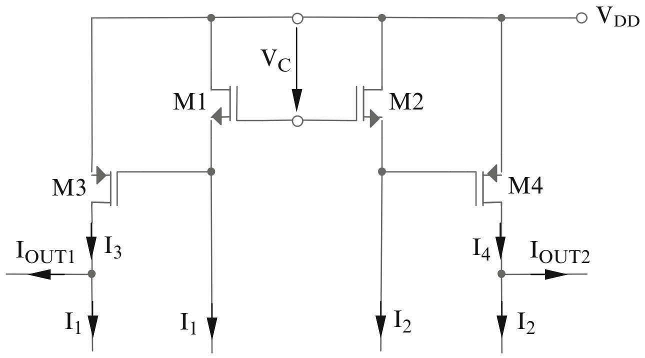

Fig. 1.13 Current-mode square-root circuit (5)

Squaring the previous relation, it is possible to write that:

$$I_5 = I_O + I_1 + 2\sqrt{I_O I_1} \tag{1.35}$$

In a similar way, it results, from the right part of the circuit:

$$I_8 = I_O + I_2 + 2\sqrt{I_O I_2} \tag{1.36}$$

The differential output current of the squaring structure can be expressed as follows:

$$I_{OUT1} - I_{OUT2} = (I_5 + I_2) - (I_8 + I_1) = 2\sqrt{I_O}\left(\sqrt{I_1} - \sqrt{I_2}\right) \tag{1.37}$$

In order to obtain a linear differential amplifier, the square-root circuit shown in Fig. 1.9 must have as input currents the drain currents I_1 and I_2 of a classical differential amplifier M9–M10, resulting the circuit presented in Fig. 1.14. [4]

The differential output current of this circuit can be obtained replacing the expressions of I_1 and I_2 drain currents by their squaring dependencies on the gate-source voltages:

$$I_{OUT1} - I_{OUT2} = 2\sqrt{I_O}\sqrt{\frac{K}{2}}(V_{SG9} - V_{SG10}) = \sqrt{2KI_O}(V_2 - V_1) \tag{1.38}$$

For the square-root circuit presented in Fig. 1.10, the translinear loop achieved using M1, M2, M5 and M6 transistors has the following characteristic equation:

$$V_{B2} - V_{B1} = (V_{GS1} + V_{SG5}) - (V_{GS2} + V_{SG6}) \tag{1.39}$$

resulting:

$$(V_{B2} - V_{B1})\sqrt{\frac{K}{2}} = 2\sqrt{I_5} - 2\sqrt{I_1} \tag{1.40}$$