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VCO-Based Quantizers Using Frequency-to-Digital and Time-to-Digital Converters

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Preface

Traditional analog-to-digital converters (ADCs) face many design challenges as technology scales. A few of these challenges are (1) voltage dynamic range decreases making it difficult to accurately quantize in the voltage domain (2) architecture contains many analog components which are challenging to design in deep submicron complementary metal oxide semiconductor (CMOS) processes. Voltage-controlled oscillator (VCO)-based ADCs are gaining popularity due to the highly digital architecture and improved timing resolution in deep submicron CMOS processes.

This book presents a theoretical and modeling approach to understanding the VCO-based quantizer. Two digital time quantizer architectures are reviewed: one using a frequency-to-digital converter (FDC) and the other using a time-to-digital converter (TDC). The TDC architecture is new to the application of the VCO-based quantizer.

Chapter 1 provides an introduction including the motivation for this topic, background on the subject, and goals of this work.

Chapter 2 provides an introduction and theoretical analysis of the FDC and TDC VCO-based quantizer. Theoretical equations are developed to determine the resolution of the quantizers and verified through a VerilogA model.

Chapter 3 provides modeling and analysis of circuit nonidealities of the VCO-based quantizer. These nonidealities are added to the VerilogA model and theoretical equations derived to verify the effects on both the FDC and TDC architecture.

Chapter 4 provides some final thoughts and analysis on the FDC and TDC VCO-based quantizer.

Chapter 5 concludes the book.

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