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Design, Analysis and Test of Logic Circuits Under Uncertainty

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Foreword

Mainstream electronic systems typically assume that transistors and interconnects operate correctly over their useful lifetime. With enormous complexity and significantly increased vulnerability to failures compared to the past, future system designs cannot rely on such assumptions. Robust design is now required to ensure that such systems perform correctly despite rising complexity and increasing disturbances.

The coming generations of silicon technologies have remarkably small circuit geometries. Consequently, several causes of hardware failures, largely benign in the past, are becoming significant at the system level. Factors such as transient errors, device degradation, and variability induced by manufacturing and operating conditions are becoming much more important. Even if error rates stay constant on a per bit basis, total chip-level error rates grow with the scale of integration. Furthermore, several emerging nanotechnologies are inherently highly subject to imperfections.

Approaches exist for building electronic systems that can tolerate hardware failures, but the associated costs are too high for many applications. For example, expensive redundancy techniques have been used in space electronics and high-end mainframes. The most significant challenge is to design future electronic systems that can tolerate errors in their underlying hardware at very low (power, performance, area) costs—much lower than traditional redundancy. It will be impossible to meet this challenge unless we address the following issues:

1. Understand the characteristics of various failure mechanisms at the circuit level.
2. Analyze their effects on system behavior.
3. Create very low-cost methods to handle a wide range of failure mechanisms.
4. Optimize an overall design to achieve the required levels of reliability at the lowest cost.
5. Validate actual hardware prototypes to ensure that the designs function correctly.

This book by Dr. Smita Krishnaswamy, Prof. Igor Markov, and Prof. John P. Hayes introduces powerful analysis frameworks that will enable designers to address the above issues. Their formalisms are flexible because they are able to represent a variety of erroneous behaviors. Their systematic methods for reasoning about reliability allow designers to incorporate efficient error protection techniques into their designs. Also, their testing techniques provide insights into effective design of experiments for validating error protection techniques using hardware prototypes. Overall, the techniques presented here will enable Electronic Design Automation tool developers to create new design analysis and optimization tools that have reliability as a primary design objective together with power, performance and area.

Of course, there are numerous open questions in this area. This book introduces researchers and practitioners to some of these open questions as well. I hope it will inspire its readers to further advance the state of the art. I am excited about this book, and I hope that you will be as well!

Stanford, CA, April 2011 Subhasish Mitra

Preface

Integrated circuits (ICs) are becoming increasingly susceptible to uncertainty caused by soft errors, inherently probabilistic devices, and manufacturing variability. As device technologies scale, these effects can be detrimental to circuit reliability. In order to address this issue, we develop methods for analyzing, designing, and testing circuits subject to probabilistic effects. The main contributions of this work are: (1) a matrix-based reliability analysis framework that can capture probabilistic behavior at the logic level, (2) test generation and test compaction methods aimed at probabilistic faults in logic circuits, (3) a fast, soft-error rate (SER) analyzer that uses functional-simulation signatures to capture error effects, and (4) novel design techniques that improve reliability using little area and performance overhead.

First, we develop a formalism to represent faulty gate behavior by means of stochastic matrices called probabilistic transfer matrices (PTMs). PTM algebra provides a stochastic alternative to the deterministic role played by Boolean algebra. To improve computational efficiency, PTMs are, in turn, compressed into algebraic decision diagrams (ADDs), and ADD algorithms are developed for the corresponding matrix operations.

We propose new algorithms for circuit testing under probabilistic faults. This context requires a reformulation of existing techniques for circuit testing. For instance, a given fault may remain undetected by a given test vector, unless the test vector is repeated sufficiently many times. Also, since different vectors detect the same fault with different probabilities, the number of repetitions required is a key issue in probabilistic testing. We develop test generation methods that account for these differences, and linear programming (LP) formulations to optimize test sets for various objectives.

Next, we propose simulation-based methods to approximately compute reliability under probabilistic faults in practical settings. We observe that the probability of an error being logically masked is closely related to node testability. We use functional-simulation signatures, i.e., partial truth tables, to efficiently compute testability measures (signal probability and observability). To account for timing masking, we compute error-latching windows from timing analysis information.

Electrical masking is incorporated into our estimates through derating factors for gate error probabilities. The SER of a circuit is computed by combining the effects of all three masking mechanisms within a SER analyzer called AnSER.

Based on AnSER, we develop several low-overhead techniques that increase reliability, including: (1) a design method called SiDeR to enhance circuit reliability using partial redundancy already present within the circuit, (2) a guided local rewriting technique to resynthesize small windows of logic to improve area and reliability simultaneously, and (3) a post-placement gate-relocation technique that increases timing masking by decreasing the error-latching window of each gate, and (4) ILP algorithms to retime sequential circuits for increased reliability and testability.

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Chapter 1
Introduction

Digital computers have always been vulnerable to a variety of manufacturing and wear-out defects. Integrated circuit (IC) chips, which lie at the heart of modern computers, are subject to silicon-surface imperfections, contaminants, wire shorts, etc. Due to the prevalence of such defects, various forms of fault tolerance have been built into digital systems since the 1960s. For example, the first computers NASA sent to space were equipped with triple-modular redundancy (TMR) [1] to protect their internal logic from defects.

Over time, IC technology scaling has brought forth heightened device sensitivity to a different kind of error, known as a soft, or transient, error. Soft errors are caused by external noise or radiation that temporarily affects circuit behavior without permanently damaging the hardware. They first became problematic in the 1970s, when scientists at Intel noticed that DRAM cells experienced spontaneous bit-flips that could not be replicated. May and Woods [2] discovered that these errors were a result of α-particles emitted by trace amounts of radioactive material in ceramic chip packaging. Although the α-particle problem was eliminated for a period of time by using plastic packaging material, other sources of soft error soon became apparent. Later that year, Ziegler et al. [3] at IBM, showed that neutrons produced by cosmic rays from outer space, could also cause errors. The neutrons could strike the p-n junctions of transistors and create enough electron–hole pairs for current to flow through the junctions.

With the advent of nanoscale computing, soft errors are beginning to affect not only memory but also combinational logic. Unlike errors in memory, errors in combinational logic cannot be easily corrected and can lead to system failures, with potentially disastrous results in error-critical systems such as pacemakers, spacecraft, and servers.

New device technologies such as carbon nanotubes (CNTs), resonant tunneling diodes (RTDs), and quantum computers exhibit inherently probabilistic behavior due to various nanoscale and quantum–mechanical effects. Resilience under these sources of uncertainty is vital for technology and performance improvements. Due to the cost and high power consumption of modern ICs, the widespread addition of

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redundancy is not a practical option for curtailing error rates. Instead, careful circuit analysis and low-cost methods of improving reliability are necessary. Further, circuits must be tested post-manufacture for their vulnerability to transient faults as well as to manufacturing defects.

In the remainder of this chapter, we review technology trends that lead to increased uncertainty in circuit behavior. We also survey previous work on soft-error rate (SER) analysis, fault-tolerant design, SER testing, and probabilistic-circuit analysis. After stating the goals of our research, we outline the remaining chapters.

1.1 Background and Motivation

Soft errors are one of the main causes of uncertainty and failure in logic circuits [4]. Current trends in circuit technology exacerbate the frequency and impact of soft errors. In this section, we describe soft errors and how they affect circuit behavior. We also survey technology trends, from current CMOS ICs to quantum devices.

1.1.1 Soft Errors

A soft error is a *transient* signal with an incorrect logic value. Soft errors can be caused by cosmic rays including α-particles, and even thermal noise. Cosmic particles can originate from supernovas or solar flares, and enter the Earth's atmosphere. They are estimated to consist of 92 % protons, 6 % α-particles, and 2 % heavy nuclei [5]. When primary cosmic particles enter the atmosphere, they can create a shower of secondary and tertiary particles, as shown in Fig. 1.1. Some of these particles can eventually reach the ground and disturb circuit behavior.

While cosmic rays are more problematic at higher altitudes, α-particles can affect circuits at any altitude. An α-particle (or equivalently, a helium nucleus) consists of two protons and two neutrons that are bound together. They are emitted by radioactive elements, such as the uranium or lead isotopes in chip-packaging materials. When packaging materials were improved in the 1980s, the problem was eliminated to a large extent; however, as device technologies scale down towards 32 nm, the particle energy required to upset the state of registers and memory circuits becomes smaller. Heidel et al. [6] show that even at 1.25 MeV, incident particles can alter the state of latches, depending on the angle of incidence. As the energy threshold for causing an error decreases, the number of particles with sufficient energy to cause errors increases rapidly [7]. For instance, even the lead in solder balls or trace amounts of radioactive contaminants in tin can affect CMOS circuits at lower energy levels [8].

When a particle actually strikes an integrated semiconductor circuit and lands in the sensitive area of a logic gate, it can cause an ionized track in silicon, known as a single-event upset (SEU), as illustrated in Fig. 1.2. An SEU is a transient fault, or soft fault as opposed to a permanent fault. The effects of an SEU do not propagate if