# FIELD EFFECT TRANSISTORS

Edited by
P. Suveetha Dhanaselvam
Srinivasa Rao Karumuri
Shiromani Balmukund Rahi
Dharmendra Singh Yadav

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*Publishers at Scrivener*
Martin Scrivener (martin@scrivenerpublishing.com)
Phillip Carmical (pcarmical@scrivenerpublishing.com)

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# Preface

The aim of this book is to uncover the complexities of the technological marvels through pioneering designs like Nanosheet FET, NC FET, Junction less MOSFET, NC TFET, Tunnel FET, Fe MOSFET GAA etc. The idea is to provide an understanding of these transistors, showcasing their attributes and applications. . One of the device architecture Tunnel Field Effect Transistor (TFET) has a lower subthreshold swing with the added benefit of reduced leakage current under OFF state. Despite its many advantages over MOSFET, TFET has a low ON current. To overcome this challenge as well as to simplify complex fabrication process, "junctionless tunnel field effect transistor (JL-TFET)" was constructed. TFET and JL-TFET work on the same mechanism of band-to-band tunneling and is therefore expected to help in the reduction of power consumption. In this book we are analysing the different structure of existing JL-TFET and simulating a junctionless transistor using TCAD tool. The book starts with discussing the quantum physics approach of tunneling then short comings of MOSFET technology and finally move towards the TFET technology. Physics and working mechanism of the TFET in ON-state, OFF-state, ambipolar state is explained in detailed manner.

The application of FET as biosensors have enlarged the need for the device and it is also discussed in detail. Various applications of nanoscale FETs are explored, including the detection of biomolecules, label-free sensing, studies on protein-protein interactions, DNA/RNA sensing with high specificity and sensitivity, pathogen detection and the early detection of cancer biomarkers. Following that, Nanosheet FETs and Nanowire FETs, offering superior control over current flow and enhanced device performance, are examined. The challenges of the short channel effect and methods to overcome them are also discussed. A comprehensive overview of these modern Field Effect Transistors, including their design principles, operational characteristics, and potential applications is provided. The future trends and innovations in FET technology are contemplated, offering readers a glimpse into the exciting possibilities on the horizon. This book serves as a foundational exploration, bridging historical context with contemporary advancements, and providing readers with a holistic understanding of the multifaceted world of Field Effect Transistors. Eventhough multigate FETs are superior in many aspects , there are certain limitations especially when scaled beyond. This is slowly ratified in the emerging alternate devices like spintronics, carbon nanotubes, photonics, Graphene materials, HEMT, etc.. This book also highlights the basic concepts of these emerging technologies and it also discusses the features for future applications. This book also provides a comprehensive exploration of Nanowire Transistors (NWTs) as a transformative element in semiconductor technology. The integration of SNTs into existing frameworks and the exploration of novel architectures promise to redefine the boundaries of performance and energy efficiency in electronic systems.

In the next few chapters of the book, we present a comprehensive exploration of the fundamental concepts underlying Heterojunction Tunnel Field-Effect Transistors (HTFETs), a novel transistor paradigm with immense potential for ultra-low power applications. This book also provides insights in to device physics and a comprehensive analysis of the electrical characteristics of Gate oxide Overlap on to Source HTFET (GOS HTFET).

A new approach to improving FET design is presented in this book, utilizing machine learning (ML). Collecting and assembling large datasets is the first step in the process. Then comes feature engineering and the use of different machine learning models, such as neural networks, decision trees, and regression. This model training and validation process rapidly explores the FET design space. ML-driven FET designs can be applied in real-world applications due to advancements in the manufacturing process.

In the last few chapters, HEMTs—particularly those based on III–IV materials like InSb—have been discussed which becomes essential in the search for electronic components that are quicker, more effective, and have a larger capacity. The scaling of electronic systems is still driven by the study of novel nanoelectronic devices and the convergence of technologies, with HEMTs being a key facilitator of these developments. The role of HFETs in future communication systems pertaining to consumer market, defense sector and space related applications have been discussed in detail.

The significant gains in channel engineering and device fabrication techniques have influenced the continued scaling of devices. The semiconductor sector's economic viability needs considerable scalability of power, speed, as well as area with each emerging technology node presented in two-year intervals. As IoT devices proliferate, they necessitate higher data transmission rates, storage systems, and retention, as well as instant access to cloud servers for data retrieval. As a result, the need for relatively small, efficient, and ultra-low-power semiconductor devices will tend to develop for at least another decade.

# 1

# Classical MOSFET Evolution: Foundations and Advantages

**S. Amir Ghoreishi[1]* and Samira Pahlavani[2]**

*[1]Department of Materials Science and Engineering, Arizona State University, Tempe, AZ, USA*
*[2]Electrical and Computer Engineering Department, Semnan University, Semnan, Iran*

***Abstract***

The realm of MOSFET innovations within the dynamic landscape of semiconductor technology is explored in this chapter. The complexities of these technological marvels through pioneering designs like nanosheet field-effect transistor (FET), negative-capacitance (NC) FET, junction less metal-oxide-semiconductor FET (MOSFET), NC tunnel FET (TFET), tunnel FET, Fe MOSFET gate-all-around (GAA), and various others are uncovered. The aim is to provide an understanding of these transistors, showcasing their attributes and applications. Junction less MOSFETs, a development in semiconductor technology, are started with. The principles, characteristics, and advancements of these innovations are delved, illustrating how they have redefined the landscape of device design. Next, TFETs, where tunneling phenomena are used for low-power operations, are examined. The workings of TFETs and their potential in electronics are uncovered. Nanosheet FETs and nanowire FETs, as well as nanoscale wonders, are then investigated. Their features, including their control over current flow, leading to enhanced performance, are studied. The short-channel effect in nanoscale transistors and strategies to mitigate it are also addressed. FinFETs, known for their three-dimensional structure, are focused on. Their principles and their role in semiconductor technology, especially in computing applications, are learned. GAA FETs are scrutinized, dissecting their architecture and their contributions to performance and efficiency. The landscape of these modern FETs is navigated, highlighting their design, characteristics, and applicability in electronics. This exploration, including insights into nanoscale transistors and the short-channel effect, serves as a resource for engineers, researchers, and enthusiasts seeking to harness these devices. By the end, the principles of these transistors and their role in electronic technologies will be understood by readers.

***Keywords*:** Field-effect transistors, short-channel effect, FinFETs, classical MOSFET, dual-gate MOSFET

## 1.1 Introduction of Classical MOSFET

Julius Edgar Lilienfeld laid the foundation for the concept of MOSFET fabrication in 1926 [1], suggesting a three-electrode structure using copper-sulfide semiconductor material.

**Corresponding author*: sghorei1@asu.edu

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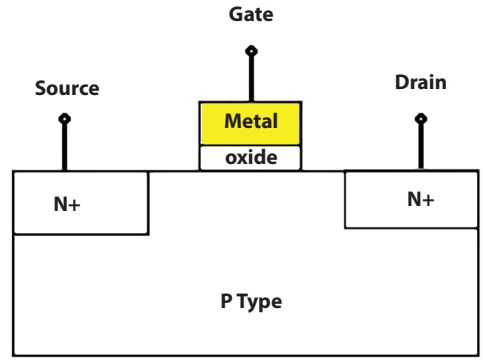


**Figure 1.1** A simple structure of a MOSFET.

While Lilienfeld's exploration sparked the idea of a new transistor type, the MOSFET, as we know it today, the concept was introduced by William Shockley, John Bardeen, and Walter Houser Brattain. The defect of this structure was the traps located on the surface of the semiconductor, which interfered with the mobility of electrons. Growing a layer of silicon dioxide on silicon wafer surface was the solution which Carl Frosch and L. Derick accidentally achieved in 1955. This layer acts as an insulator, preventing the diffusion of dopants into the silicon wafer. According to this achievement other scientists such as M. Atalla demonstrated that silicon dioxide plays a key role in solving the surface problems of wafers [2].

Special crystal clear, the metal-oxide-semiconductor field-effect transistors (MOSFETs) because of their special specifics and high performance not only have revolutionized in the electronic world but also have opened a new window in modern technology to engineers. They are the prevalent type of field-effect transistor (FET), used widespread in electrical devices ranging from memory to smartphone. MOSFETs are widely applied in both analog and digital circuits and are considered the most vital component of integrated circuits. They may be viewed as electronic switches and amplifiers, wherein the flow of current between the source and drain terminals is regulated by the voltage applied to the gate terminal. Figure 1.1 demonstrates a basic structure of classic MOSFETs. They consist of three terminals, entitled gate, drain, and source.

### 1.1.1 The Advantages of MOSFET

There are a variety of advantages for MOSFETs that can be mentioned. The milestone of MOSFETs is their high speed and low power consumption when they act as a switch. Furthermore, they possess reasonable efficiency in high frequency. Today, because of growing usage of portable electrical devices like smartphones and laptops, demand for fabricating electronics devices with small scale has increased. Manufacturing in small dimension is another ability of MOSFETs, which paves the way for producing semiconductor chips with numerous numbers of them. In terms of thermal stability, a wide temperature range is defined for them to operate accurately. This characteristic is crucial.

## 1.2 Dual-Gate MOSFET

According to a number of previous research that have been conducted [3], the classical MOSFET represents some restrictions when its gate length is shrunk under 30 nm. Enormous investigations have been carried out to reduce this limitation, and new architectures have been proposed during recent years [4, 5]. The dual-gate (DG) transistors are the most popular devices that maintain their characteristics when their gate-length is 30 nm [6]. Dual-gate MOSFET is a kind of MOSFET, consisting of two gate terminals that are electrically isolated from each other. These gates are embedded one after other along channel length and affect current, flowing among drain and source, thus providing better electrostatic control on channel. The increasing demand for the supply of this useful semiconductor device has prompted many well-known producers to fabricate them, in which Motorola, NXP Semiconductors, and Hitachi are pioneers in the production of these state-of-art transistors. Figures 1.2 and 1.3 illustrate circuit symbol of P-channel and N-channel MOSFET along with device structure of DG MOSFET, respectively.

The DG MOSFET consists of a source, a drain, and two gates. These gates are separated from the channel by oxide layers, with a metal layer positioned above them. As a classical MOSSFET, carriers enter the devices from source and leave them from drain terminal. Additionally, the gate regulates the flow of carriers. Among the recent high-technology MOSFETs, this model is like the classical model. However, there are several differences between them. Firstly, the second gate fortifies their abilities for controlling the channel. Secondly, DG MOSFET has two work modes based on their gate's situation. When both

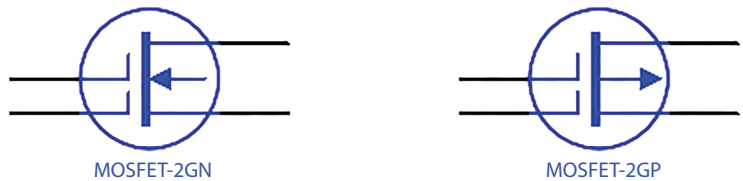


**Figure 1.2** Electronic symbol of DG MOSFET.

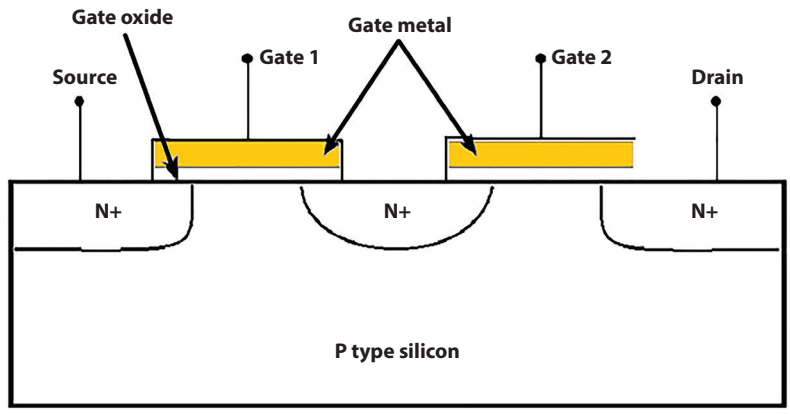


**Figure 1.3** Dual-gate MOSFET structure.

gates are activated, the DG MOSFET functions like a single-gate device. However, when only one gate is activated, the device operates in a mode referred to as "substrate biasing."

### 1.2.1 Advantage

Compared to the single-gate form, double-gate MOSFET has shown better performance in some electrical aspects.

#### *1.2.1.1 Scalability*

The most important factor preventing MOSFETs from scaling down is the short-channel effect. Because two gates control the channel and its current, this arrangement results in less short-channel effects, which provides greater flexibility for scaling and lower subthreshold current.

#### *1.2.1.2 Improvement of Gain*

In addition, the unique structure of DG MOSTFETs boosts the gain of them. The point is that, when they work in substrate biasing mode, situation that only one gate is on, turned-off gate creates depletion region. This region acts as a barrier against the device current flow to restrict it.

#### *1.2.1.3 Low-Power Consumption*

Another advantage of DG MOSFETs is consuming lower power. If a gate is off, then the channel length and gate leakage current will be reduced that contributes to power saving.

#### *1.2.1.4 Better $I_{ON}/I_{OFF}$*

Previous studies simulated their proposed models and reported that $I_{ON}/I_{OFF}$ is improved in DG MOSFETs [7].

#### *1.2.1.5 Higher Switching Speed*

The body of DG MOSFETs significantly decreases junction capacitances of drain and source. Hence, reducing the junction capacitance can enhance the switching speed of DG MOSFETs. Plus, the amount of feedback capacitance between the input and output of the devices can be significantly reduced by using the second control terminal.

### 1.2.2 Application

The characteristics of DG MOSFETs make them appropriate to be used in various applications, which will be mentioned.

### 1.2.2.1 RF Mixer

Radio frequency (RF) mixer consists of two inputs: local oscillator (LO) and RF. The DG MOSFET architecture fulfills the requirement of RF mixer as it has two inputs for the LO and RF signal. As demonstrated in Figure 1.4, commonly, gate 1 is allocated to RF signal, and the second signal is connected to gate 2. The channel current is regulated by two input signals, and the mixer generates a frequency based on its specific needs.

### 1.2.2.2 RF Amplifier

The most application of DG MOSFETs is in RF circuits especially in RF amplifiers. This type of transistors can operate efficiently at high frequency, due to elimination of unwanted capacitive and short-channel effects. Every single DG MOSFET has the ability to be converted to a two-stage amplifier, known as cascode structure. Figure 1.5 shows a conventional cascode circuit that comprises two separate MOSFETs. The input stage is a common-source amplifier, driven by an input signal source, Vin. The output signal Vout is connected to a common-gate amplifier that is the second stage, where the first stage is responsible for driving it.

A DG MOSFET can provide a cascode structure as it has two gates which G1 can play the role of stage where has common-source arrangement and G2 is the gate, connected to constant voltage and form a common-gate type. Therefore, by means of minimal components and power consuming, an amplifier can be designed that not only improves Miller effect by eliminating the capacitance existing between input and output but also occupies less space in circuits. A biasing for DG is depicted in Figure 1.6 to operate as a cascade amplifier.

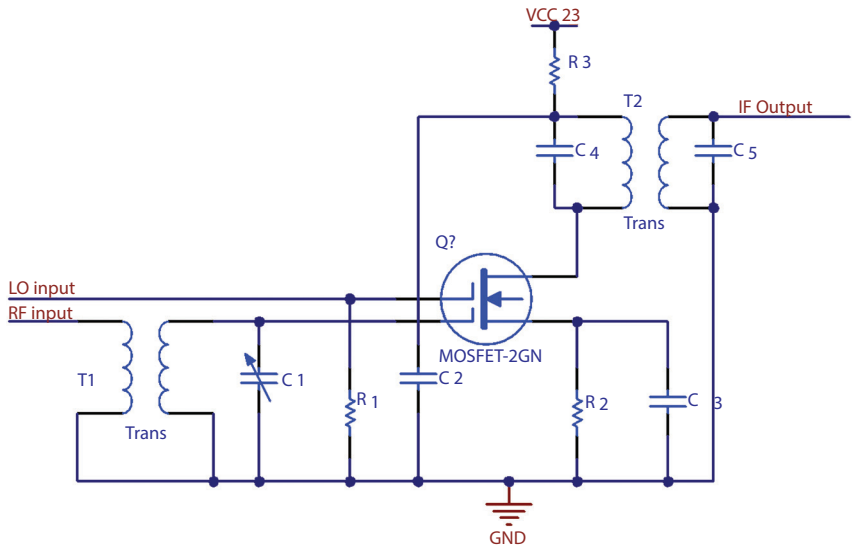


**Figure 1.4** A circuit of RF mixer.

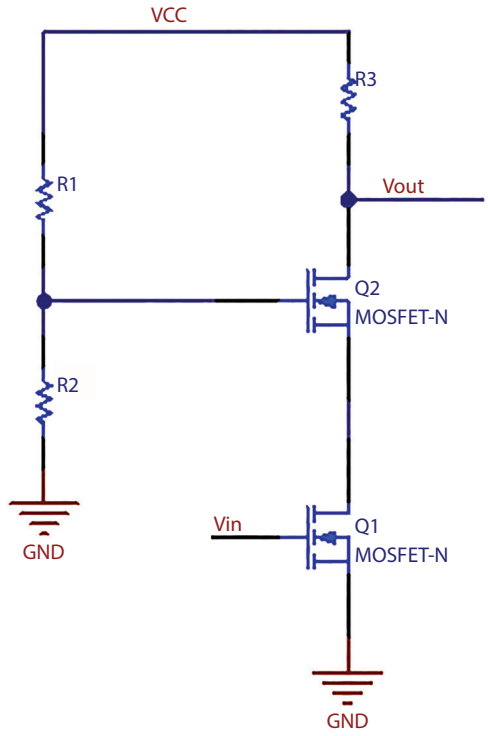


**Figure 1.5** Cascade circuit with two classical MOSFETs.

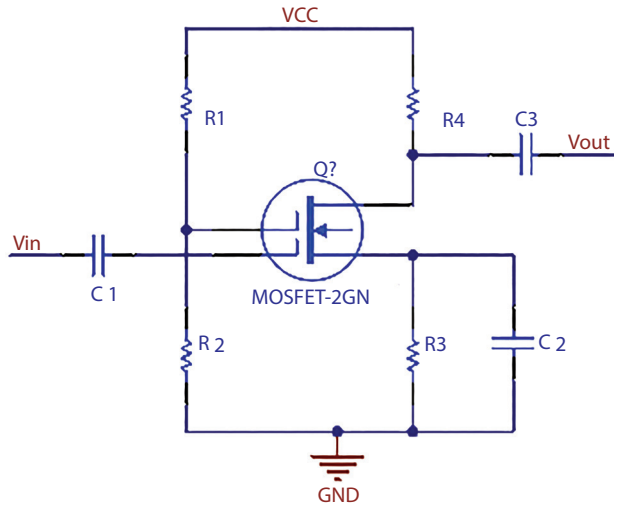


**Figure 1.6** Design a cascade construction by a dual-gate MOSFET.

### *1.2.2.3 Controllable Gain*

The output voltage of DG MOSFETs is depended to voltage level of both gates' terminal. To put it differently, if a constant voltage is considered for one of the gates, varying the voltage

on another gate terminal can affect output voltage. Indeed, a linear gain controller can be proposed by MOSFTEs, having two gates.

## 1.3 Gate-All-Around MOSFET

Over the past few decades, miniaturizing transistors has posed a significant challenge for electronics companies. They have competed with their peers to achieve a feasible solution. Accordingly, researchers are trying to figure out a structure with greater density, lower cost, higher performance, smaller dimension, and so on. However, when the length of channel varies, undesirable variations occur that should be considered. Research in this field resulted in a variety of promising schemes like multi-gate and gate-all-around FET.

Fujio Masuoka, a Japanese engineer, was a person who invented the first gate-all-around (GAA) MOSFET model that was showcased by Toshiba in 1988 [8]. GAA MOSFET, entitled "surrounding gate transistor" (SGT) is a semiconductor, surrounded by its own gate. The gate surrounds the channel on all four sides. It is a nanoscale silicon with a gate placed around it, which can have two or four effective gates. Small-scale design capability and compatibility with shorter channel length are the two main advantages of this feature, making it a strong competitor to overtake FinFets as it is expected to have better efficiency below 7 nm. In this structure, the gate has more contact with nanosheet or nanowire channel that leads to more control over the channel characteristics. Moreover, the controllable width of nanosheets in GAA FETs facilitates convenient adjustment of the device specifications [9].

Regarding manufacturing technology, nanowire and nanosheet structures have been introduced for the fabrication of GAA transistors. Because the nanowires offer better electrostatic control and nanosheets provide higher on current, they are more popular than other proposed architectures among semiconductor manufacturers [10].

### 1.3.1 The Fabrication Procedure of GAA MOSFETs

Nanosheets, known as foundation of GAA MOSFETs, should be formed first. For creating them, on the Si substrate, a stack of Si and SiGe epitax6ial layers should be alternatively grown. It is essential to be accurately checked the layers' thickness. In the next step, an inner dielectric spacer is eventually deposited in an indentation in the SiGe layers between source and drain, next to the pillar and the space where the gate will be. This spacer defines the gate width and the channel release and protects the drain and source regions. When the inner spacers are in place, a channel release etch eliminates the SiGe. Then, the gate dielectric and metal will be deposited into the spaces between the silicon nanosheets by atomic layer deposition (ALD).

### 1.3.2 Advantage of Gate-All-Around MOSFETs

#### *1.3.2.1 Excellent Performance*

Fabrication technology such as other fields of semiconductor industry is evolving. Although most companies have turned to FinFET technology, it seems that this trend has achieved its threshold. The point is that FinFETs cannot bear more scaling down and, when become

smaller, is not able to maintain their stability and specifics in many aspects. Reducing the control of both leakage current and short-channel effects, Finfet transistors' operation malfunctions. In this situation, GAA has shown its superiority by removing these defects and performing properly on the nanoscale.

#### *1.3.2.2 The Ability to Shrink*

The proposed methods for fabricating GAA MOSFET allow electronic devices producers to manufacture transistors with dimensions of 3 nm. Although their size can be reduced, the cost of production has not decreased.

#### *1.3.2.3 Adjustable Nanosheet*

Another benefit of GAA MOSFET is that their nanosheets width and number can be adjusted. This option serves more flexibility for electronic designers to alter the devices characteristics by varying the width of nanosheets and achieve their desired architect.

#### *1.3.2.4 Monitoring the Channel by Gate*

The exceptional performance of the GAA MOSFET can be attributed to the gate's effective management of the channel, creating a surround effect. This structure ensures precise control of leakage current and mitigates short-channel effects by achieving optimal channel dimensions and layout.

## 1.4 $I_D$-$V_G$ and $I_D$-$V_G$ Characteristics of Conventional MOSFETs

### 1.4.1 Introduction to $I_D$-$V_G$ Curves

The $I_D$-$V_D$ characteristics showcase the behavior of MOSFETs concerning variations in drain voltage while keeping the gate voltage constant. This relationship is crucial for understanding how MOSFETs operate under different operating conditions.

The $I_D$-$V_D$ curve of a MOSFET transistor exhibits two distinct regions: The transistor operates in two main regions: the linear region and the saturation region. In the linear region, the drain current ($I_D$) rises linearly with the drain-source voltage ($V_{DS}$) at a given gate voltage ($V_G$). On the other hand, the saturation region is characterized by the drain current ($I_D$) becoming independent of the drain-source voltage ($V_{DS}$) and reaching a maximum value for a given gate voltage ($V_G$).

The shift from the linear region to the saturation region happens when the drain-source voltage ($V_{DS}$) hits a crucial point known as the pinch-off voltage ($V_p$). This pinch-off voltage ($V_p$) equals the gate voltage ($V_G$) subtracted by the threshold voltage ($V_{th}$) of the MOSFET transistor. The threshold voltage ($V_{th}$) represents the minimum gate voltage ($V_G$) necessary to activate the MOSFET transistor.

Various factors can influence the $I_D$-$V_D$ curve of a MOSFET transistor, including channel length modulation (λ), drain-induced barrier lowering (DIBL), and velocity saturation (vsat).