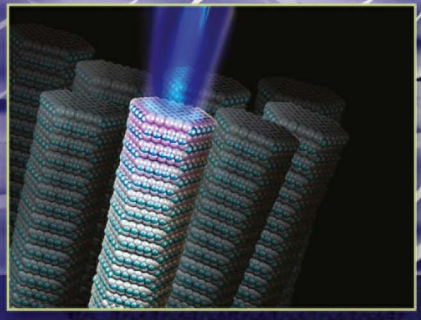
INTEGRATED DEVICES FOR ARTIFICIAL INTELLIGENCE AND VLSI

VLSI DESIGN, SIMULATION AND APPLICATIONS



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Preface

The current research trend in Integrated Semiconductor Devices for Artificial Intelligence and Very Large Scale Integration (VLSI) is exploring the potential of device and artificial intelligence for emerging engineering applications. In the current Integrated Circuits, switching time is on the order of nanoseconds, minimum feature size is on the order of nanometers, transistor count is on the order of billions and cost is on the order of a few dollars. Scaling of conventional MOSFETs towards smaller sizes is near to end because of limited mobility, large Short Channel Effects (SCEs), high leakage currents and power dissipation. To mitigate these challenges of conventional MOSFET devices and to scale the semiconductor device further into nanoscale domain, alternative materials and device structures are required. There are numerous challenges in the development of models for distributed intelligence systems for environmental monitoring, but these can be mitigated with artificial intelligence, machine learning, and deep learning. This book will help identify the areas where we encounter numerous challenges and apply diverse solutions for the development of advanced Integrated Devices for Artificial Intelligence and VLSI.

Chapter 1: The chapter 1 offers a thorough comparison of the two well-known transistor designs, MOSFET and FinFET, which have revolutionized integrated circuit architecture. The chapter offers a thorough investigation of the core ideas, design factors, and operational traits between the two transistor techniques. It describes the development of MOSFET technologies and how it has significantly advanced current electronics. The drawbacks of conventional MOSFET scaling are brought to light, necessitating the use of FinFET and other innovative transistor architectures. FinFET, revealing its ground-breaking design with a channel shaped like a fin and many gates. It examines the special operational benefits of FinFET, such as greater device scalability, improved electrostatic control, and lower leakage current. The article also looks at difficulties in designing and producing FinFETs, such as increasing process complexity and unpredictability. The outcomes of MOSFET and FinFET are compared and contrasted over a

number of important factors. These factors involve switching speed, noise immunity, power efficiency, power dissipation, leakage current, on-state current, subthreshold slope, threshold voltage control, and device scaling.

Chapter 2: Improvements in the VLSI industry have always been striving to justify the Moore's law by implanting, twice count transistors from the existing one. This law has made a significant improvement in the trends of FET family starting with the straightforward MOSFET with one gate controlling the channel, then next followed by FET with Dual gates, later Tri-gate/Fin FET and now persisting Gate-All-Around Field Effect Transistor. Each era of technology contributed its own advantages and disadvantages. Presently the Gate-All-Around FETs are ruling the FET industry because of its major advantage of improved gate electrostatic integrity over the channel from all the directions, with reduced overall size of the FET. In this research work, the vertically stacked GAA Nanosheet FET is simulated at the device-level using Visual TCAD – 3D Cogenda tool. Research is conducted to substantiate the influence of geometrical variations with respect to thickness and width on the performance of the FET. Parameters analyzed to in the research are ION, IOFF, Switching ratio (ION/IOFF), Subthreshold swing (SS), DIBL, and Threshold voltage (Vth). Device is optimal if it offers better ON current, minimum OFF current. To evaluate this optimal performance the thickness of the nanosheet (NT) is varied from 5nm to 9nm, and the width is varied from 10nm to 50nm. Visual TCAD - 3D Cogenda tool is used in analyzing the outputs generated and conclude the best geometric dimension for optimum characteristics.

Chapter 3: The standard MOSFET used in modern IC technology is expected to be replaced by new tunnel fieldeffect transistor (TFET), which is seen to be the utmost viable contender. Researchers have been very interested in it as a result of it's capacity to attain a steep sub-threshold slope, a stronger resilience to shortchannel effect's, and a reduced standby power dissipation. The current transport technique, band to band tunnelling (BTBT), causes TFET's two main bottlenecks, lower Ion current and ambipolar conductivity, despite the fact that it promises several benefits over other MOSFET competitors. This article provides a thorough overview of the many methods researchers have proposed to increase the ON-State current and subthreshold swing in Tunnel FETs.

Chapter 4: The unique characteristics of nanowire field effect transistors (NW FETs), such as high electron mobility, low power consumption, and scalability, have made them a promising technology for upcoming electronic devices. An overview of the underlying concepts, methods of fabrication, and performance traits of NW FETs are given in this chapter. The chapter discusses the benefits and drawbacks of NW FETs, including

how contact resistance, defect density, and surface effects affect device performance. The chapter also highlights the potential uses of NW FETs in several industries, including sensing, computing, and energy harvesting. Overall, this chapter offers a thorough reference for researchers and engineers interested in this innovative technology since NW FETs are anticipated to play a significant role in the creation of next-generation electronic devices.

Chapter 5: The Moore law for scaling of technological nodes has led to the major advancement in chip design and functionality. With the downscaling of technological nodes, the efficiency of gate becomes insignificant compared to the interconnect performance. The reliability issue play a major role at nano-scaled technological nodes since future interconnects requires higher current density with compact cross-sectional dimensions. Formerly, copper was employed as interconnect due to high current density and less resistivity but as technology downscales below 45nm its resistance increases due to the reduction of MFP. The scaling of interconnect dimensions effects the delay time as well as power dissipation. The electronics circuit operational speed is affected by the signal delay at the output of wire. The power dissipation is also a key factor in VLSI ICs. In today's world, everyone demands higher power standby and speed in electronic circuits. The motivation for minimizing delay in signal and power dissipation at global lengths for various technological nodes varies according to applications. The overall performance of electronic circuit depends on the product of power dissipation and delay. Both are independent parameters but to estimate actual performance of an interconnect their product must be taken into account for elite integrated circuits. This chapter has proposed MLGNR as suitable and alternative material in on-chip interconnects for future technological nodes compared to copper interconnects.

Chapter 6: We examine the recent development of ferroelectric memory, along with ferroelectric random access memory (FRAM). Sophisticated non-volatile memories including resistive random access memory (ReRAM), phase-change random access memory (PRAM), and magnetoresistive random access memory (MRAM) have all been expanded, but FRAM is the first of these to be commercially available. Currently, a few Mb of extremely dependable FRAM is accessible. FRAM has been used in sophisticated smartcards, RFID tags, and other electronic devices because of its superior electric features, which include fast read/write speeds around 50 ns, low power consumption, and high switching durability around 10^{13}. We also discuss recently created materials, manufacturing techniques, and circuit technologies that are anticipated to solve the scalability issue with FRAM.

Chapter 7: Very large-scale integration (VLSI) is the process of combining a large number of transistors on a single chip to form an integrated circuit. VLSI development is rapidly moving toward the efficient design of a single chip. However, VLSI design faces numerous challenges, including power optimization, design productivity, manufacturing variability and testability. Conventional methodologies are primarily manual, timeconsuming and resource-intensive. Artificial Intelligence (AI) and Machine Learning (ML) techniques, on the other hand, provide automated learning approaches for dealing with large amounts of data in complex chip design. Furthermore, incorporating machine learning algorithms can improve system-on-chip performance. AI/ML is becoming more important in VLSI design due to its numerous applications in both logical and physical design. As a result, AI/ML has become an essential component in the VLSI industry. This chapter discusses popular ML algorithms, their mathematical foundations, performance metrics, and how AI and ML applications can transform VLSI design by allowing for high-speed, intelligent and efficient implementations.

Chapter 8: A computing device is deemed rudimentary if its operational scope is confined to elementary high-school-level mathematical tasks. Conversely, a mechanism that incorporates components of biotic origin, like as DNA units, as opposed to conventional electrical elements, closely mirrors the intricacies of the human brain. The instantiation of a computation system that operates neurons and synapses in parallel, exhibiting high capacity and low power consumption, constitutes a neuromorphic computing system (NCS). Neurons communicate through the transmission of both chemical and electrical signals. A neural network is established through minuscule junctions, termed "synapses," where each neuron is intricately linked to others, facilitating signal propagation. Neuromorphic systems seamlessly integrate computing systems and memories, thereby mitigating the separation between them and overcoming the challenges associated with the "memory wall. This chapter provides an exhaustive perspective on neuromorphic computing, commencing with an examination of recent challenges in achieving effective computing systems capable of supporting diverse novel applications. Subsequently, device-level perspectives are scrutinized to enhance the efficacy of neuromorphic solutions. The comprehensive applications of neuromorphic computing are delineated to maximize exposure for research groups and the scientific community engaged in this field.

Chapter 9: Neuromorphic computing is a rapidly developing field that seeks to emulate the neural structure and function of the human brain using hardware and software technologies. In recent years, the

development of neuromorphic computing has been fueled by advancements in semiconductor technology and the need for more efficient and intelligent computing systems. This review chapter provides an overview of the state-of-the-art in neuromorphic computing, including the principles and concepts that underlie the technology, its key applications, and the challenges and opportunities that lie ahead. In this chapter discussion about the potential of neuromorphic computing to enable a wide range of applications, including sensory processing, robotics, machine learning, and cognitive computing. In this chapter discussions are made on some of the key challenges associated with the development of neuromorphic computing systems, including scalability, power consumption, and programming models. Overall, this review chapter provides a comprehensive overview of the current state of the art in neuromorphic computing and its potential impact on the future of computing and artificial intelligence.

Chapter 10: This chapter presents the production and characterization of a sol-gel composite nanoparticle composed of titanium dioxide (TiO_2) and zinc aluminate ($ZnAl_2O_4$)as a prototype microstrip patch antenna. Initially, the molecular composition was used with the chemical formula $xTiO_2(1\text{-}x)\ ZnAl_2O_4$ and defined as $0.08TiO_2$ for x = 8%. X-ray diffraction (XRD) was used to investigate the generated composite nanoparticles, which indicated the dominating peaks of $ZnAl_2O_4$ and TiO_2. The crystallite size of the nanoparticles was calculated to be 16.9 nm. Fourier transform infrared spectroscopy (FTIR), field-emission scanning electron microscopy (FESEM), and energy dispersive spectroscopy (EDS) were also used to evaluate the functional groups, shape, and elemental content of the composite nanoparticles.These nanoparticles were also used to fabricate a prototype patch antenna in order to test its performance. Finally, a fabricated patch antenna was suitable for the X-band applications with the operating frequency 8.49 GHz, return loss (RL) -19.97 dB and VSWR<2.

Chapter 11: Advances in the semiconductor era have increased the overall performance and capabilities of chipsets while reducing size and cost. Additionally, advances in AI frameworks and libraries are enabling more AI with less assistance on IoT devices at the edge. Sensors are essential in today's environment, providing seamless data for the development of new smart applications. An example is a smart home situation with many connected devices. In such a place, there is easy and fast access to web services and personal statistics, including calendar, notes, email, reminders, bank and more., users connect 0.33 Birthday Celebration talents or skills from the Amazon store to their smart speaker. In addition, smart home devices such as smart security cameras, video doorbells, smart stores, smart carbon monoxide video indicators and smart door locks have come

very close to smart homes. With smart speakers that add special requirements. Considering that the smart machine interacts with the products and devices used by the user account, every day people who own a physical device can use it. They have the most advanced technology available for smart speakers via voice commands. In this case, poverty, home security and other new aspects of the consumer suffer. Recently, Tensor Cam brought AI cameras, and Toshiba's Symbio and Facebook's Portal are smart speakers that support digital cameras and AI capabilities. Although they support cameras, they currently do not have an authentication process. This article discusses how smart speakers face cyber security risks due to the lack of authentication mechanisms, and discusses improvements to the modern, digital camera-enabled, microphone array-based Alexa smart speaker prototype.

Chapter 12: Recently, nanostructure-based drug delivery systems have become the center of attraction for researchers. In the last decade, various studies have revealed that fullerenes can be effectively utilized as carriers to transport various drugs to the affected cells. Thus, the potential application of borospherene (B_{40}) as a carrier for delivery of anti-cancer drug, 5-Fluorouracil, to prostate cancer cells is investigated using the density functional theory. To achieve targeted drug delivery, anisamide molecule is attached as ligand to the nano-carrier. It is deduced that the drug prefers to interact with the boron fullerene via its fluorine and oxygen atoms. The interaction of the drug and ligand at both the 6- and 7-membered rings of the borospherene is considered. The complex with ligand attached at the heptagonal ring and drug at the hexagonal ring is found to be the most stable with adsorption energy of -0.76eV. In order to get more insight, electronic properties viz. Density of states and Eigen states are also calculated for the most stable complex. This complex is found to be stable even in the aqueous medium. A pH stimulated drug release phenomenon is also proposed based on the knowledge that the cancer cells have lesser pH in comparison to the healthy cells. Thus, this study reveals that borospherene can be efficiently utilized as a potential nano-carrier for delivery of 5-Fluorouracil drug to prostate cancer cells.

Chapter 13: When a rectangular waveguide is in free space, the waveguide's characteristics and field distribution for different modes are computed using HFSS software. The analysis is performed for several parameters. The electric and magnetic field intensities, as well as the fundamental modal distributions, are investigated within a rectangular waveguide. Simulated analysis for the X-band is performed on a single size that has dimensions of 22.76, 10.15, 0.2, and 60 mm for breadth, width, wall thickness, and waveguide lengths. The performance of the rectangular

waveguide is examined together with characteristic profiles. The waveguide is simulated, and the outcomes are confirmed. An HFSS (High Frequency Structural Simulator) simulation platform is shown in the figure for the analysis of aperture radiation from a rectangular waveguide made of dielectric material or air.

1

Comparative Analysis of MOSFET and FinFET

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Abstract

The current chapter offers a thorough comparison of the two well-known transistor designs, MOSFET and FinFET, which have revolutionized integrated circuit architecture. The chapter offers a thorough investigation of the core ideas, design factors, and operational traits between the two transistor techniques. It describes the development of MOSFET technologies and how it has significantly advanced current electronics. The drawbacks of conventional MOSFET scaling are brought to light, necessitating the use of FinFET and other innovative transistor architectures. FinFET, revealing its ground-breaking design with a channel shaped like a fin and many gates. It examines the special operational benefits of FinFET, such as greater device scalability, improved electrostatic control, and lower leakage current. The article also looks at difficulties in designing and producing FinFETs, such as increasing process complexity and unpredictability. The outcomes of MOSFET and FinFET are compared and contrasted over a number of important factors. These factors involve switching speed, noise immunity, power efficiency, power dissipation, leakage current, on-state current, subthreshold slope, threshold voltage control, and device scaling.

***Keywords*:** FET, BJT, MOSFET, FinFET

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1.1 Introduction

Bipolar junction transistors (BJTs) have a significant problem with static power dissipation, which means that power is lost even when the circuit isn't switching. The vacuum tubes were replaced with BJT. A silicon component having three regions—emitter, base, and collector—the BJT was a current-controlled device. Before this, the current-controlled MOSFET was developed. A FET (field effect transistor) is so-called since the gate switches are switched on or off through the transistor with an electric field crossing the gate oxide, as opposed to a basic MOS transistor, which utilized metal as the gate material, SiO_2 as insulator, and semiconductor as the substrate [1–5]. The drain, gate, source, and body of a MOS transistor are its four terminals. NMOS and PMOS are two complementary architectures that may be used to describe MOS transistors. In overall, poly-silicon is utilized as the gate material and contains heavy n or p type doped materials. Silicon serves as the insulator, and donor dEffects are implanted on each side to provide the source and drain. If two regions are biased with distinct possibilities, the less potentially area will function as the source and the more significant potential area as the drain. The "insulated gate" MOS transistors that were previously employed in IGFETs or MOSFETs (metal oxide semiconductor field effect transistors) are no longer around. IGFETs and MOSFETs are voltage-controlled electronics with metal oxide layers separating the gates from the bodies. The input resistance is significantly increased by this layer. There is not any current passing through the gate because it is electronically insulated from the primary current-carrying channel joining the drain and the source [6–10].

1.1.1 Scaling Issue

The Moorey's law, which was first proposed by Gordon E. Moore Sr. in 1965, states that the total number of transistors in a chip shall double on an annual basis. Considering its low power dissipation, speed, packing density, efficiency cost proportion, advancement in computing innovations, and most importantly, scalability, CMOS has greater characteristics than other semiconductors [11–16]. Technological scaling refers to the shrinking of the transistor chip's horizontal and vertical widths as well as the supply voltage V_{dd} that minimizes power loss and prevents oxide breakdown. In this circumstance, the threshold voltage (Vt) is correspondingly decreased in order to equalize the transistor's outputs. Therefore, it is crucial for nanoscale design to minimize either dynamic or leakage power [17–22].

The difficulty was in coming up with methods to decrease both of these elements while extending the life of the cellular devices' batteries. Continuing scaling has caused the number of dopants to drop from thousands to just a few several dozen, which also lowers the doping's expensive cost in CMOS devices and gives us better operational densities. The most intriguing novel technologies that have been launched, such as double gate MOSFET, FinFET, and Carbon Nanotube Field Effect Transistor, can replace traditional CMOS semiconductors. Planar technologies had a scaling issue that was present in planar technologies beneath 32 nm, which led to the introduction of non-planar devices [23–28].

1.1.2 Problems in MOSFET

The MOSFET's channel length has a significant impact on how well it works. In contrast to short channel devices, long channel devices have a very long channel that connects the source and drain. The transistor densities on a single chip are increased by the low operational voltage requirements and fast processing rate of short channel MOS. Even with all these benefits, short channel devices have significant drawbacks [29–34]. A few of which are briefly discussed below:

i. **Leakage Current:** That is the unwanted flowing of current while the transistor is meant to run in its off state, is a problem that MOSFETs may encounter. Leakage current can result in wasted energy and decreased efficiency, especially in low-power applications because cutting down on energy use is crucial [35–37].
ii. **Subthreshold Leakage:** Whenever a MOSFET is functioning in the sub threshold zone, wherein the gate voltage is lower than the threshold voltage, sub threshold leakage relates to the tiny amount of current that passes through the device. In low-power applications wherein the transistor must be fully off to save power, sub threshold leakage might be troublesome [38–40].
iii. **Threshold Voltage Fluctuation:** Throughout production, processing differences cause MOSFETs to display threshold voltage fluctuation. The voltage that causes a transistor switches on or off is known as the threshold voltage. The efficiency and dependability of circuits can be negatively impacted by large fluctuations in threshold voltage, which can result in instability and probable failure [41–43].

iv. **Self-Heating:** As a MOSFET conducts current, heat is produced as a result of power loss within the channel. The MOSFET's temperatures may increase if its heat is not adequately drained, which might result in efficiency deterioration or possibly thermal runaway.
v. **Hot Carrier Effects**: Whenever MOSFETs run at high voltages, the carriers—electrons or holes—in the channel may acquire significant kinetic energy, which can result in collision against the silicon lattice. The performance of the gadget may eventually deteriorate as a result of these accidents damaging the channel [44–50].

1.2 Double Gate

A variation of the multigate transistor known as the double gate MOSFET (DG MOSFET) was created from the incredibly popular MOSFET technologies. In contrast to the typical MOSFET design, which only has one gate regulating the channel, DG MOSFETs have two gates. For nanoscale size transistors in very dense IC design, the DG MOSFET shows significant potential [6]. The DG MOSFET's fundamental design requires placing two gate contacts towards the top and bottom of the channel within an ultrathin body to enable efficient channel control via the two gates. Enhanced gate control improves drain to source current during the "ON" mode while preventing leakage current from flowing across the source and drain connections in the "OFF" mode. In this manner of lowering SCE, it also has a larger ON-OFF ratio than a typical MOSFET [7, 8]. Due to the employment of two gates to regulate the channel from each side, the DG MOSFET has better electrostatic properties than a Single Gate MOSFET (SG MOSFET). Larger switching signals arise from the two gates controlling nearly three times much current as a single gate. Each gate has the ability to regulate one device half, and each gate's function is totally distinct from each other. Since DG MOSFETs have double the current carrying capacity of planar CMOS, they can function at significantly lower inputs as well as threshold voltages. The DG MOSFET has a roughly two-times scaling benefit. The DG MOSFET has two gates that enable two different operating modes. Two configurations of DG MOSFET are possible: symmetrically driven double gate (SDDG) and independently driven double gate (IDDG). The bias of the gates is the primary distinction among both of them. Front and rear gates are coupled together when using SDDG method, but they get independent biasing in IDDG method [51–55]. The DG MOSFET idea

has been studied extensively various academics during the past ten years, particularly as a remedy for the very short channel length technology. The DG MOSFET has established itself as a transistor's forerunner. The development of the DG MOSFET has opened up a vast array of potential study areas. It additionally acts as the primary driver of our academic initiatives as we transition from the simple design of devices to their practical uses in the digital sector [56–62]. Therefore, adopting a DG MOSFET circuit to create a logic gate structure that is more effective and has better gate voltage control would be a step forward. The general block diagram of DG MOSFET is shown in Figure 1.1.

A double gate MOSFET is a type of MOSFET that has two gates instead of one. The schematic diagram of a double gate MOSFET is similar to that of a traditional MOSFET, but with an additional gate. The double gate MOSFET has a source and a drain, which are connected by a channel. The channel is made of a semiconductor material, such as silicon, and is covered by a thin insulating layer, typically made of oxide. This oxide layer is known as the gate oxide. In a double gate MOSFET, there are two gates: the front gate (also known as the control gate or the top gate) and the back gate (also known as the body gate or the bottom gate). Both gates are separated from the channel by a thin oxide layer. The front gate is the primary gate and controls the flow of current through the channel. It is connected to the input signal and is used to turn the MOSFET on and off. The back gate is used to control the threshold voltage of the MOSFET. The threshold voltage is the voltage at which the MOSFET starts to conduct current. By applying a voltage to the back gate, the threshold voltage can be adjusted, which can be used to optimize the MOSFET for specific applications [9–11]. The DG MOSFET is a more advanced version of the traditional MOSFET and has several advantages, including improved performance, lower power consumption, and better scalability. It is commonly used in high-performance

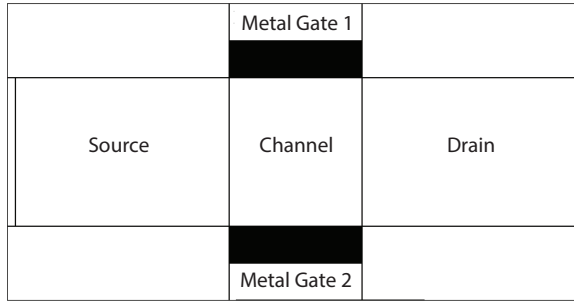

Figure 1.1 Double gate MOSFET.

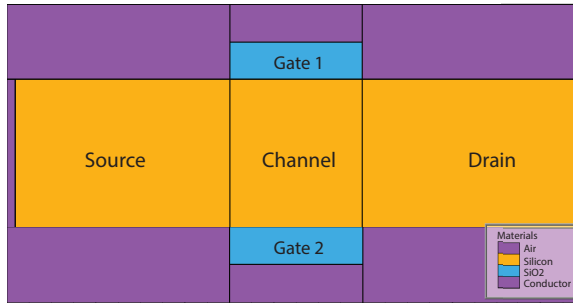

Figure 1.2 Schematic of double gate MOSFET.

electronics, such as microprocessors and memory chips, as well as in other applications that require low power consumption and high speed [63–68]. The Schematic of DG MOSFET is shown in Figure 1.2.

Because it establishes the fundamental doping characteristic of the semiconductor material, the acceptor concentration in a double gate MOSFET is typically constant across the substrate or channel area. The amount of doping in a material affects its conductivity as well as other electrical properties. In a MOSFET, neither the biasing conditions nor the applied voltage (V_{ds}) have a direct impact on the acceptor concentration [12]. It is a material characteristic that is established throughout the production processes and doesn't change until the doping profile is purposefully altered. It is important to keep in mind that the acceptor concentration might indirectly affect the efficiency and behavior of the double gate MOSFET, considering aspects such threshold voltage as well as sub threshold properties [69–72]. The acceptor concentration curve is shown in Figure 1.3 at different V_{gs}.

The electric potential of a double gate MOSFET is commonly shown across the source to the drain through the channel length. The supplied V_{ds}, gate voltages, and biasing circumstances all have an impact on the potential curve. The potential curve could display a somewhat straight drop throughout the channel length for a low V_{ds}, like 0.5 V. The potential would be stronger close to the source end and progressively decline as it moved nearer the drain side. Current flow is made possible by the potential gradient, which aids in drawing charge carriers (electrons or holes) from the source to the drain [13–15]. The potential curve might demonstrate a more pronounced decline throughout the channel length when V_{ds} rises to 1 V and 1.5 V. A steeper potential gradient is produced by the stronger electric field caused by the larger V_{ds}. Due to the drain voltage's ability to draw charge carriers, the potential at the drain side shall be lower than the source side. It is significant to consider that other elements, including as

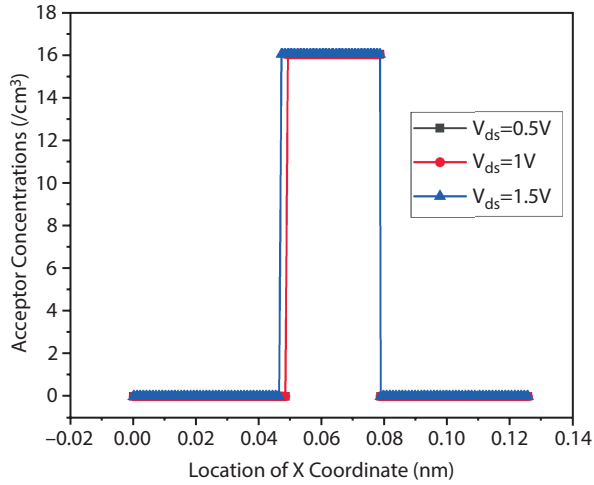

Figure 1.3 Acceptor concentration curve of DG MOSFET.

gate voltages, doping profiles, and device dimensions, may have an impact on the appearance and properties of the electric potential chart [73–77]. Additionally, the potential distributions in modern MOSFET architectures may be impacted by device scaling effects and technological improvements. Electric potential graph of DG MOSFET is shown in Figure 1.4.

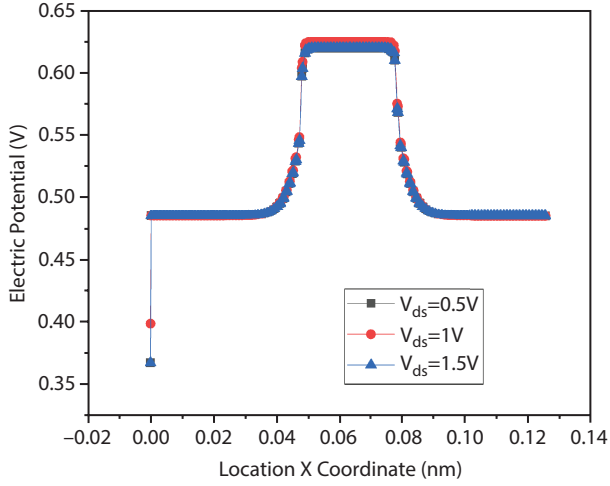

Figure 1.4 Electric potential graph of DG MOSFET at different V_{ds} = 0.5 V, 1 V, 1.5 V.

A double gate MOSFET's electric field curve will vary depending on the amount of V_{ds}, the device shape, the biasing setup, and the operational parameters. The electric field of a double gate MOSFET is commonly depicted across the source to the drain across the channel length. The gate voltages and the channel's potential profiles have an impact on the electric field distribution. The electric field variation might display a somewhat uniform distribution over the channel length at a low V_{ds}, such 0.5 V. The electric field would be comparatively small and consistent, both gates would be biased to regulate the channel area, and the transistor behavior would be good [16–20]. The electric field distributions may show more dramatic fluctuations when V_{ds} approaches 1 V and 1.5 V. The higher drain voltage might result in a greater electric field close to the drain side of the channel [78–83]. Larger electric field intensity might arise from this, might lead to hot carrier effects and deterioration of the transistor's efficiency. Scientists strive to reduce the peak electric field of a well-constructed double gate MOSFET to prevent reliability problems. To lessen the impacts of high electric fields, methods may be used including modifying the doping profile, enhancing channel length, and managing gate voltages. It's crucial to remember that a double gate MOSFET's exact electric field distribution might change depending on the device's size, the material's characteristics, and the biasing setup. Device designers frequently do thorough simulations and analyses to comprehend and optimize the behavior of the electric field in particular device architecture [21, 22]. Electric field graph of DG MOSFET is shown in Figure 1.5.

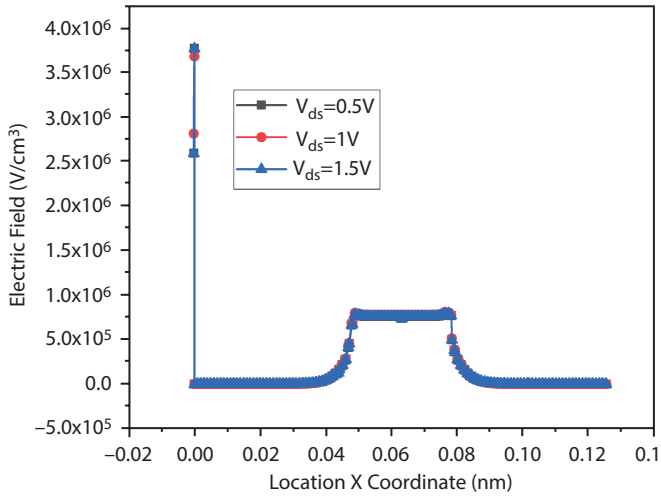

Figure 1.5 Electric field graph of DG MOSFET at different V_{ds} = 0.5 V, 1 V, 1.5 V.