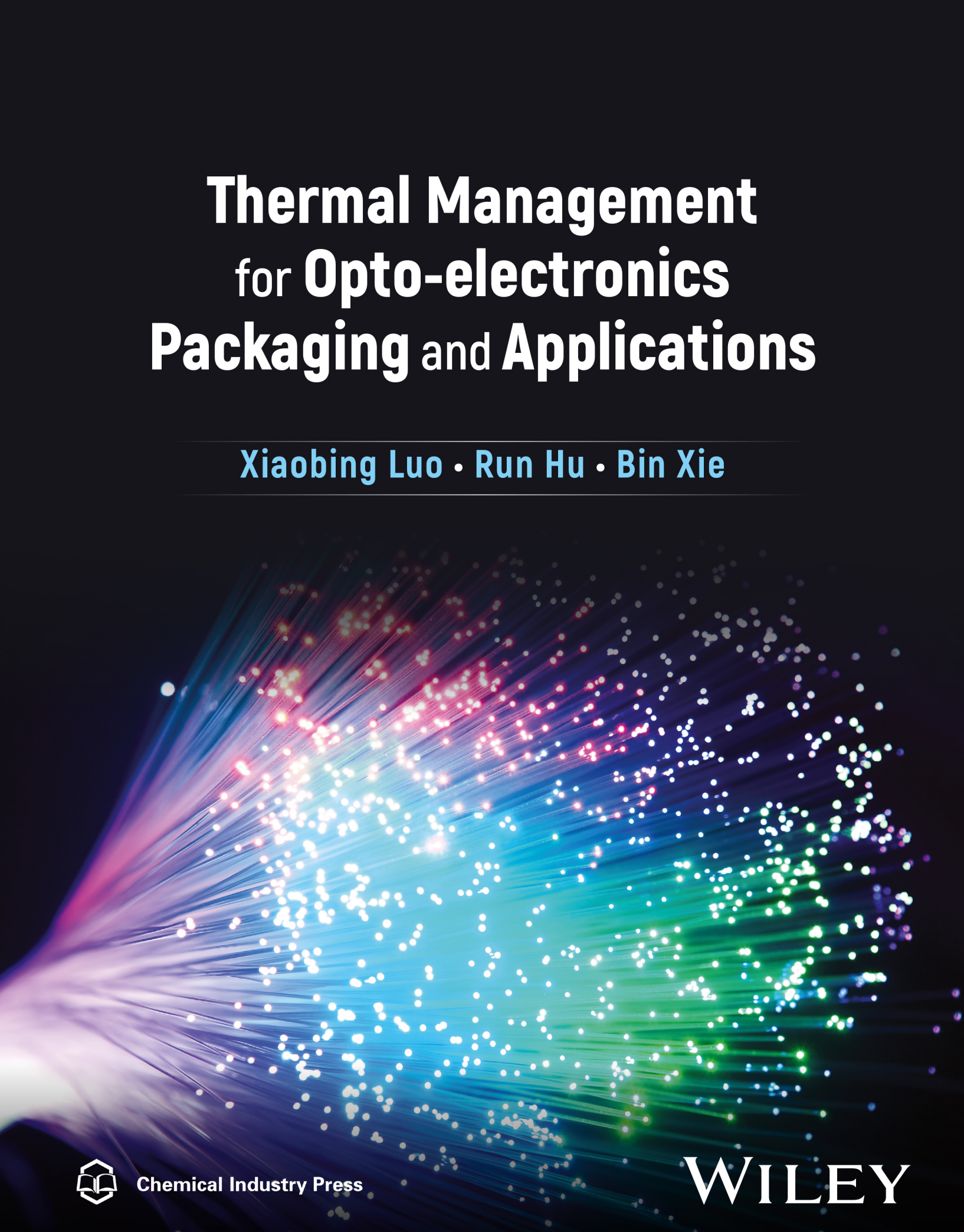
Thermal Management for Opto-electronics Packaging and Applications

Xiaobing Luo • Run Hu • Bin Xie



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Contents

List of Nomenclatures

Abbreviation

1D	one-dimensional
2D	two-dimensional
3D	three-dimensional
α-GaN	A-gallium nitride
β-Ga_2O_3	B-zirconia
AM	arrangement followed by mixing method
APG	alkyl polyglucoside
AW	atmospheric transparent window
BeO	beryllium oxide
BG	bilayer graphene
BGA	ball grid array
BLT	bond line thickness
BN	boron nitride
BW	bandwidth
CB	conduction band
CCT	correlated color temperature
CFD	computational fluid dynamics
CFs	carbon fibers
CH_2I_2	diiodomethane
CIE	Commission Internationale de L'Eclairage
CLTE	coefficient of linear thermal expansion
CMOS	complementary metal-oxide semiconductor
CMY	Cooper–Mikic–Yovanovich
CNC	computerized numerical control
CNT(s)	carbon nanotube(s)
Com-film	luminescent films containing without hBN
Com-WLEDs	common QDs-WLEDs without hBN
CPCMs	composite phase change materials
CRC	colored radiative cooler
CRI	color-rendering index
CS	crystal structure
CSF	cumulative structure function
CSP	chip-scale package
CTAB	hexadecyl trimethyl ammonium bromide
CTE	coefficients of thermal expansion
CTMS	centralized thermal management system
CVD	chemical vapor deposition
DA	diffusion approximation

DAA	die attach adhesive
DBC	direct bonded copper substrates
DC	dielectric constants
DIP	dual in-line package
DM	directly mixing without arrangement method
DMA	dynamic mechanical analysis
DPC	direct plate copper substrates
DQN	deep Q-learning network
DRL	deep reinforcement learning
DSC	differential scanning calorimetry
DTMS	distributed thermal management system
EBL	electron blocking layer
ECB	electrical conductivity bandwidth
EDS	energy dispersive spectroscopy
EG	expanded graphite
EGE	epsilon greedy exploration
EL	electroluminescence
EMA	effective medium approximation
EQE	external quantum efficiency
ER	electrical resistivity
FCP	flip chip package
FEA	finite-element analysis
FEM	finite-element model
FES	finite-element simulation
FLG	few-layers graphene
FRTE	an extension of RTE integrated with fluorescence
FWHM	full-width-at-half-maximum
GA	genetic algorithm
GNP	graphene nanoplatelets
GNs	graphene nanosheets
GO	graphene oxide
GP	graphene
HAADF-STEM	high-angle-annular-dark-field STEM
HBC	hybrid body cooling
hBN	hexagonal boron nitride
hBNPs	hexagonal boron nitride platelets
hBNS	hexagonal boron nitride sheets
HEC	hydroxyethyl cellulose
HG	Henyey–Greenstein
HP	heat pipe
HRTEM	high-resolution transmission electron microscope
HTHP	high-temperature and high-pressure
$I_{AM1.5}$	the standard AM 1.5 spectrum of solar radiation
IC(s)	integrated circuit(s)
IGBT(s)	insulated gate bipolar transistor(s)
iNEMI	international electronics manufacturing initiative
IQE	internal quantum efficiency
IR	infrared
Iso-film	luminescent films containing with isotropic distributed hBN
Iso-WLEDs	isotropic thermal conductive QDs-WLEDs with isotropic arranging hBN
JAICIPM	jet array impingement cooling system with integrated piezoelectric micropump
JIBC	jet impingement body cooling

JISC	jet impingement surface cooling
KM	Kubelka–Munk
LDs	laser diodes
LE	luminous efficiency
LED(s)	light-emitting diode(s)
LEE	light extraction efficiency
LERP	laser-excited remote phosphor
LFA	laser flash analysis
$LiAlO_2$	lithium aluminate
LM	lattice mismatch
MA	mixing followed by arrangement
MBAM	modified Bruggeman asymmetric model
MCE	mixed cellulose esters
MCM	multi-chip module
MCPCB	metal core-printed circuit board
MD	molecular dynamics
MDM	metal–dielectric–metal
mhBN	magnetically responsive hBN
mhBN-silicone	Imhbn-silicone
m-MPMF	micro multiple piezoelectric magnetic fan
mohBN	modified hBN
MOSFET	metal-oxide-semiconductor field-effect transistor
MPP	mesophase pitch
MQW	multiple quantum well
MWT	maximal working temperature
NICFs	nickel-coated carbon fibers
PAN	polyacrylonitrile
PCB	printed circuit board
pc-LD	phosphor-converted laser diode
pc-LED	phosphor-converted light-emitting diode
PCM(s)	phase change material(s)
PDMS	polydimethylsiloxane
PEEK	poly-ether–ether–ketone
PET	photo-electro-thermal
PG	propylene glycol
PID	proportional–integral–derivative (controller)
PL	photoluminescence
PMMA	polymethyl methacrylate
PTMS	passive thermal management system
QDs	quantum dots
QDs-WLEDs	QDs-converted WLEDs
QE	quantum efficiency
QFP	quad flap package
QSNs	QDs-silica coated nanoparticles
QY	quantum yield
RC	radiative cooling
RDL	redistribution layer
RE	relative error
RMSE	root mean square error
RTDs	resistance temperature detectors
RTE	radiative transfer equation
SAM	self-assembled monolayer

SAM-CH3	alkanethiol type SAM
SAM-NH2	11-amino-1-undecanethiol hydrochloride
SCMC	sodium carboxymethyl cellulose
SEM	scanning electron microscope
SiC	carborundum
SILAR	successive ionic layer adsorption and reaction
SLA	stereolithography
SLG	single-layer graphene
SMD	Sauter mean diameter
SNTP	solid heat conduction, natural air convection, thermal radiation, and phase change processes
SOI	silicon-on-insulator
SP	solid heat conduction and phase change processes
SPD	spectral power distribution
SR	selective radiative cooling radiator
SRH	Shockley–Read–Hall
SSH	the sustainability of the image horizontal direction
SSV	the sustainability of the image in the vertical direction
STEM	scanning transmission electron microscope
TC	thermal camouflage
TCEE	thermal conductivity enhancement efficiency
TD	thermal diffusion coefficient
TEOS	tetraethyl orthosilicate
TES	thermal energy storage
TFFC	thin-film flip-chip
TG	thermal gravimetric analysis
TIM(s)	thermal interface material(s)
TIR	total internal reflection
TMA	thermal mechanical analysis
TmhBN-silicone	through-plane-aligned mhBN-silicone
TMM	transfer matrix method
TMR	thermal mismatch rate
TMS(s)	thermal management system(s)
TO	transistor outline
TOP	tri-*n*-octylphosphine
TRPL	time-resolved PL
TSOP	thin small outline package
TSV	through silicon via
UHMR	ultrahigh magnetic response
UV	ultraviolet
VB	valance band
VC	vapor chamber
VCHP	variable conductance heat pipe
Ver-film	luminescent films containing with vertical hBNSCMC templates
Ver-WLEDs	vertical thermal conductive QDs-WLEDs
V-ORI	orientation in the vertical direction
WLEDs	white light-emitting diodes
WRC	white-color radiative cooler
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
XRT	X-ray tomography
ZnO	zinc oxide

Nomenclature (Units of Measure)

$\mathrm{Rate}_{\mathrm{SRH}}$	recombination rate (s^{-1})
Eu	Euler number (–)
Gr	Grashof number (–)
Nu	Nusselt number (–)
Pe	Berkeley number (–)
Pr	Prandtl number (–)
Re	Reynolds number (–)
k_{SRH}	SRH recombination coefficient ($cm^6 \cdot s^{-1}$)
k_{auger}	the Auger recombination coefficient ($cm^6 \cdot s^{-1}$)
k_{rad}	the radiative recombination coefficient ($cm^6 \cdot s^{-1}$)
A	surface area (m^2)
A_{c}	cross-sectional area (m^2)
A_{r}	the radiative surface area (m^2)
n	carrier concentration (cm^{-3})
n_{c}	phosphor concentration ($g \cdot cm^{-3}$)
k_{f2}	constant coefficient 2 (–)
$\mathrm{Rate}_{\mathrm{auger}}$	the rate of Auger recombination (s^{-1})
k_{f1}	constant coefficient 1 (–)
P_{h}	heat transfer rate (W)
Q_{f}	flow rate ($ml \cdot min^{-1}$)
P_{rad}	the rate of thermal radiation energy (W)
e	electron charge (C)
q	heat flux density ($W \cdot m^{-2}$)
$\partial T/\partial x$	temperature gradient ($K \cdot W^{-1}$)
F	driving force (N)
R	resistance of the process ($K \cdot W^{-1}$)
R_{thermal}	thermal resistance ($K \cdot W^{-1}$)
R_{c}	contact resistance ($K \cdot W^{-1}$)
m_{t}	transfer amount (W)
m	mass (kg)
k_{f3}	constant coefficient 3 (–)
T_{j}	junction temperature (K)
T_{a}	ambient temperature (K)
$R_{\mathrm{c\text{-}TIMs}}$	thermal contacted resistance with TIMs ($K \cdot W^{-1}$)
R_{TIMs}	the bulk resistance of the TIMs ($K \cdot W^{-1}$)
R_{s}	thermal spreading resistance ($K \cdot W^{-1}$)
R_{cu}	total thermal resistance of the copper substrate ($K \cdot W^{-1}$)
C_{p}	constant pressure heat capacity ($J \cdot kg^{-1} \cdot K^{-1}$)
k_{wl}	coefficient determined by the materiel of surface and liquid
D_{h}	hydraulic diameter (m)
F_x	external force in x-direction (N)
F_y	external force in y-direction (N)
g	gravity ($m \cdot s^{-2}$)
h	convection heat transfer coefficient ($W \cdot m^{-2} \cdot K^{-1}$)
k_{P}	Planck's constant ($J \cdot s$)
h_{c}	stable heat transfer coefficient ($W \cdot m^{-2} \cdot K^{-1}$)
$h_{\mathrm{non\text{-}rad}}$	a non-radiative heat transfer coefficient that combines the effective conductive and convective heat exchange ($W \cdot m^{-2} \cdot K^{-1}$)
$h_{\mathrm{microchannel}}$	the heat transfer coefficient of the microchannel liquid cooling ($W \cdot m^{-2} \cdot K^{-1}$)

l	length (m)
l_{n}	nozzle length (m)
l_{p}	length of plate (m)
l_y	length in y-direction (m)
l_z	length in z-direction (m)
p	pressure (Pa)
k_{f4}	constant coefficient 4 (–)
k_{f5}	constant coefficient 5 (–)
k_{asp}	aspect ratio of a rectangular duct (–)
p_{in}	pressure of the entrance of the flow (Pa)
p_{out}	pressure of the exit of the flow (Pa)
p_{sw}	shear stress of the partial wall (Pa)
P_{in}	the total output optical power from LED
q_{c}	convection heat transfer density ($\mathrm{W \cdot m^{-2}}$)
q_{w}	heat transfer density between fluid and contacting solid ($\mathrm{W \cdot m^{-2}}$)
s_{v}	horizontal pipe spacing in the vertical flow direction (m)
s_{l}	horizontal pipe spacing in the longitudinal pipe spacing along the flow (m)
T_{f}	qualitative temperature of the fluid (K or °C)
T'_{f}	average temperature of the fluid at inlet (K or °C)
T''_{f}	average temperature of the fluid at outlet (K or °C)
T_{m}	qualitative temperature of the vapor (K or °C)
T_{s}	saturation temperature (K or °C)
T_{w}	temperature of the wall and the flow (K or °C)
T_{∞}	temperature of the flow (K or °C)
u_x	velocity in x-direction ($\mathrm{m \cdot s^{-1}}$)
$u_{x\mathrm{dim}}$	dimensionless velocity in x-direction (–)
u_y	velocity in y-direction ($\mathrm{m \cdot s^{-1}}$)
$u_{y\mathrm{dim}}$	dimensionless velocity ratio in y-direction (–)
x	coordinate x (m)
x_{dim}	dimensionless length in x-direction (–)
y	coordinate y (m)
y_{dim}	dimensionless length in y-direction (–)
p_{dim}	dimensionless pressure (–)
T_{Edim}	dimensionless excess temperature (–)
$\bigtriangledown T$	temperature difference (K or °C)
E_λ	the energy radiated per unit volume by a cavity of a blackbody in the wavelength interval λ to $\lambda + \Delta\lambda$ ($\Delta\lambda$ denotes an increment of wavelength) ($\mathrm{W \cdot m^{-3}}$)
c	the speed of light ($\mathrm{m \cdot s^{-1}}$)
k_{B}	the Boltzmann constant ($\mathrm{J \cdot K^{-1}}$)
T	temperature (K or °C)
$\mathrm{rew_t}$	the reward in Bellman equation (–)
r_{log}	radius of the logging tool (m)
$\mathrm{wei_{tar}}$	the weights of the target network (–)
$\mathrm{wei_{main}}$	the weights of the main network (–)
P_{cooling}	cooling power of the emitter (W)
P_{rad}	the power emitted from the emitter (W)
P_{atm}	the input power from the atmosphere absorbed by the emitter (W)
P_{solar}	the incident solar power (W)
$P_{\mathrm{cond+conv}}$	the power of the non-radiative heat transfer due to the conductive and convective (W)
T_{amb}	the temperature of the ambient air (K)
I_{BB}	the spectral radiance of a blackbody at temperature T and wavelength λ ($\mathrm{W \cdot m^{-1} \cdot sr^{-1}}$)

G	the total solar irradiance ($\mathrm{W \cdot m^{-2}}$)
T_{ste}	the steady temperature when the P_{cooling} is zero (K)
H	nozzle-to-surface distance (m)
k_{sro}	the spearman rank order correlation coefficients (–)
$k_{\mathrm{sro\_L}}$	the spearman rank order correlation coefficients of *Lightness* (–)
$k_{\mathrm{sro\_C}}$	the spearman rank order correlation coefficients of *Chroma* (–)
$k_{\mathrm{sro\_H}}$	the spearman rank order correlation coefficients of *Hue* (–)
J	the LED injection current density ($\mathrm{A \cdot m^{-2}}$)
q_{eff}	effective radiation ($\mathrm{W \cdot m^{-2}}$)
t	time (s)
$\mathrm{BE_c}$	the effective density of states at conduction band edge ($\mathrm{m^{-3}}$)
$\mathrm{BE_V}$	the effective density of states at valence band edge ($\mathrm{m^{-3}}$)
P_{opt}	the optical power (W)
P_{ele}	a constant input electrical power (W)
P_{heat}	the heat generation power within the LED (W)
k_{heat}	the heat-dissipation coefficient (–)
R_{hs}	the heat sink to ambient thermal resistance ($\mathrm{K \cdot W^{-1}}$)
R_{jc}	the junction-to-case thermal resistance ($\mathrm{K \cdot W^{-1}}$)
k_{rs}	the relative slope (–)
$\boldsymbol{n}_{\mathrm{w}}$	the unit inward normal vector at the substrate boundary ($z = 0$) (–)
n_{p}	the refractive index of the phosphor layer (–)
n_0	the refractive index of the air (–)
$\boldsymbol{\Omega}^m$	a specific angular direction with the superscript m (sr)
M	the total angular number (–)
I_{j}	the radiative intensity at solution node j ($\mathrm{W \cdot sr^{-1}}$)
I_{g}	the global approximation intensity ($\mathrm{W \cdot sr^{-1}}$)
N_{sol}	the total number of solution nodes (–)
P_{ph}	the phosphor heating power (W)
R_{ph}	the conductive thermal resistance of phosphor layer ($\mathrm{K \cdot W^{-1}}$)
R_{mir}	the conductive thermal resistance of mirror layer ($\mathrm{K \cdot W^{-1}}$)
R_{bond}	the conductive thermal resistance of bonding layer ($\mathrm{K \cdot W^{-1}}$)
R_{conv}	the convective thermal resistance between heat sink with the ambient ($\mathrm{K \cdot W^{-1}}$)
D_{ph}	the diameter of a circular phosphor plate (m)
D_{spot}	the diameter of a circular pump spot (m)
P_{limit}	the critical incident power (W)
R_{j}	thermal resistance at the joint ($\mathrm{K \cdot W^{-1}}$)
R_{b}	thermal boundary resistance ($\mathrm{K \cdot W^{-1}}$)
R_{bulk}	bulk resistance of TIM ($\mathrm{K \cdot W^{-1}}$)
G_{int}	interfacial thermal conductance ($\mathrm{K \cdot W^{-1}}$)
D/t	aspect ratio (–)
D	diameter (m)
D_{n}	nozzle diameter (m)
f	volume fraction (%)
T_{ave}	average temperature of heat source (K)
T_{max}	maximum temperature (K)
k_{Fit}	fitting parameters (–)
I	relative PL initial intensity (–)
$P_{\mathrm{heat\text{-}chip}}$	heat power of LED chip (W)
$P_{\mathrm{QDs/hBN\text{-}phosphor}}$	heat power of QDs/hBN-phosphor (W)
$P_{\mathrm{QDs\text{-}phosphor}}$	heat power of QDs-phosphor (W)

P_{el}	input electrical power of WLEDs package (W)
$P_{op.ref}$	optical power from WLEDs with only silicone (W)
$P_{op\text{-}Qs}$	optical power from WLEDs with QSNs and silicone (W)
$P_{op\text{-}to}$	optical power from the type I WLEDs (W)
$P_{op\text{-}tt}$	optical power from the type II WLEDs (W)
P_{QSNs}	heat power of QSNs (W)
$P_{phosphor}$	heat power of phosphor silicone gel (W)
$P_{QSNs/phosphor}$	heat power of QSNs/phosphor-silicone gel (W)
$P_{op\text{-}wq}$	optical power from WLEDs with QSNs and silicone
r	radius (m)
T_b	bottom temperature (K or °C)
T_t	top temperature (K or °C)
C_{eff}	equivalent heat capacity of PCM ($J \cdot kg^{-1} \cdot °C^{-1}$)
h_L	average convective heat transfer coefficient ($W \cdot m^{-2} \cdot K^{-1}$)
m_{PCM}	mass of PCMs (kg)
LH	total latent heat (J)
SH	total sensible heat (J)
r_h	radius of the wellbore wall (m)
T_0	initial temperature (K or °C)
T_e	final temperature (K or °C)
T_l	final phase change end temperature of PCM (K or °C)
$T_{s\text{-}ini}$	initial phase change temperature of PCM (K or °C)
D_s	Sauter mean diameter (m)
T_{sub}	substrate temperature (K or °C)
T_{sur}	surface temperature (K or °C)
ΔT_{uni}	temperature non-uniformity (K or °C)
$\overline{Q}''$	mean volumetric flow rate ($m^3 \cdot s^{-1} \cdot m^{-2}$)
Q_v	total volume flow rate ($m^3 \cdot s^{-1}$)
q_r	heat flux ratio (%)
w	frequency (Hz)
w_c	critical frequency (Hz)
dir^m	the direction cosine along z-direction (–)
f_{PCM}	volume fraction of liquid PCM (–)
Abs	absorptivity (–)
Abs_{emi}	the absorptivity of the emitter
DF	the discount factor (–)
LH_{liq}	latent heat of liquefaction ($J \cdot kg^{-1}$)
k_z	correction factor determined by the number of pipe rows (–)
k_β	correction factor determined by the impact angle (–)
Tran	transmissivity (–)
$Tran_{atm}$	the transmissivity of the atmosphere in the zenith direction
T_E	excess temperature (K or °C)
k_a	the absorption coefficient (mm^{-1})
k_s	the scattering coefficient (mm^{-1})
ORI	degrees of orientation (–)
u_m	average velocity of the pipe section ($m \cdot s^{-1}$)
u_∞	velocity of the flow ($m \cdot s^{-1}$)
u_i	in-plane-diffused velocity ($m \cdot s^{-1}$)
T_{hs}	the heat sink temperature (K or °C)
T_{ph}	the phosphor temperature (K or °C)
T_c	the critical temperature (K or °C)

L_{PCM}	the latent heat of PCM ($\mathrm{kJ \cdot kg^{-1}}$)
$\boldsymbol{u}$	the air velocity ($\mathrm{m \cdot s^{-1}}$)
C_{air}	specific heat capacity of air($\mathrm{J \cdot kg^{-1} \cdot K^{-1}}$)
Fg	the gravity (N)
J_i	the effective radiation of the surface i ($\mathrm{W \cdot m^{-2}}$)
G_i	the input radiation of the surface i ($\mathrm{W \cdot m^{-2}}$)
T_i	the temperature of the surface i (K)
q_i	the radiation heat transfer of surface i (W)
$k_{F_{ij}}$	the radiation angle coefficient from surface i to surface j (–)
A_i	surface area of surface i ($\mathrm{m^2}$)
A_j	surface area of surface j ($\mathrm{m^2}$)
d_{ij}	the distance between the surface i and the surface j (m)
$C_{\mathrm{PCM\text{-}S}}$	heat capacity of solid PCM ($\mathrm{J \cdot kg^{-1} \cdot {}^{\circ}C^{-1}}$)
$C_{\mathrm{PCM\text{-}L}}$	heat capacity of liquid PCM ($\mathrm{J \cdot kg^{-1} \cdot {}^{\circ}C^{-1}}$)
$V_{\mathrm{PCM\text{-}S}}$	the volume of the solid PCMs ($\mathrm{m^{-3}}$)
$V_{\mathrm{PCM\text{-}L}}$	the volume of the liquid PCMs ($\mathrm{m^{-3}}$)
u_{mud}	the velocity of the logging tool movement ($\mathrm{m \cdot s^{-1}}$)
l_{log}	the length of the logging tool (m)
$l_{\mathrm{insulator\ 1}}$	the length of insulator 1 (mm)
$l_{\mathrm{PCMs\ 1}}$	the length of PCMs 1 (mm)
$l_{\mathrm{PCMs\ 2}}$	the length of PCMs 2 (mm)
$l_{\mathrm{insulator\ 2}}$	the length of insulator 2 (mm)
$T_{\mathrm{heat\ source\ 1}}$	the temperature of heat source 1 (°C)
$T_{\mathrm{heat\ source\ 2}}$	the temperature of heat source 2 (°C)
N_{v}	the number of vertexes in the simplex (–)
X_i	the ith vertex (–)
X_{l}	the optimal vertex (–)
K_{VT}	the temperature rise rate ($\mathrm{{}^{\circ}C \cdot min^{-1}}$)
L_{comp}	the latent heat of CPCMs ($\mathrm{kJ \cdot kg^{-1}}$)
L_{para}	the latent heat of paraffin ($\mathrm{kJ \cdot kg^{-1}}$)
ΔM	weight loss ratio (–)
r_{β}	the Kapitza radius (m)
W_{SL}	thermodynamic parameter ($\mathrm{J \cdot m^2}$)
P_{thermal}	thermal power (W)
r_{p}	the radius of the circular microcontact point (m)
r_{t}	the radius of the heat flux tube (m)
R_{a}	the arithmetic mean deviation (m)
k_{sl}	the slope (–)
H_{a}	heights of asperity (m)
wid	width (m)
S	spacing between nozzles (m)
U	uncertainty (–)
T_{in}	the inlet temperature (K or °C)
T_{out}	the outlet temperature (K or °C)
T_{loc}	the local temperature of the surface (K or °C)
N_{top}	the number of nozzles of the top surface (–)
N_{front}	the number of nozzles of the front surface (–)
N_{right}	the number of nozzles of the right surface (–)
H_{ch}	channel height (m)
R_{fth}	effective fluid thermal resistance ($\mathrm{K \cdot W^{-1}}$)
R_{fconv}	fluid convection thermal resistance ($\mathrm{K \cdot W^{-1}}$)

R_{wcond}	conduction thermal resistance to the wall ($\mathrm{K \cdot W^{-1}}$)
R_{wconv}	wall conduction thermal resistance ($\mathrm{K \cdot W^{-1}}$)
$l_{\mathrm{chip}\text{-}x}$	the dimensions of the chip in x-direction (m)
$l_{\mathrm{chip}\text{-}y}$	the dimensions of the chip in y-direction (m)
$l_{\mathrm{chip}\text{-}z}$	the dimensions of the chip in z-direction (m)
$\mathrm{wid_{ch}}$	channel width (m)
$\mathrm{wid_{w}}$	channel wall width (m)
$P_{\mathrm{thermal\_sur}}$	thermal power of the surface (W)
N_x	the number of discrete mesh in x-direction (–)
N_y	the number of discrete mesh in y-direction (–)

Greek Letters

δ	thickness (m)
δ_{LED}	the thickness of LED active region (m)
δ_{ph}	the thickness of the phosphor plate (m)
δ_{b}	the thickness of boundary layer (m)
δ_{tb}	the thickness of thermal boundary layer (m)
δ_{r}	thickness ratio (–)
τ	time constant (s)
τ_1	stable PL lifetime (s)
Ω	the solid angle (sr)
θ	fiber orientation angle (deg)
θ_c	critical incident angle (deg)
θ'	emission angle (deg)
θ'_i	emission angle of the surface i (deg)
θ'_j	emission angle of the surface j (deg)
θ_{t}	the transmitted angle (deg)
θ_{c}	contact angle (deg)
α	thermal diffusivity ($\mathrm{m^2 \cdot s^{-1}}$)
α_{mud}	thermal diffusivity of the mud ($\mathrm{m^2 \cdot s^{-1}}$)
α_{T}	through-plane thermal diffusivity ($\mathrm{m^2 \cdot s^{-1}}$)
β	coefficient of cubical expansion (–)
Γ	surface energy (J)
μ	dynamic viscosity ($\mathrm{N \cdot s \cdot m^{-2}}$)
μ_{c}	dynamic viscosity of the coolant ($\mathrm{N \cdot s \cdot m^{-2}}$)
μ_{f}	dynamic viscosity of average fluid temperature ($\mathrm{N \cdot s \cdot m^{-2}}$)
μ_{l}	dynamic viscosity of the saturation liquid ($\mathrm{N \cdot s \cdot m^{-2}}$)
μ_{w}	dynamic viscosity of average wall temperature ($\mathrm{N \cdot s \cdot m^{-2}}$)
μ_{v}	dynamic viscosity of vapor ($\mathrm{N \cdot s \cdot m^{-2}}$)
μ_{K}	kinematic viscosity ($\mathrm{m^2 \cdot s^{-1}}$)
ρ	density ($\mathrm{kg \cdot m^{-3}}$)
ρ_{air}	density of the air ($\mathrm{kg \cdot m^{-3}}$)
ρ_0	density of the air initial density ($\mathrm{kg \cdot m^{-3}}$)
ρ_{PCM}	density of the PCM ($\mathrm{kg \cdot m^{-3}}$)
$\rho_{\mathrm{PCM\text{-}S}}$	density of the solid PCM ($\mathrm{kg \cdot m^{-3}}$)
$\rho_{\mathrm{PCM\text{-}L}}$	density of the liquid PCM ($\mathrm{kg \cdot m^{-3}}$)
ρ_{l}	density of the liquid ($\mathrm{kg \cdot m^{-3}}$)
ρ_{v}	density of the vapor ($\mathrm{kg \cdot m^{-3}}$)

ρ_{md}	microcontacts density (m^{-2})
σ	the Stefan–Boltzmann constant ($\mathrm{W}\cdot\mathrm{m}^{-2}\cdot\mathrm{K}^{-4}$)
σ_{g}	Gaussian distribution (–)
ζ_{s}	surface tension of the liquid ($\mathrm{N}\cdot\mathrm{m}^{-1}$)
ζ_{AW}	air–liquid surface tension ($\mathrm{J}\cdot\mathrm{m}^{2}$)
ε	emissivity (–)
$\varepsilon_{\mathrm{atm}}$	the emissivity of the atmosphere (–)
η_{qm}	the phosphor quantum efficiency (%)
η_{lum}	the luminous efficiency (%)
η_0	the rated efficiency at the temperature T_0 (%)
η_{EQ}	the external quantum efficiency (%)
η_{con}	the conversion efficiency (%)
η_{ex}	light extraction efficiency (%)
η_{inj}	electrical injection efficiency (%)
η_{IQ}	internal quantum efficiency (%)
η_{wp}	wall-plug efficiency (%)
γ	reflectivity (–)
γ_{m}	mirror reflectivity (–)
γ_{B}	the diffuse reflectivity at substrate surface for blue light (–)
γ_{Y}	the diffuse reflectivity at substrate surface for yellow light (–)
ω^{m}	the angular weight corresponding to the incident direction $\boldsymbol{\Omega}^{m}$ (%)
ω_{GN}	the mass fraction of GNs (%)
λ	wavelength (m)
$\Delta\lambda$	an increment of wavelength (m)
λ_{B}	the wavelength for excitation blue light (m)
λ_{Y}	the wavelength for emission yellow light (m)
φ	distribution function (–)
ξ	the pre-set value (–)
κ_{p}	reduced thermal conductivity (–)
κ	thermal conductivity ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
κ_{air}	air thermal conductivity ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
κ_{PCM}	thermal conductivity of PCM ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
$\kappa_{\mathrm{PCM\text{-}S}}$	thermal conductivity of solid PCM ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
$\kappa_{\mathrm{PCM\text{-}L}}$	thermal conductivity of liquid PCM ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
κ_{mud}	thermal conductivity of the mud ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
κ_{f}	fluid thermal conductivity ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
κ_{m}	thermal conductivity of matrix ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
κ_{T}	through-plane thermal conductivity ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
κ_{TIM}	thermal conductivity of TIM ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
κ_{v}	thermal conductivity of vapor ($\mathrm{W}\cdot\mathrm{m}^{-1}\cdot\mathrm{K}^{-1}$)
q_{vol}	volumetric heat generation in the solid ($\mathrm{W}\cdot\mathrm{m}^{-3}$)

About the Authors

Xiaobing Luo (Date of birth: April 3, 1974) is a professor, doctoral supervisor, recipient of the National Outstanding Youth Fund, IEEE Fellow, ASME Fellow, and leading talent in scientific and technological innovation under the National Ten Thousand Talents Plan. He enjoys special allowances from the State Council and is the Dean of the School of Energy and Power Engineering and the Chinese Dean of the China Europe Energy Institute at Huazhong University of Science and Technology (HUST). He received his PhD in 2002 from Tsinghua University, China. From 2002 to 2005, he worked at the Samsung Advanced Institute of Technology (SAIT) in Korea as a senior engineer and obtained the SAIT Best Researcher Award in 2003. In September 2005, he returned to China and became an associate professor. In November 2007, he became a full professor after an exceptional promotion. He obtained the 2020 Baosteel Excellent Teacher Special Award, the second prize of the 2018 National Teaching Achievement Award (ranked second), the 2016 IEEE CPMT Outstanding Technical Achievement Award, the second prize of the 2016 National Technology Invention Award (ranked second), and the first prize of the 2015 Hubei Provincial Natural Science Award. He served as the Associate Editor for IEEE Packaging and ASME Electronic Packaging, respectively. In 2019 and 2018, he served as the Vice General Chair for the ASME InterPACK Conference in Silicon Valley, USA. As the first or corresponding author, he has published 176 SCI-indexed papers and authorized 56 Chinese invention patents and 5 US patents, of which 20 have been transferred in cash.

Run Hu (Date of birth: September 6, 1987) is a professor and doctoral supervisor at the School of Energy and Power Engineering, Huazhong University of Science and Technology. He received his bachelor and PhD degrees in 2010 and 2015, respectively, from HUST. He then joined the faculty in the School of Energy and Power Engineering. From November 2014 to March 2015, he worked at Purdue University, United States, as a visiting scholar. From November 2016 to November 2017, he worked at the University of Tokyo, Japan, as a JSPS postdoctoral fellow. In 2017 and 2023, he got promoted to associate professor and full professor, respectively. He was the recipient of Outstanding Youth Scholar and Chutian Scholar in Hubei Province. He served as the youth editor for several journals like Research. As the first or corresponding author, he has published more than 90 SCI-index papers and granted 20 Chinese invention patents.

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Preface

Date back to 2002 when the first author Xiaobing Luo graduated from Tsinghua University and began to work at Samsung Electronics Co. Ltd. in Suwon, Korea, he realized the importance of thermal management for electronics and devoted himself to the development of advanced thermal management solutions for integrated circuits (ICs), power electronics, microelectromechanical systems, etc. Three years later, although he had gotten promoted to senior engineer at Samsung, he resolutely and determinedly returned to China and joined the faculty at the School of Energy and Power Engineering at Huazhong University of Science and Technology, where he had spent his undergraduate and postgraduate periods from 1991 to 1998. Since then, he has established the Thermal Packaging Laboratory, which aims at developing advanced active/passive thermal management solutions for optoelectronics and electronics. He built a strong and fruitful collaboration with Prof. Sheng Liu from the School of Mechanical Engineering and Science and Wuhan National Laboratory for Optoelectronics at Huazhong University of Science and Technology and developed high-performance, high-power light-emitting diode (LED) packaging technologies, which perfectly solved the state-of-the-art optical, thermal, and mechanical challenges of high-power LED packages. Besides, he firmly believed that liquid cooling is the trend for active thermal management of power electronics, and the core of liquid cooling is the pump. Since 2008, he began to develop the miniature mechanical pump and successfully developed the prototypes of the hydraulic suspension pump, super-thin vortex pump, and piezoelectric pump, which have been granted many patents in China and the United States and transferred to companies for industrial commercialization. In 2010 and 2014, Run Hu and Bin Xie joined his group as PhD students and began to devote themselves to developing different kinds of thermal management solutions for optoelectronics and power electronics, such as high-power white-light LEDs, quantum-dot LEDs, insulated gate bipolar transistor (IGBT), IC packaging, and so on. In particular, they realized the importance of package-inside thermal management, which provides unique solutions for high-performance photoluminescent materials and optoelectronics. More importantly, due to increasing miniaturization of chips, devices, and power electronics, thermal management has become the bottleneck and attracts booming attention from both academic and industrial aspects, which is almost the common consensus across the world. So it is quite the right time to summarize what we did in the field of thermal management for optoelectronics and electronics. This book intends to assemble what we learned in the past years into a useful reference book for both the LED community and the IC packaging community, in the hope that the results to be presented will benefit engineers, researchers, and young students.

Therefore, this book's subject matter is thermal management for electronics, which can be a reference book for thermal engineers, mechanical engineers, packaging engineers, reliability engineers, and graduate students. This book covers the three basic ways for thermal management (i.e. thermal conduction, thermal convection, and thermal radiation) and the specific applications of these three ways for advanced thermal management in optoelectronics and power electronics. Moreover, this book will also demonstrate some specific applications, such as opto-thermal modeling, thermal interface materials, liquid cooling, packaging-in thermal dissipation, phase-change materials in downhole electronics, and so on. This book will not only present the specific applications but also provide fundamental research to satisfy the interests of active researchers.

There have already been five nice books about thermal management of electronics available to readers in English. They are *Thermal Management Handbook: For Electronic Assemblies* by Jerry Sergent and Al Krum in 1998; *Heat Transfer: Thermal Management of Electronics* by Younes Shabany in 2009; *Thermal Management for LED Applications* by Clemens J.M. Lasance and Andras Poppe in 2013; *The Art of Software Thermal Management for Embedded Systems* by Mark Benson in 2014; and *Thermal Management of Microelectronic Equipment* by Lian-Tuu Yeh in 2016. Moreover, there are some books on specific applications, such as lithium-ion batteries, electric vehicles, aircrafts, engines, heat pipes, LEDs, telecommunications equipment, power plants, data centers, and military applications. However, there is not such a book focusing on the

thermal management of opto-electronics from both fundamental analysis and application design aspects. In addition, there have been no books dedicated to package-inside thermal management and its corresponding applications.

All authors feel obligated to explore these subjects and contribute to the whole community through our recent findings to promote the healthy development of thermal management technologies for optoelectronics and power electronics. Chapter 1 provides an introduction of packaging, with an emphasis on thermal issues and challenges. Chapters 2–4 provide the fundamentals and development trends of thermal management solutions with respect to thermal conduction, convection, and radiation, respectively. Specifically, Chapter 2 will cover the introduction of different thermal materials, ranging from thermal conduction materials, thermal interfacial materials, heat pipes, phase-change materials, and thermal metamaterials. Chapter 3 will introduce the air and liquid cooling technologies. Chapter 4 will introduce spectral and directional radiative cooling materials for electronics cooling. The upcoming chapters will begin to provide some specific examples, including the problems and their solutions. Chapter 5 focuses on the opto-thermal modeling of photoluminescent materials such as phosphors in silicone for light converters in white-light LEDs. Chapter 6 emphasizes on the thermally enhanced thermal interfacial materials, covering the modeling of thermal interfacial resistance and modulation of thermal conductivity. Chapter 7 is devoted to liquid cooling for high-heat-flux electronics, including jet impingement cooling, spray cooling, direct body cooling, and microchannel cooling. Chapter 8 tends to introduce the concept of package-inside thermal management for phosphors and quantum dots. Chapter 9 will provide a unique example of high-temperature thermal management for downhole electronics with distributed phase-change materials. We hope this book will be a valuable source of reference for all those who have been facing the challenging thermal problems created by the ever-expanding application. We also sincerely hope it will aid in stimulating further research and development on new thermal materials, analytical methods, testing and measurement methods, and even newer standards, with the goal of achieving a green environment and an eco-friendly energy-saving industry.

The organizations that know how to develop thermal management have the potential to make major advances in developing their own intellectual properties (IPs) in packaging and applications to achieve benefits in performance, cost, quality, and size/weight. It is our hope that the information presented in this book may assist in removing some of the barriers, avoiding unnecessary false starts, and accelerating the applications of these techniques. Developing thermal management solutions for opto-electronics packaging and applications may be limited only by the ingenuity and imagination of engineers, managers, and researchers.

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1

Introduction

1.1 Development History of Packaging

Since the invention of the first semiconductor transistor in 1947, the electronic industry has experienced rapid development following Moore's law in the past decades. Packaging plays a key role in the electronic industry: it integrates numerous packaging components (i.e., chip, solder, printed circuit board [PCB], encapsulant, and cooling device) together to form a full-featured electronic system. The rapid development of the electronic industry raises numerous requirements for packaging. On the one hand, packaging is moving toward high integration, high frequency, high power, and low cost. On the other hand, packaging is expected to be more energy efficient, environment-friendly, and sustainable. These requirements pose several challenges for packaging including material development, process innovation, electrical design, and thermal management.

Nowadays, a single-chip package contains most functions of an electronic system and chips are the core component of the package. However, bare chips are far from application due to several problems. First, chips should be connected with the external circuit by pin, bonding wire, or solder ball. Second, chips are very sensitive to external factors including external mechanical force, moisture, and dust. Therefore, the chips should be isolated from these external factors by encapsulation. Third, chips generate heat during operation, which raises the chip junction temperature. If, without excellent thermal management, the chip junction temperature reaches an extremely high value, this would cause serious efficiency drop, lifetime reduction, and even chip failure. These problems are becoming more serious due to the increasing requirement for high integration, high frequency, and high power. For electronic connection, high integration of chips results in dense pin, bonding wire, and solder joint. For chip isolation, to place more chips on a fixed-size circuit, the encapsulation should be more compact. For thermal management, the high integration and high power of chips result in extremely high heat flux, which requires advanced cooling technologies such as vapor chamber, microchannel, microjet cooling, and spraying cooling. The main function of packaging is to solve the three problems listed earlier. Therefore, packaging is also regarded as chip packaging. It not only plays an important role in placing, fixing, sealing, and protecting the chips but also connects the chips with the external circuits and provides thermal management for chips.

In the past decades, packaging has undergone rapid development. In general, the development of packaging can be divided into three stages. The first stage is the through-hole insertion technology before the 1980s. This technology inserts the chip pins directly into the through holes of PCB. Because the technology requires extremely high alignment of the pins and holes, it presents low packaging density and frequency. The second stage is the surface-mount technology that emerged in the mid-1980s. It mounts the chips on the PCB through tiny pins. Compared to the through-hole insertion technology, it enhances the electrical characteristics of chips and improves the automation degree of production significantly. Although this technology has advantages of high density, small pin spacing, low cost, and suitability for surface mounting, it still fails to meet the packaging requirements of some advanced electrical systems. The third stage is the ball grid array (BGA) and chip scale package (CSP) technologies after the 1990s. During this period, the electronic industry developed rapidly, so the previous packaging technologies no longer met the packaging requirements. In this situation, the BGA and CSP were developed. They utilize the solder balls as input/output (I/O) pins, which greatly increases the package density. The emergence of BGA and CSP led to the explosive growth of the electronic industry.

Thermal Management for Opto-electronics Packaging and Applications, First Edition. Xiaobing Luo, Run Hu, and Bin Xie.

During the development of packaging, a lot of packaging technologies have been developed, such as transistor outline (TO) package, dual in-line package (DIP), quad flat package (QFP), thin small outline package (TSOP), BGA, CSP, flip-chip package (FCP), multichip module (MCM), and 3D packaging. From TO to 3D packaging, the technical indicators of packaging have greatly improved, such as closer chip area to package area ratio, higher integrating density, better thermal management, denser pins, closer pin spacing, smaller weight, and higher reliability. As the packaging requirements increase, some packaging technologies have been gradually eliminated. However, some advanced packaging technologies have been used until today, such as BGA, CSP, MCM, and 3D packaging, which will be introduced in the following text.

1.1.1 BGA

With the development of electronic industry, the number of I/O pins and power consumption of chips increase dramatically. Therefore, the traditional QFP and TSOP technologies can no longer meet the packaging demand. To solve this problem, the BGA packaging technology was developed in 1998. It synthesizes solder balls at the bottom of the package and uses them as I/O pins to connect with the PCB. Compared to the QFP and TSOP, it has many advantages:

① Dense I/O pins but larger pin pitch, which improves the assembly yield greatly.
② Good electrical and thermal performance.
③ Small size. Compared to the QFP, its thickness is reduced by more than 1/2 and its weight is reduced by more than 3/4. Compared to the TSOP, its packaging size is reduced by more than 2/3.
④ Small signal transmission delay and higher frequency.
⑤ High reliability.

Attributing to these advantages, it became the best choice for high-density, high-performance, multifunction, and high I/O pins packaging as soon as it was invented.

1.1.2 CSP

Although the rise and development of BGA solved the difficulties faced by QFP and TSOP, it still occupies a large substrate area. In order to integrate more chips on a fixed-size PCB, the CSP was invented in 1994. The perimeter of a CSP is no more than 1.2 times the perimeter of the chip it contains, thereby allowing more chips to be arranged in the same area and reducing the overall electrical system significantly. The structure of the CSP is similar to that of the BGA with smaller solder balls and ball spacing, so that more I/O pins can be arranged at the same size package. Compared to the prior packaging technologies, the CSP has several advantages:

① Small size and low weight. The size and weight of the CSP are smaller than any other packages. For packages with the same I/O number, the CSP technology reduces the weight of the package by more than 4/5 and the size of the package by 2/3–9/10, when compared with the QFP.
② Large number of I/O pins. For same size package, the number of I/O pins of the CSP is ~3 times that of QFP and ~1.5 times that of the BGA package.
③ Good electrical performance. The interconnection length of the CSP between the chip and the package shell is much shorter than that of QFP and BGA packages, so it has lower signal transmission delay and higher frequency.
④ Good thermal performance. Because the thickness of the CSP is extremely less, the heat generated by the chips can be easily transferred to the outside of the packaging.

Although the CSP technology was invented more than 20 years ago, it is still in the early development stage and many problems remain to be solved, such as the packaging standard and I/O pins alignment. It is undeniable that the CSP will be one of the mainstream packaging technologies in the future.

1.1.3 MCM

The rapid development of electronic systems raises high demand for multifunction and multichip packaging technologies. However, the traditional packaging technologies only contain one chip in the package and integrate numerous packages on a PCB, which increases the system size and leads to low reliability and high signal transmission delay caused by the long interconnecting wire between the packages. To tackle this issue, the MCM packaging technology was developed.

It integrates two or more large-scale chips together in one packaging shell, so the signal transmission delay between the chips is reduced greatly due to the tiny chip spacing. The MCM has many advantages:

① Low signal transmission delay and high signal transmission speed. Compared to the single-chip package, the MCM increases transmission speed by 4–6 times.

② Compact size and low weight. The chips in the MCM package can be tiled on a single layer or stacked on multiple layers. The multiple-layer structure can decrease the packaging size significantly, resulting in low weight. Compared to the single-chip packaging, it decreases the weight by more than 80%.

③ High reliability. The failure of the electronic systems is mainly caused by failure of circuit interconnections, while the MCM reduces such interconnections, thereby improving the reliability of the electronic system.

④ Multiple functions. The MCM integrates chips with various functions together to form multifunctional electronic systems directly.

Although the MCM has many advantages, it is not as widely applied in industrial production as the BGA and CSP technologies. There are two reasons: the cost of the MCM is much higher than other packaging technologies and the MCM package presents poor thermal performance because the heat cannot be quickly dissipated to the outside due to the high chip integration along the vertical direction. For most commercial electronic systems, the BGA and CSP technologies would be a better choice due to their relatively low cost.

1.1.4 3D Packaging

In recent years, the development of the electronic industry has failed to obey Moore's law, which predicts that the number of transistors on a chip will double every 24 months, due to the physical limitations present in the complementary metal-oxide semiconductor (CMOS) processing technology. The 3D packaging is expected to break this limitation. By stacking more than two chips in the vertical direction through silicon via (TSV), the 3D packaging assembles more chips on the electronic system without increasing the size of the PCB. Compared to the 2D packaging, it has advantages of higher assembly density, lower cost, smaller size, lower power consumption, higher signal transmission speed, and smaller signal transmission delay. So far, the 3D packaging is rarely applied in the industrial production because there are many problems that need to be solved, such as the cost and reliability of the TSV and redistribution layer (RDL) and the severe thermal issue caused by the high chip integration along the vertical direction.

From the TO in the 1970s to the current 3D packaging, packaging technology has undergone tremendous development in materials, processes, and applications. With the further development of the electronic industry, more changes are taking place in the field of packaging.

① High thermal conductivity packaging materials. The low thermal conductivity of some key packaging materials, i.e., thermal interface material (TIM), encapsulant, and chip substrate, has become a serious problem that blocks further development of high integration and power electronic systems. For the TIM and encapsulant, the scholars and industry are trying to enhance their thermal conductivity by adding high thermal conductivity particles, such as graphene nanoplatelets (GNP), carbon nanotube (CNT), hexagonal boron nitride (hBN), and metallic oxide. And the concentration and arrangement of the particles are optimized by considering the material properties of the liquid matrix and particles. For the chip substrate, high thermal conductivity materials, i.e., silicon (Si), silicon carbide (SiC), aluminum nitride (AlN), beryllium oxide (BeO), and diamond, are developed to replace the conventional sapphire (Al_2O_3).

② Advanced cooling technologies. For some electronic systems with high chip power and integration, the local heat flux could reach an extremely high level $>500\,W\,cm^{-2}$, which requires advanced cooling technologies to dissipate the heat immediately. Therefore, conventional air cooling technologies can no longer meet the cooling requirement. To solve this issue, liquid cooling technologies with microchannel, vapor chamber, and phase change materials have been developed.

③ Environmental packaging material. To protect the environment, it is meaningful to use lead-free, halogen-free, and easy-clean packaging materials. In recent years, the use of lead-free solders has been attracting extensive attention. However, most of the lead-free solders have relatively high melting point and poor wettability, which results in voids in the solder layer and thereby worsens the reliability of the electronic devices. Therefore, it is very important to develop lead-free solders with a low melting point and good wettability. Besides, the conductive adhesive could also be a prior choice.

④ Reliability of the electronic systems. Most chips are sensitive to moisture, oxide, and high temperature environment. Therefore, it is of great importance to investigate the effect of these factors on the reliability of electronic systems and enhance the reliability by developing advanced packaging technologies.

1.2 Heat Generation in Opto-electronic Package

In general, the chips can be regarded as resistors, and the heat power of the chips is proportional to the driven current and equal to the input electrical power in most cases. However, for some electronic packages with opto-electro chips, only part of the input electrical power is converted into heat and the heat generation mechanism can be extremely complex. The accumulation of heat increases the chip junction temperature sharply and induces many thermal problems including thermal stress, performance degradation of the chip, and mechanical and electrical reliability of the package. The opto-electro packages have undergone rapid development in recent decades due to their wide application in solid-state lighting. Therefore, it is of importance to understand the heat generation mechanism of the opto-electro chips.

Light-emitting diode (LED) is a typical opto-electro chip, so we use it as an example in the following text to make the description clearer. The LED was invented by Holonyak and Bevacqua in 1962 [1], and widely applied to general lighting until Nakamura et al. [2] invented blue LED chips with high power and light efficiency in 1991. As a typical type of solid-state lighting, LED converts part of the input electrical power into light power. Compared to the conventional lighting sources (i.e., incandescent lamp and fluorescent lamp), it has the advantages of high light efficiency (>100 $\mathrm{lm \cdot W^{-1}}$), long lifetime (>50,000 hours), high reliability, compact size, and environmental protection. Therefore, it has become the mainstream light source in the twenty-first century [3, 4].

Figure 1.1 shows the working principle of LED. The core functional structure of the LED chip is the PN junction that is composed of P-type semiconductor and N-type semiconductor. In P-type semiconductor, the carriers that transport electrical energy are holes, while in N-type semiconductors, the carriers that transport electrical energy are electrons. Under the drive of an electric field, the electrons and holes move relatively and recombine in the multiquantum well (MQW) layer to emit light. In addition, part of the electrical power is converted into heat due to the nonradiative combination of electrons and holes, Shockley–Read–Hall (SRH) recombination, Auger recombination, surface recombination, current crowding and overflow, light absorption, etc.

1.2.1 Heat Generation Due to Nonradiative Recombination

Figure 1.2 shows the schematic of the band gap of the semiconductor material, which has an electronic band structure determined by the crystal properties of the material. The discrete energy distribution is affected by the absolute temperature. Above absolute zero temperature, the existing energy levels are filled with electrons according to the Boltzmann distribution. The free electrons range from their bounds to a freely moving state, which is called a conduction band (CB). The valance band (VB) is the highest range of electron energies in which electrons are bounded. The difference between CB and VB is called the band gap or forbidden band, since ideally there is no electron energy state within this region [5].

The freely moving electrons in the meta-stable state exist in the CB until they fall to the VB and recombine with an electron hole. This process is referred to as recombination. There are two types of recombination within the active region of LED chips, i.e., radiative recombination and nonradiative recombination. For radiative recombination, the electron fills a hole in the VB by releasing a photon with energy equal to the band gap energy of the semiconductor material [6]. This process is the

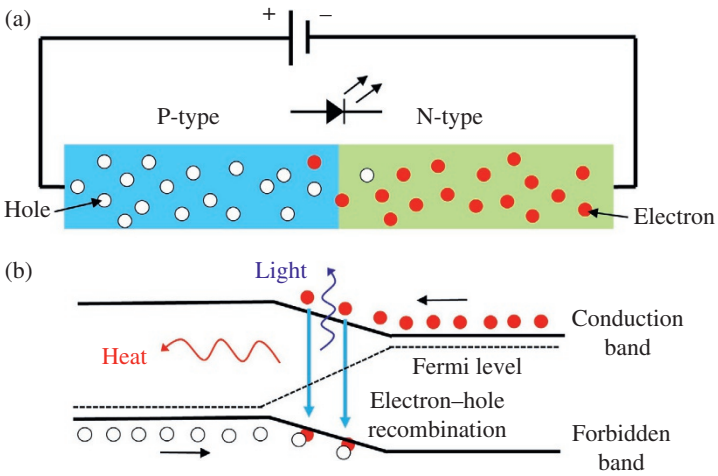

Figure 1.1 (a, b) Working principle of a typical LED chip.

foundation of the LED working mechanism. For nonradiative recombination, the releasing energy exists in the form of atom vibrations within the crystal, such as phonons; if the energy is not collected, it dissipates as heat. Apparently, the nonradiative recombination should be minimized for high device performance and low heat generation [7].

In the active layer of the LED chips, there are two major nonradiative recombination processes, i.e., defect-related SRH recombination and Auger recombination, which will be described in detail next.

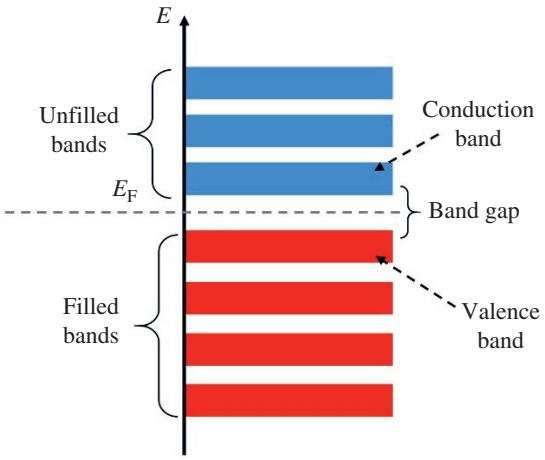

Figure 1.2 Schematic of the band gap of the semiconductor material.

1.2.2 Heat Generation Due to Shockley–Read–Hall (SRH) Recombination

Figure 1.3 shows the band diagram which illustrates the recombination process. In Figure 1.3, the SRH recombination is used to describe the recombination of the electron and hole at the undesired energy level, which is created within the band gap by defects in the lattice. They were first investigated by Shockley, Read, and Hall in 1952 and were used as a model to study the nonradiative recombination caused by defects [8].

Defects in the crystal structure are the main cause of SRH nonradiative recombination. These defects include unwanted foreign atoms and crystallographic defects. All of the defects have energy-level bands that are different from the major semiconductor atoms. Therefore, one or more new energy levels can be generated within the forbidden band gap. Unfortunately, these energy levels within the gap of the semiconductor are efficient recombination centers, especially when the deep level is near the middle of the gap. Detailed analytical expressions are obtained for the lifetime estimation of the SRH recombination [7]. These expressions reveal that when the trap level is at or close to the mid-gap energy, the lifetime is twice the minority lifetime and the probability of SRH recombination is increased. Moreover, the increase in temperature will raise the nonradiative recombination probability. For simplicity, the recombination rate can be estimated by $\text{Rate}_{\text{SRH}} = k_{\text{SRH}}n$, where k_{SRH} is the SRH recombination coefficient and n is the carrier concentration [9].

1.2.3 Heat Generation Due to Auger Recombination

Auger recombination describes the process in which the electron in CB gives off excess energy and recombines with a hole in VB. During this process, the excess energy is obtained by a second electron or hole instead of emitting the energy as a photon. The newly excited electrons or holes release their energy through collision with the crystal lattice and return back to the band edges.

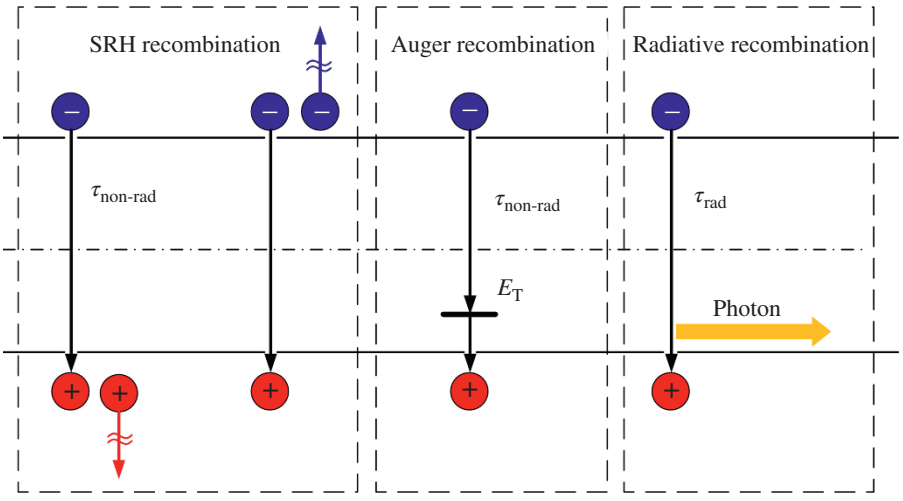

Figure 1.3 Band diagram illustrating: SRH recombination, Auger recombination, and radiative recombination. Adapted from Schubert [7].

The probability of Auger recombination increases with the concentration of charge carriers since this process is based on the ability of the charge carriers to exchange energy. The rate of Auger recombination can be expressed as $\text{Rate}_{\text{Auger}} = k_{\text{auger}} n^3$, where k_{auger} is the Auger recombination coefficient and n represents the carrier concentration. The coefficient k_{auger} on the scale of 10^{-28}–10^{-29} $\text{cm}^6 \cdot \text{s}^{-1}$ for III–V semiconductors plays an important role [10]. Normally, k_{auger} decreases with increased energy band gap. According to the reported Auger recombination coefficients in Table 1.1, the simulation work adopts 10^{-30} $\text{cm}^6 \cdot \text{s}^{-1}$ for GaN-based LED chip design, which exhibits good prediction of device performance [15]. More detailed discussions about the Auger recombination coefficients can be found in reports by Cho et al. [16]. At low carrier concentrations, the Auger recombination is neglected for practical reasons. However, at very high excitation intensity or carrier injection in the current situation, n is much higher and Auger recombination should be considered.

Table 1.1 Auger recombination coefficients reported for GaN-based LED chips.

Material	Auger recombination coefficient ($\text{cm}^6 \cdot \text{s}^{-1}$)	Reference
$In_{0.10}Ga_{0.90}N/GaN$	1.5×10^{-30}	[11]
InGaN/GaN	3.5×10^{-31}	[12]
$In_xGa_{1-x}N$ ($x \sim 9\%$–15%)	1.4–2.0×10^{-30}	[13]
GaInN/GaN	2.5×10^{-31}	[14]

1.2.4 Heat Generation Due to Surface Recombination

Nonradiative recombination also occurs at the semiconductor surface. At surfaces, the periodicity of the crystal lattice ends. Therefore, the band diagram will change at the surface since the strict periodicity of the crystal arrangement is perturbed. Additional electronic states will appear within the forbidden gap of the material [17]. Fortunately, surface recombination can be greatly reduced if the injected carriers are away from the surface. This can be realized by carrier injection under one contact, which is smaller than the LED chip.

1.2.5 Heat Generation Due to Current Crowding and Overflow

Heat generation within the active region of LED chips due to the nonradiative recombination is introduced. Here, the focus will be placed on heat generated outside the LED active region. Particularly, heat generation due to current crowding and overflow will be considered. The solutions are largely attributed to efficient LED chip design at the epitaxial and device levels.

In the realm of semiconductor physics, current crowding is used to describe a nonhomogeneous distribution of current density through the semiconductor at the vicinity of the contacts and over the PN junctions. As shown in Figure 1.4(a), in conventional LED chips, the GaN layer grows on insulating substrates (e.g., sapphire) where electrons laterally spread from N-pad to P-pad. Due to this geometry, the finite resistance of the Ohmic contact and the confinement layer causes the current to "crowd" near the edge of the contact. As shown in Figure 1.4(b), the current density distribution can be undesirably nonuniform. The current density could drop from $99\ \text{A} \cdot \text{cm}^{-2}$ at N-pad to $11\ \text{A} \cdot \text{cm}^{-2}$ at P-pad [18].

Due to the nonlinear distribution of the current density, the crowding phenomenon becomes more severe in high-power LEDs operating at high current density. The remarkable current concentration at the edges of P-type and N-type electrodes has a detrimental effect on the device performance. On the one hand, the local increase in carrier density leads to a high recombination rate, causing nonuniformity of light emission in the active region. This will induce localized overheating of the heterostructure at certain points and the formation of hotspots, whereas a large portion of the device remains inactive during operation. On the other hand, the nonhomogeneous distribution of current will increase the electromigration effect, and voids will be formed. Overall, current crowding will induce the local overheating of the heterostructure, lower the device performance, and increase the series resistance.

Various solutions have been proposed to reduce the current crowding problem, such as multifingered chip design [19]. Through simulation, Joshi et al. report that the current crowding problem is finally eliminated by a combination of multifinger with delta-doping design. Vertical chip configuration can also solve this problem. Figure 1.5 presents the schematic