ADVANCED NANOSCALE MOSFET ARCHITECTURES

CURRENT TRENDS AND FUTURE PERSPECTIVES

EDITED BY

KALYAN BISWAS | ANGSUMAN SARKAR

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Current Trends and Future Perspectives

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Preface

The field of metal–oxide–semiconductor field-effect transistor (MOSFET) devices has observed swift growth in the last decade. In recent years, scientists' views on the use of technology have increased. Nanotechnology is a technology that has the potential to significantly impact almost all areas of human activity, raising great hopes for finding solutions to the major needs of society. The fields of application of research in nanoscience include aerospace, defense, national security, electronics, biology, and medicine. In recent years, human knowledge has made great progress through both theoretical analysis and experimental findings in the area of nanoscience and nanoscale devices.

Nanoelectronic devices are the basis of today's powerful computers and are attracting many new applications, including electronic switching, sensing, and other computational applications. However, our purpose is not to discuss specific tools or applications. Rather, it is to illustrate the concept that has emerged in the last two years to understand the flow of electricity at the atomic scale. This is important not only for the creation of new nanoscale materials but also for the insights it provides into some long-standing questions in transport and quantum physics.

Reasonable attention has been given to editing this book to promote knowledge exchange and collaboration among different stakeholders in the field of nanoscale materials. Nano-devices include new and broad fields of activity such as physics, chemistry, biology, and materials engineering focusing on the nanoscale. To understand how these devices work, it is crucial to understand the structure, properties, and quantum behavior of these devices.

Modern life is revolutionized by the advancements of complementary metal–oxide–semiconductor (CMOS) technology. Performance of MOSFET has been improved continuously at a dramatic rate via gate length scaling since its invention. In order to serve the next-generation high-performance requirements with lower operating power, remorseless scaling of CMOS technology has now reached the atomic scale dimensions. Conventional MOSFET scaling not only involves the reduction of device size but also requires the reduction in the transistor supply voltage (V_{DD}). With the reduction of V_{DD}, the threshold voltage (V_{th}) must be scaled down simultaneously in order to attain reasonable ON-state current, reduce delay, and maintain sufficient gate overdrive voltage. As a consequence of scaling of device following Moore's law, the channel length of the MOSFET is reducing every year, causing short channel effects (SCEs). Different strategies have been considered to surmount SCEs using different device architectures and material compositions.

In this book, the problems associated with the emerging nanoscale MOSFET devices and their trends are highlighted. This book is focused on the evaluation of the present development of nanoscale electronic devices and the future projection of device technologies. Basic device physics and MOSFET operation are presented at the beginning. A widespread discussion on basics of MOSFETs and potential difficulties related to scaling and its remedies is presented. Next, discussion on the impact of high-*k* gate dielectrics in next-generation transistors is included. The effects of trap charges on dielectric defects for multiple gate devices, strain engineering for advanced devices like FinFETs, gate all around nanosheet transistors, etc., have been discussed in different chapters. TCAD analysis is a very important methodology for device performance analysis. TCAD simulation is discussed for negative capacitance field-effect transistors (FETs) and their linearity performance. Quantum-mechanical tunnelling effect for electrically doped nano-devices is also included in the scope of this book. The principles and operations of tunnel FETs, graphene-based FETs, and related issues are discussed. Applications of GaN devices are considered for optoelectronics applications. Performance analysis of nanosheet transistors and low-power circuit design using advanced MOSFETs is also discussed. Finally, an FET-based biosensor with negative capacitance is included.

Readers can feel pleasure in learning about nanoscale devices in real-world applications. Throughout this book, one can discover the amazing developments of nanoelectronics, its challenges, and its future prospects. We hope that this book will appear as a one volume reference for postgraduate students, prospective researchers, and professionals requiring knowledge for design of integrated circuits using nanoscale devices.

November 4th, 2024

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1

Emerging MOSFET Technologies

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1.1 Introduction: Transistor Action

The human life of the modern generation has been revolutionized by the progress of complementary metal–oxide–semiconductor (CMOS) technology. Metal–oxide–semiconductor field-effect transistor (MOSFET) is one of the most noteworthy inventions of the twentieth century. One important milestone in the progress of semiconductor integrated circuits was the famous – Moore's law [1]. Following Moore's law, the performance of MOSFET has been improved continuously at an intense rate through gate length scaling. To serve the next-generation high-performance requirements with lower operating power, unrelenting scaling of CMOS technology has now reached the atomic scale dimensions. The trend will continue with emerging areas of applications such as the internet of things (IoT), e-mobility, artificial intelligence, and 5G. The cutting-edge innovation in MOSFET technologies is the most important and at the heart of these emerging technologies. A schematic diagram of the Conventional Bulk MOSFET Structure is shown in Figure 1.1.

1.2 MOSFET Scaling

This downscaling of dimensions of the device is critical to integrate the greater number of devices in integrated circuits (ICs). As a consequence of the Moore's law, every year channel length of the MOSFET sinks, causing short channel effect (SCEs). SCEs are affecting power consumption of the circuits [2–9]. The transistor scaling target has been made reachable because of the advanced lithographic

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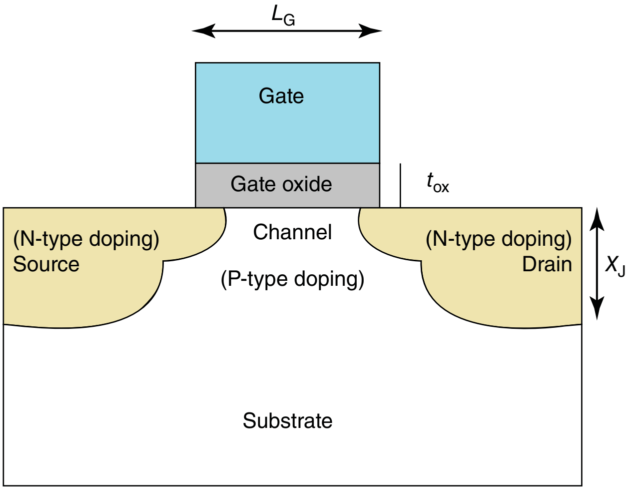

Figure 1.1 Schematic diagram of the Conventional Bulk MOSFET Structure.

capability to make shorter/thinner channels. In the early stage, scaling was possible with conventional structures and material technology, but it is understood that conventional scaling technology cannot continue forever. Therefore, investigation of non-classical device structures became necessary.

1.3 Challenges in Scaling the MOSFET

Scaling of MOSFETS is not an easy task but faces lots of challenges. Normally, six different short-channel effects can be distinguished such as "Sub-Threshold Slope," DIBL and threshold voltage roll-off, velocity saturation, hot carrier effects, and direct source to drain tunneling [10–12].

As the SCEs set hurdles to device operation and degrade device performance, these effects should be removed or minimized, so that a device with a shorter physical channel length can preserve the required device characteristics. Researchers tried to overcome these problems by reducing the gate oxide thickness and the depth of source/drain junction while reducing the gate length in conventional bulk MOSFETs. But these scales reached the physical limit of dimension. As a remedy, gate dielectric materials with higher permittivity were used. The use of these high-k materials as gate oxide allowed for achieving smaller equivalent oxide thickness with a thicker physical dimension. But shrinking of MOSFET to the sub-10 nm scale is challenging and new technologies were necessary. As per ITRS forecasts and published literature, it is understood that the main research is going on in two different directions: possible modification of the planar architecture and use of non-planner 3D structure [13–17] to push for its physical limits, or a new way of making transistors, such as devices based on III–V group materials, use of nanomaterials and nanotechnologies like silicon nanowires, carbon nanotubes (CNTs) or graphene, single electron transistors, and also some other emerging devices such as quantum cellular automata and spin-based electronics.

1.4 Emerging MOSFET Architectures

For decades, traditional scaling techniques based on sinking its physical dimensions have largely dominated the development path of MOSFETs. However, this traditional scaling technique is not valid for emerging nanoscale devices. As device scaling enters beyond the 22 nm node, various significant changes in terms of device architecture and materials in the traditional MOSFET would be required for the competent operation of the device and to extend Moore's law [18–21]. To surmount SCEs, researchers are employing different strategies for nanoscale devices. The main approaches are (i) by employing different structures such as multigate MOSFETs (ii) advanced device physics approaches, such as junctionless MOSFET, tunnel FET (TFET), and (iii) different channel materials having higher carrier mobility such as III–V-based materials, strained silicon, CNTs, Graphene, etc. for continuing the progress in nanoscale.

1.4.1 Tunnel FET

To reduce power consumption in MOSFETs without degrading device performance, operating voltage (V_{dd}) and threshold voltage (V_{th}) of the device need to be scaled down. If V_{th} is reduced keeping sub threshold swing (SS) of MOSFET unchanged, the power consumption increases. The TFET, which is based on the principle of band-to-band quantum tunneling, is one of the most favorable devices, having a steep slope for applications in low-power circuits. The device structure of a TFET differs from that of the conventional MOSFET as a type of doping in the source region and drain region of TFET are of opposite types. A schematic diagram of single-gate n-type TFET is shown in Figure 1.2. A positive voltage in the gate and reverse bias between the source and drain is required to switch the n-type device ON. It is a semiconductor device based on the band-to-band tunneling principle of electrons rather than thermal emission. TFETs operate by tunneling through the S/D barrier rather than diffusion over the barrier [22–31]. The device switches between ON-state as well as OFF-state at lower voltages than the V_{dd} of the MOSFET, making it a suitable choice for low-power consumption applications in the era of emerging nanoscale devices. This type of device can

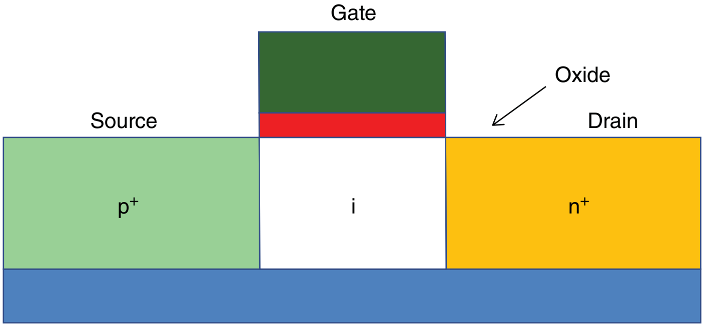

Figure 1.2 Schematic diagram of tunnel FET.

provide extremely low OFF-current and steeper sub-threshold slope than conventional MOSFET. Tunneling occurs for an electron between the valence band of the semiconductor to the conduction band through a potential barrier without having enough energy required for this transition, and this phenomenon can only be explained by quantum mechanical physics. The output characteristics of a TFET are dependent on the parameters such as the doping, the gate work function, etc. Therefore, these parameters can be modified to obtain the desired output characteristics of a TFET. However, from the fabrication point of view, TFET faces a few challenges such as the fabrication of an ultra-thin body required for robust electrostatics, formation of abrupt junction, III–V/high-*k* interface with low trap density, etc.

Two-dimensional crystal semiconductors are being investigated as the materials of the channels for field effect transistors (FETs). The main advantages of such 2D-transistors consist of outstanding electrostatic control of the gate terminal because of the considerably higher surface-to-volume ratio, pristine surfaces to confirm better interface quality with the insulators, and greater electrical conductivity owing to the ballistic/quasi-ballistic transport. It also offers tunable electronic properties dependent on the layer and stacking providing further flexibility in transistor design. These distinctive attributes offer the chance to acquaint with 2D materials in the design of TFET, which can concurrently combine the benefits of greater electrostatic integrity and tunneling barrier engineering. As a result, the arena of TFET design based on 2D materials has grown significantly in recent years.

1.4.2 Nanowire FET

In the era of sub-10-nm technology nodes, cylindrical-shaped structures with gates all around were proposed to provide better gate controllability on the

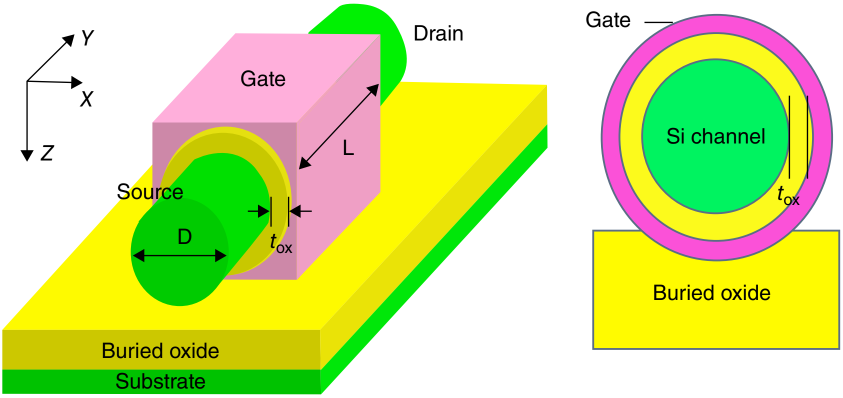

Figure 1.3 Schematic 3D view and a cross-sectional view of a cylindrical FET.

channel and reduce "Short Channel Effects" [32–35]. In this structure, a gate is wrapped around the cylindrical-shaped channel region and termed a silicon nanowire FET (Figure 1.3). Nanowires can be fabricated with single-crystal structures, controllable doping, and diameters as small as several nanometers. Though the silicon nanowire transistors (SNWT) improves device performance, the fluctuations in process parameters rigorously affect the device characteristics. As per the projection of the International Technology Roadmap for Semiconductor (ITRS), the multiple-gate SOI MOSFETs will be able to scale up to sub-10 nm dimensions and are capable candidates for nanoscale devices in the future.

1.4.3 Nanosheet FET

Nanosheet FETs are considered as a transistors of next-generation technology, which have been broadly adopted by the industry to carry on logic scaling beyond 5 nm technology nodes, and beyond FinFETs. Scaling of FinFET beyond 7 nm node results worsened SCEs, forced them to move from tri-date to gate all-around structures. Among different gate all-around structures, wider nanosheets provide higher "ON" current and better electrostatic control [36]. FinFETs were the first architectural change of devices in transistor history and gate-all-around nanosheet FETs are the milestones in the history of transistor devices as they utilize the complete architectural change. To obtain the full advantages of nanosheet FETs, multiple nanosheets should be stacked on one another. The channel thickness during the stacking is fully dependent on the lithographical limit of the fabrication process. Induction of strain to increase hole mobility has also been adopted recently to improve the device's performance (Figure 1.4).

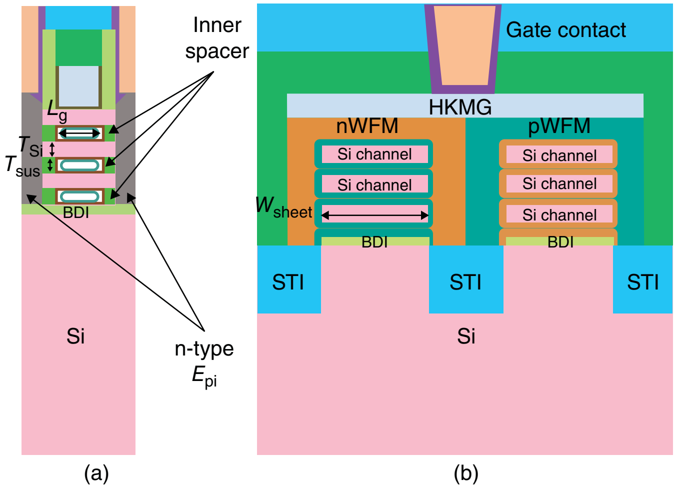

Figure 1.4 Schematic diagram of a gate-all-around nanosheet FET [36]/MDPI/CC by 4.0. Cross section view across a) source-drain region b) gate region.

1.4.4 Negative Capacitance FET

The negative capacitance field effect transistor (NCFET) has become a good solution for extending Moore's Law due to its process compatibility, high on/off current ratio, and low subthreshold swing. In these devices, a layer of ferroelectric material is sandwiched between the gate oxide and gate metal and utilizes the property of polarization inversion of the ferroelectric material under the influence of gate voltage to provide negative capacitance (Figure 1.5).

Additionally, the use of ferroelectric layers, for example, NCs in the gate stack, helps to reduce the sub-threshold slope of the FET to less than the theoretical limit

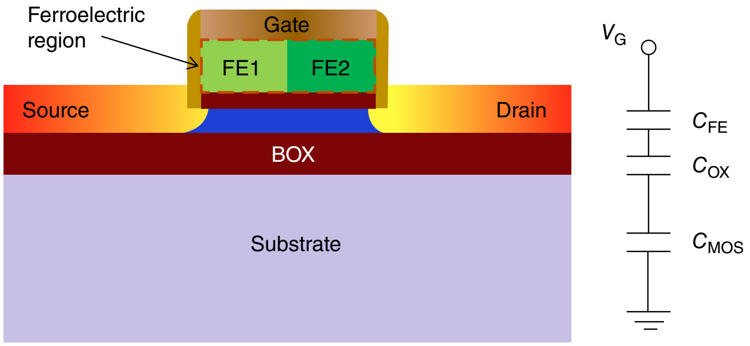

Figure 1.5 (a) Schematic diagram of the DFR-negative capacitance FET, (b) equivalent capacitance model of the device [37]/MDPI/CC by 4.0.

of 60 mV/decade [37]. Various additives such as Al (HAO), Zr (HZO), and Si (HSO) in hafnium-based ferroelectric materials have also been considered to improve the performance of NCFETs.

1.4.5 Graphene FET

CNTs are planar graphite sheets known as graphene that are wrapped into tube shapes. CNTs have outstanding electrical characteristics and they can be fabricated with very small dimensions, as small as 4–8 Å in diameter. The encouraging electrical properties of a CNT depend on its diameter and the wrapping angle of the graphene. Theory shows that the structure of CNTs may be expressed by a chiral vector linked with two integers (n, m). CNTs can be metallic or semiconducting depending on the difference of values in fundamental tube indices (n, m), and their bandgap is dependent on the diameter. The analysis also indicates that semiconducting CNTs have very high low-field mobility, large current-carrying capability, excellent thermal and mechanical stability, and high thermal conductivity [38–40]. Because of their superior material properties, nanotubes are attractive as future interconnects and show enormous advantages as a channel material of high-performance MOSFETs. Though CNT-based MOSFETs promise great performance lots of processing issues remain such as fabrication of identical nanotubes, control of abrupt doping profiles, etc. A sketch of the graphene FET is shown in Figure 1.6 [39].

1.4.6 III–V Material-based MOSFETS

As the performance improvement of silicon-based MOSFETs reaches its limit of scaling. Interest has been greatly increased in introducing non-silicon materials as

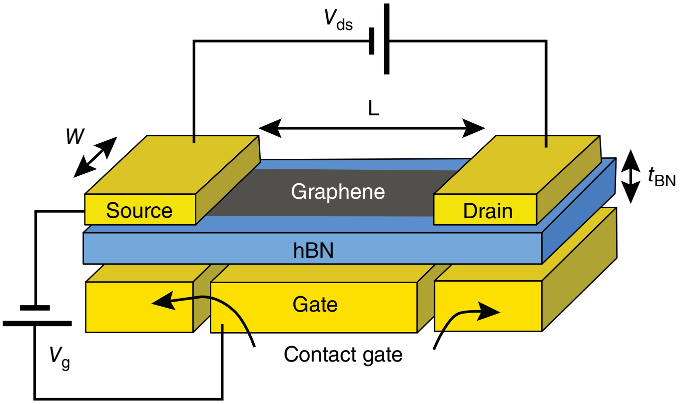

Figure 1.6 A sketch of the graphene FET [39]/MDPI/CC by 4.0.

a channel. III–V-based MOSFETs are considered one of the most efficient devices for high-performance digital logic applications. Currently, III–V MOSFETs are expected to allow higher drive currents and greater flexibility than silicon-based MOSFETs. A wide range of compound semiconductor materials can be obtained using elements from the Periodic Table's columns III and V, like GaAs, InP, and $In_xGa_{(1-x)}As$. The main parameter which defines the important characteristics of these materials is the bandgap energy. The integration of Ge/III–V and Si CMOS platforms is promising in providing low-power integrated circuits in 10 nm technology nodes and beyond [41]. One of the key challenges of the III–V MOSFET technology is thermodynamically stable, high-quality gate dielectrics that passivate the interface states.

1.4.7 HEMT

In recent times, high electron mobility transistor (HEMT) accomplished excessive interest due to its superior electron transport. HEMT devices are facing tremendous challenges and replacing traditional field-effect transistors (FETs) because of their outstanding performance at high frequencies [42]. HEMT technology was first innovated by T. Mimura who was involved in compound semiconductor device development at Fujitsu Laboratories Ltd, Japan [43]. HEMT devices incorporate heterojunctions formed at the junction of two different bandgap materials in which electrons are trapped in quantum wells to avoid scattering by impurities. Thanks to their higher electron mobility and dielectric constant, GaAs having direct bandgap have been used in high-frequency applications and the field of optoelectronic integrated circuits. AlGaAs having nearly similar lattice constant but larger bandgap in comparison to GaAs, are considered the most suitable contender for barrier material and one of the most prevalent choices to be used in HEMTs [44–46]. However, another excellent material that has been widely studied for HEMT devices in recent years is AlGaN/GaN. AlGaN/GaN HEMTs can operate at very high frequencies with high breakdown strength and high saturation electron velocity. GaN also shows very robust piezoelectric polarization that helps to accumulate huge carriers at the interface of AlGaN/GaN. The performance of the MEMS devices depends on many factors such as a combination of material layers, concentration of doping, and different layer thicknesses, which provide flexibility in the device design process.

1.4.8 Strain Engineered MOSFETs

Strained silicon technology based on the improvement of carrier mobility under the influence of axial strain. Proper use of strain in the silicon channel has emerged as a powerful technique for improved MOSFET performance [47].