The Designer's Guide to Jitter in Ring Oscillators

The Designer's Guide Book Series

Series Editor: Ken Kundert
Cadence Design Systems
San Jose, CA
USA

The Designer's Guide to Jitter in Ring Oscillators
John A. McNeill and David S. Ricketts
978-0-387-76526-6

The Designer's Guide to High-Purity Oscillators
Emad Hegazi, Jacob Rael, and Asad Abidi
978-1-4020-7666-4

The Designer's Guide to Verilog-AMS
Ken Kundert and Olaf Zinke
978-1-4020-8044-9

The Designer's Guide to SPICE and Spectre®
Ken Kundert
978-0-7923-9571-3

For other titles published in this series, go to
www.springer.com/series/6967

John A. McNeill • David S. Ricketts

The Designer's Guide to Jitter in Ring Oscillators

Springer

John A. McNeill
Worcester Polytechnic Institute
Worcester, MA
USA

David S. Ricketts
Carnegie Mellon University
Pittsburgh, PA
USA

ISBN 978-0-387-76526-6 e-ISBN 978-0-387-76528-0
DOI: 10.1007/978-0-387-76528-0

Library of Congress Control Number: 2009920784

Printed on acid-free paper.

springer.com

Preface

This is a book for engineers concerned with jitter: the effects of noise visible in the time domain. The material presented will be helpful for work at both the system level and the circuit level:

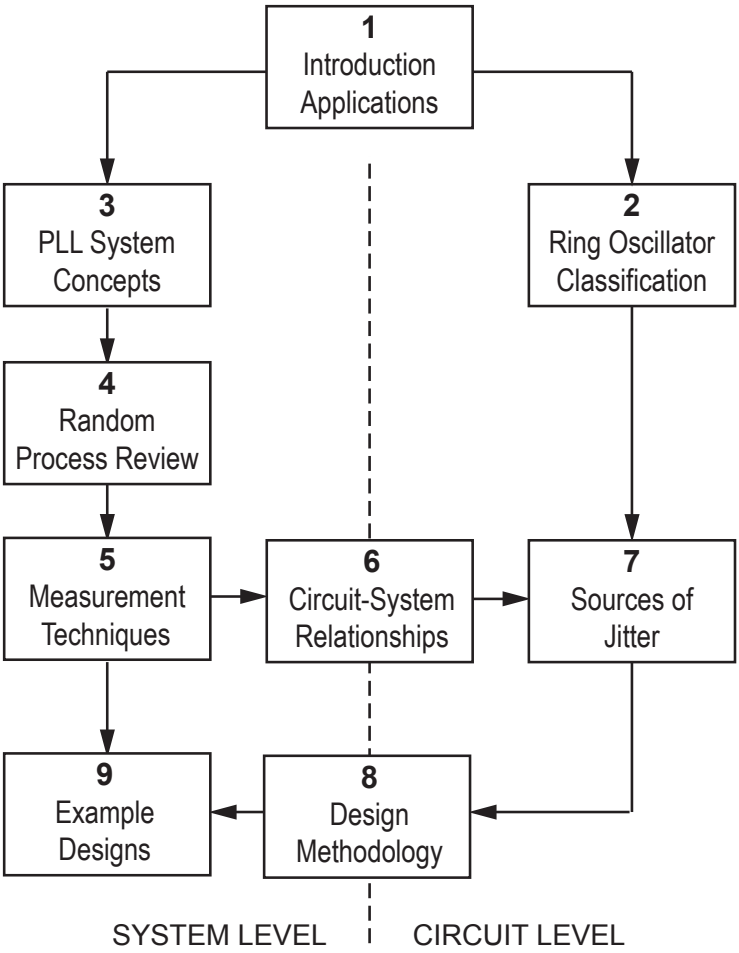
- At the system level, the challenge is to describe, specify, and measure time domain uncertainty and when necessary, relate jitter to phase noise specifications in the frequency domain.
- At the circuit level, the challenge is to design low noise circuitry within power, area, and process constraints so that ultimate performance meets system level requirements.

Throughout the book concepts are presented in the context of an engineering application requiring low jitter performance: the voltage controlled oscillator (VCO) used in a phase-locked loop (PLL). Techniques are presented for circuit-level design of low jitter delay elements for use in ring oscillators, as well as relating the circuit-level characteristics to system-level performance. Although the emphasis is on time-domain (jitter) measures of oscillator performance, a simple method of translating performance to frequency domain (phase noise) measures is presented as well.

Structure of this Book

This book is divided into nine chapters. The diagram on the following page shows the relationship between material in each chapter as well as placement in the system-level vs. circuit-level design hierarchy. Wherever possible, experimental verification is presented in the same chapter as the corresponding theoretical development, rather than being isolated in a separate chapter.

Chapter 1 begins as a bridge between the system and circuit levels, describing a range of applications for which jitter is a concern and beginning the exploration of the ring oscillator on the circuit level. Somewhat more emphasis is placed on clock recovery in serial data communication, the main



application for which this work was originally done. Chapter 1 also provides a brief overview of the different types of VCOs that are used in clock recovery PLLs, and establishes the need for an intuitive methodology to guide design for low-jitter ring VCOs.

Chapter 2 provides a classification of existing ring oscillator delay stage circuits according to signal type, output, and method of tuning. This classification scheme is organized from the circuit designer's perspective, covering most existing ring oscillator architectures and laying the foundation at the circuit level for the system level analysis techniques that will be developed to guide the designer in choosing among the options and tradeoffs in the ring oscillator VCO design process.

Chapter 3 introduces fundamental concepts for understanding phase, phase noise, and jitter, as well as their effect on the PLL. A review of fundamental PLL and phase noise concepts shows how VCO jitter is shaped by PLL loop dynamics to determine system-level jitter. After a brief introduction to jitter measurement techniques, several different system-level jitter and phase noise measures are specified which will be related by a mathematical framework to be described in Chapter 5.

Chapter 4 reviews the basic system-level concepts of random signals and noise used in the development of the mathematical framework of Chapter 5. It is meant as a review for the reader who has studied random signals or as an introduction for the circuit designer new to the area.

Chapter 5 covers the mathematical development of a technique for relating different jitter and phase noise measures introduced in Chapter 5. A key insight in this chapter is the definition of figures-of-merit, N_1 (frequency domain) and $\mathcal{K}$ (time domain), to describe jitter of the open-loop VCO. Knowledge of either N_1 or $\mathcal{K}$, together with the PLL loop dynamics, gives complete information on the system-level closed-loop jitter performance as measured in either the time or frequency domain. The technique is verified experimentally through measurements made on several existing PLLs and VCOs in both closed loop and open loop conditions.

The material in Chapter 6 begins building a "bridge" in the methodology necessary for circuit-level design to meet a required system-level specification. It is seen that the time domain figure-of-merit $\mathcal{K}$ is independent of both the ring frequency and number of stages, and thus can provide an intuitive link between circuit-level and system-level performance. This leads to a simple, general design methodology which flows naturally from the time-frequency domain relationships described in Chapter 5. Experimental results are presented verifying the concepts underlying the methodology.

Chapter 7 is concerned with circuit-level design of delay stages to realize a low-jitter ring VCO function. The jitter figure of merit $\mathcal{K}$, developed in Chapters 5 and 6, is applied to characterize jitter in delay stages designed in both CMOS and bipolar technologies. Explicit numerical relationships are developed relating noise sources to resulting jitter. Simulated and experimental results from several rings of different lengths demonstrate the applicability of this approach. Comparing the expressions for $\mathcal{K}$ in rings with results from other types of VCOs illuminates the relative merits of ring oscillators in terms of jitter performance.

Chapter 8 completes the "bridge" back to the system level from the circuit level, providing a summary of the entire methodology for the designer whose interest is circuit level design of a low jitter ring oscillator. Starting with desired jitter performance at the system level, expressed in either the time or frequency domain, the procedure gives explicit constraints on values of circuit elements.

As examples of the procedure in Chapter 8, the design of low jitter ring VCOs for both CMOS and bipolar PLLs is described in Chapter 9. Design

techniques for overcoming some of the inherent limitations of the ring architecture are discussed. Measured test results, incorporating the techniques of Chapter 7 are presented showing good agreement to the design methodology's numerical predictions.

Acknowledgements

The authors acknowledge the support of our colleagues at our respective institutions, Worcester Polytechnic Institute and Carnegie Mellon. At Analog Devices, Inc., Larry DeVito provided critical financial support and technical guidance for this work at its inception; Bob Surette and Rosa Croughwell also contributed technical support and valuable discussions. We thank Ted Arbo, Joe Carr, and Rich Hoft from Agilent; John Seney and Mike Schnecker of LeCroy; Laszlo Dobos and Bob Wieners from Tektronix, for assistance with the instrumentation described in Chapter 5. The National Science Foundation provided funding to support several past and present graduate students who have assisted in this work, including Yuping Toh, David Bowler, Chengxin Liu, Ali Ulas Ilhan, Michael Chen, En Shi and Qianyu Liu. We thank the editorial staff at Springer for their assistance in developing this book, and the work of the reviewers for their comments which have helped to improve it. Finally, we thank our families for their patience and support.

Worcester, MA — *John A. McNeill*
Pittsburgh, PA — *David S. Ricketts*
November 2008

Contents

1 Introduction to oscillator jitter 1
1.1 Applications 1
1.1.1 Clock recovery in serial data transmission 1
1.1.2 Methods of clock and data recovery 3
1.1.3 Other applications 4
1.1.4 Summary 5
1.2 Types of VCOs 7
1.2.1 LC resonant 7
1.2.2 Multivibrator 8
1.2.3 Ring oscillator 8
1.3 Motivation and goals of this book 9
1.4 Chapter summary 11

2 Classification of ring oscillators 13
2.1 Type of signal in the ring 13
2.1.1 Single-ended 14
2.1.2 True differential 16
2.1.3 Pseudo differential 18
2.1.4 Regenerative switching 21
2.1.5 Signal format summary 21
2.2 Tuning method 21
2.2.1 Number of stages 22
2.2.2 Loading 24
2.2.3 Drive strength 27
2.2.4 Voltage 28
2.2.5 A Note on linearity 29
2.2.6 Summary 29
2.3 Output format 29
2.3.1 Single output 31
2.3.2 Dual output (quadrature) 33
2.3.3 Multiple output 34

2.3.4 Summary 34
2.4 Chapter summary 34

3 Phase-Locked Loop System Concepts 35
3.1 Phase and frequency concepts 35
3.2 Phase and jitter concepts in PLL applications 39
3.2.1 Response of PLL loop to input signal and VCO phase noise 40
3.2.2 Summary 43
3.3 Measuring phase 43
3.3.1 Time Domain 43
3.3.2 Time domain: two sample standard deviation 44
3.3.3 Frequency Domain 46
3.3.4 Summary 49
3.4 Measures that will be related in this book 49
3.4.1 Case (i): Frequency domain, VCO open loop 50
3.4.2 Case (ii): Frequency domain, PLL closed loop 52
3.4.3 Case (iii): Time domain, closed loop, transmit clock referenced 54
3.4.4 Case (iv): Time domain, closed loop, self-referenced 56
3.4.5 Case (v): Time domain, open loop, self referenced 58
3.5 Chapter Summary 59
Appendix 3A Approximate loop transfer functions 62
Appendix 3B Power spectra relationships 66

4 Overview of Noise Analysis Fundamentals 69
4.1 Fundamentals of random signals - time domain 69
4.1.1 Deterministic vs. stochastic signals 69
4.1.2 Expectation value and time average 71
4.1.3 Autocorrelation 73
4.1.4 Variance 79
4.1.5 Classes of random signals 81
4.2 Fundamentals of random signals - frequency domain 82
4.2.1 Fourier transform 82
4.2.2 Power spectrum of random signals 82
4.3 Circuit analysis with random voltages and currents 84
4.3.1 Time domain 84
4.3.2 Frequency domain 86
4.3.3 Measurement of p.s.d. 88
4.4 Noise 89
4.4.1 Types and classification of noise 89
4.4.2 Representation of noise 92
4.5 Noise in oscillators 92
4.5.1 Time domain - jitter 93
4.5.2 Frequency domain - phase noise 94

4.6 Chapter summary 96
Appendix 4A Non-ergodic processes 98
Appendix 4B Exponentials with gaussian distributed exponents .. 99
Appendix 4C Fourier transform pairs 100

5 Measurement Techniques 101
5.1 Theoretical development 101
5.1.1 Case (i): Frequency domain, VCO open loop 101
5.1.2 Case (ii): Frequency domain, PLL closed loop 102
5.1.3 Case (iii): Time domain, closed loop, transmit clock referenced 102
5.1.4 Case (iv): Time domain, closed loop, self-referenced 103
5.1.5 Case (v): Time domain, open loop, self referenced 103
5.2 Instrumentation 106
5.2.1 Time domain measurement instruments 106
5.2.2 Frequency domain instrumentation 112
5.2.3 Instrumentation summary 112
5.3 Experimental verification 113
5.3.1 PLL with multivibrator VCO 113
5.3.2 Ring VCO 118
5.3.3 Discussion of results 118
5.4 Chapter summary 120
Appendix 5A Analysis of jitter process 121
Appendix 5B Data acquisition techniques 123

6 Analysis of jitter in ring oscillators 129
6.1 Review of jitter analysis in different types of oscillators 129
6.1.1 Harmonic oscillators 129
6.1.2 Relaxation oscillators 132
6.1.3 Ring oscillator 136
6.2 Jitter model theoretical development 137
6.2.1 Time domain approach: jitter in each oscillator period . 138
6.2.2 Special case I: independent delay errors give $1/f^2$ spectrum 140
6.2.3 Special case II: correlated delay errors 143
6.2.4 General case 146
6.2.5 Development in terms of gate delays 148
6.3 Methodology: applying model to circuit design 150
6.4 Experimental verification 151
6.5 Chapter summary 155
Appendix 6A Stationarity of two-sample variance 156
Appendix 6B Variance of clock period errors 157

7 Sources of jitter in ring oscillators 161
7.1 Introduction 161
7.1.1 Classification of jitter sources 161
7.1.2 Strategy 164
7.2 Control Path: system-level sources of noise 166
7.3 Load element noise 167
7.3.1 Fully differential case 167
7.3.2 Single ended case 171
7.3.3 Comparison of differential, single-ended $\mathcal{K}$ expressions . . 174
7.4 Switching element noise 175
7.4.1 Fully differential case 175
7.4.2 Single ended case 189
7.4.3 Comparison with other jitter sources 196
7.4.4 Variation in $\mathcal{K}$ with tuning 196
7.5 Bias element noise 199
7.5.1 Fully differential case: tail current noise 199
7.5.2 Comparison with other jitter sources 203
7.6 Summary of noise contributions 204
7.7 Experimental Verification 208
7.7.1 Simulation 208
7.7.2 Hardware tests 214
7.8 Comparison with jitter in harmonic oscillator 220
7.8.1 Time domain approach 220
7.8.2 Frequency domain approach 221
7.9 Chapter summary 223
Appendix 7A Differential pair switching delay 224
Appendix 7B Time-domain (transient) noise source simulation . . . 227

8 Design methodology 231
8.1 Implications for design and simulation 231
8.2 Methodology 0verview 233
8.2.1 Step 1: refer design goal to asymptotic $\mathcal{K}$ 233
8.2.2 Step 2: adjust asymptotic $\mathcal{K}$ to gate-level $\mathcal{K}$ 234
8.2.3 Step 3: determine constraints on the design of the individual gate 234
8.2.4 Step 4: design for ring center frequency 235
8.3 General design techniques for low jitter 237
8.4 Chapter summary 237

9 Low jitter VCO design examples 239
9.1 CMOS single-ended ring oscillator 239
9.1.1 VCO topology 239
9.1.2 Number of stages 240
9.1.3 Oscillation frequency 241
9.1.4 Frequency tuning 242

9.1.5 Jitter minimization - long channel 244
9.1.6 Jitter minimization - short channel 245
9.1.7 Experimental results 245
9.2 Bipolar differential ring oscillator 247
9.2.1 VCO requirements 247
9.3 Ring oscillator design 249
9.3.1 Experimental results 257
9.4 Chapter summary 264

Index 275

List of Figures

1.1 Typical fiber optic serial data transmission system. 2
1.2 Independent test of BER due to clock recovery function. 3
1.3 Jitter on recovered clock waveform. 4
1.4 Typical wireless communication system. 6
1.5 Typical measurement of oscillator power spectrum. 6
1.6 Conceptual LC resonant oscillator. 7
1.7 Conceptual multivibrator oscillator. 8
1.8 Conceptual ring oscillator. 9

2.1 Ring oscillator with single-ended signal. 14
2.2 Amplitude coupling to single-ended signal. 15
2.3 Delay modulation of single-ended signal. 16
2.4 Ring oscillator with true differential signal. 17
2.5 Amplitude coupling interference to true differential signals. 18
2.6 Ring oscillator with pseudo differential signal. 19
2.7 Amplitude coupling interference to pseudo differential signals. . . 20
2.8 Delay modulation of pseudo differential signal. 20
2.9 Simple model of ring frequency, stage delay. 22
2.10 Discrete “tuning” of ring frequency. 23
2.11 Use of interpolator for continuous tuning of ring frequency. 24
2.12 Combining phase selection, interpolating techniques. 25
2.13 Tuning of ring delay by varying load resistance. 26
2.14 Tuning of ring delay by varying load capacitance. 26
2.15 “Current-starved” ring delay stage. 28
2.16 Tuning delay by varying ring V_{DD}. 29
2.17 Oscillator core with output buffer. 30
2.18 Single output ring oscillators. 31
2.19 Effects of unequal loading. 32
2.20 Addition of dummy stages to mitigate effects of unequal loading. 32
2.21 Ring oscillator with quadrature outputs. 33
2.22 Ring oscillator with multiphase outputs. 34

3.1 Ideal signal vs. signal with jitter / phase noise. 36
3.2 Random walk of a free running VCO. 38
3.3 $1/f^2$ p.s.d. of integrated white noise at VCO output. 39
3.4 PLL used for clock and data recovery. 40
3.5 Phaselock loop as a control system. 41
3.6 Phase signal and noise for shaped $1/f^2$ noise 42
3.7 Measuring σ_x in CDR application. 44
3.8 Jitter measurement over time delay ΔT. 45
3.9 "Direct spectrum" measurement of phase noise. 46
3.10 Idealized system for intuitive view of phase noise spectrum shape 47
3.11 Idealized system for intuitive view of phase noise spectrum shape 48
3.12 Measurement in frequency domain, VCO open loop 51
3.13 Measurement in frequency domain, PLL loop closed 53
3.14 Measurement in time domain, transmit clock referenced 55
3.15 Measurement in time domain, closed loop, self-referenced 57
3.16 Measurement in time domain, open loop, self-referenced 59
3.17 Summary of jitter measurement techniques. 61
A.1 Synthesizer PLL block diagram 62
A.2 Magnitude and phase of loop transmission; phase noise transfer function 64
B.1 Voltage and phase noise waveforms. 67
B.2 Representation of phase noise as added noise in quadrature. . . . 68

4.1 Deterministic versus stochastic signals 70
4.2 Example probability density functions. 71
4.3 Expectation value versus time average. 73
4.4 Ideal integration of a random signal. 75
4.5 Random signal autocorrelation of a low pass, RC filter. 78
4.6 Transfer function for random signals in the time and frequency domains. 85
4.7 Single-sided versus double-sided p.s.d. 88
4.8 Equivalent circuit for noisy resistor. 90
4.9 Random phase in the time domain: jitter. 93

5.1 Mathematical relationships among jitter measurement techniques. 105
5.2 Time domain measurement: clock threshold crossing times. 106
5.3 Time domain measurement: Time Interval Error (TIE). 107
5.4 Instrumentation measurement principle waveforms. 108
5.5 Instrumentation conceptual block diagrams. 109
5.6 $\mathcal{K}$ plot from idealized TIE data. 110
5.7 AD802 Experimental Jitter Results: frequency domain, open-loop. 114
5.8 AD802 Experimental Jitter Results: frequency domain, closed-loop. 115

5.9 AD802 Experimental Jitter Results: time domain, closed loop, transmit clock referenced. 116
5.10 AD802 Experimental Jitter Results: time domain, closed loop, self-referenced. 117
5.11 AD802 Experimental Jitter Results: time domain, open loop, self-referenced. 117
5.12 Four state ring VCO: schematic 119
5.13 Four stage ring VCO: frequency domain, open loop. 119
5.14 Four stage ring VCO: time domain, open loop, self referenced . . 120
A.1 Jitter on clock recovered under closed loop conditions. 121
B.1 Typical time domain measurement program output. 126
B.2 Apparent increase in measured σ when height of histogram box is increased. 127
B.3 Typical frequency domain measurement program output. 128

6.1 LRC resonant circuit. 130
6.2 Impedance of resonant circuit vs. frequency. 131
6.3 Classic emitter-coupled multivibrator. 133
6.4 Schmitt trigger representations of emitter-coupled multivibrator. 134
6.5 Multivibrator equivalent circuit for noise analysis. 135
6.6 Waveforms in multivibrator equivalent circuit. 135
6.7 Typical ring oscillator schematic. 136
6.8 Definition of random process for clock with jitter. 138
6.9 Graphical procedure for autocorrelation calculation. 141
6.10 Graphical summation procedure for VCO with white noise input. 142
6.11 Graphical summation procedure for VCO with white noise input. 144
6.12 Measured jitter with bandlimited white noise at VCO input. . . . 146
6.13 Closed loop jitter σ_x from open loop jitter plot. 147
6.14 Common cases of VCO phase noise. 149
6.15 Experimental results for ring oscillator. 152
6.16 Plot of ring jitter for 3, 4, 5, 7, 9 stage rings. 154
A.1 Definition of $x[n]$ for stationarity proof. 157
B.1 Graphical determination of p.s.d. for $x[n]$ process. 158

7.1 Example delay stage 162
7.2 Example delay stage with noise sources 163
7.3 General gate delay, jitter waveforms. 165
7.4 Load resistance thermal noise model. 168
7.5 Load resistance thermal noise waveforms. 168
7.6 Load resistance noise model, single ended case. 171
7.7 Load resistance noise waveforms, single ended case. 172
7.8 Switching element noise model. 176
7.9 Switching element transconductance model. 177

7.10 Switching waveforms with noise and transconductance model. . . 178
7.11 Differential pair delay gate 183
7.12 Differential input noise switching model. 184
7.13 Differential input noise switching waveforms. 185
7.14 Switching element noise model, single ended case. 189
7.15 Switching element noise waveforms, single ended case. 190
7.16 Switching element noise model, current-starved delay stage case. 194
7.17 Switching element noise model waveforms, current-starved delay stage case. 195
7.18 Drive strength tuning (current starved). 197
7.19 V_{DD} Tuning. 197
7.20 Tail current source noise model. 200
7.21 Tail current source noise waveforms. 200
7.22 Idealized differential pair for simulation. 208
7.23 Load resistor thermal noise simulation results 210
7.24 Tail current noise simulation results 211
7.25 Differential input noise simulation results 212
7.26 Schematic for ring oscillator experiment 214
7.27 Ring experiment results. 218
7.28 Measured results and predicted $\mathcal{K}$ vs. I_{EE} 219
7.29 Noise model of resonator 222
A.1 Differential pair for switching time calculations. 224
B.1 Transient noise simulations. 228
B.2 PSH noise waveform shaped by time-varying gain. 229

9.1 Schematic of CMOS ring oscillator design example 240
9.2 Variation of CMOS stage delay with device width and length . . 243
9.3 $\mathcal{K}$ reduction due to W and L scaling 246
9.4 Frequency tuning for current starved inverter. 247
9.5 4 stage ring schematic. 249
9.6 Interpolating circuit. 251
9.7 Quadrature ring VCO block diagram. 252
9.8 Nonlinearity of interpolating VCO V-to-f characteristic. 254
9.9 Gate schematic with C_{jc} stray capacitance. 255
9.10 Gate schematic with bypass network. 256
9.11 Translinear circuit for nonlinearity compensation. 258
9.12 VCO linearity with/without compensation. 259
9.13 Corner frequency drift over temperature, with/without PTAT bias. 260
9.14 Simulated supply-induced jitter, with/without decoupling network. 261
9.15 VCO open loop, self referenced jitter and $\mathcal{K}$ dependance on x. . . 262

List of Tables

5.1 Instrumentation for jitter and phase noise measurement. 106

6.1 Ring experiment results. 153

7.1 Jitter relationships: load source 175
7.2 Jitter relationships: load source and switching source. 183
7.3 Jitter relationships: load source and switching source for differential; load source for single-ended. 188
7.4 Jitter relationships: load source and switching source for differential; load source and switching source for single-ended. . . 193
7.5 Jitter relationships: load source and switching source for differential; load source and switching source for single-ended, full swing and current starved. 196
7.6 Jitter relationships: load, switching and bias source for differential; load source and switching source for single-ended, full swing and current starved. 204
7.7 Summary of $\mathcal{K}$ contributions by architecture. 205
7.8 Summary of $\mathcal{K}$ contributions by source. 206
7.9 Experimental circuit element values and predicted $\mathcal{K}$ equations . 216

8.1 Example design using relations of Table 7.9. 236

9.1 Ring Oscillator Prototypes 241
9.2 Predicted $\mathcal{K}$ values for bipolar design example. 263

1

Introduction to oscillator jitter

This chapter begins exploration of jitter with system-level issues. Section 1.1 describes a range of applications for which jitter is a concern. Somewhat more emphasis is placed on clock recovery in serial data communication, the main application for which this work was originally done. Section 1.2 also provides a brief overview of the different types of VCOs that are used in clock recovery PLLs, and establishes the need for an intuitive methodology to guide design for low-jitter ring VCOs. Section 1.3 summarizes the motivations and goals for the remainder of the book.

1.1 Applications

1.1.1 Clock recovery in serial data transmission

One application that uses a VCO and PLL to develop a low jitter clock is the clock and data recovery (CDR) function, which is necessary in a wide variety of serial data applications such as FibreChannel and SONET [1–5]. A conceptual example of serial data transmission over a fiber optic link is shown in Figure 1.1. To reduce interconnection hardware, only the data is transmitted over a single fiber. At the receiving end of the link, a clock recovery circuit generates the bit clock RCLK from the serial data stream V_{in}. The clock recovery circuit also samples V_{in} to retime the serial data with respect to the recovered clock.

In this application, the design tools presented in this book are relevant to determining how well we can perform the clock recovery function. The timing diagram in Figure 1.1 shows the ideal case when clock recovery is performed perfectly: There is no phase error in the recovered clock, and RCLK samples V_{in} at the exact center of the bit period. This gives the minimum bit error rate (BER). Any deviation of RCLK from the ideal will increase BER .

In reality, there will be both static ("phase offset") and dynamic ("phase jitter" or simply "jitter") phase errors in the recovered clock, which will degrade performance and increase the BER. Reducing the bit error rate is a

J.A. McNeill and D.S. Ricketts, *The Designer's Guide to Jitter in Ring Oscillators*,
The Designer's Guide Book Series, DOI: 10.1007/978-0-387-76528-0_1,

major motivation for reducing jitter in the recovered clock. This book will address techniques for describing and reducing dynamic phase errors; static phase errors are not considered.

Increased BER is not the only negative effect of jitter in serial data communication . In a system architecture including repeaters, where the recovered clock is also used as the reference for the transmit clock for a subsequent data link, clock jitter can increase at each stage of clock recovery. An increase in jitter reduces the number of links that can be cascaded before jitter becomes unacceptably large [6].

Note that in evaluating the BER performance of a data link, the end user must be concerned with many other possible influences on BER besides the jitter in the CDR block. Among other factors that can degrade system BER are power loss and dispersion in the optical fiber, inadequate optical power

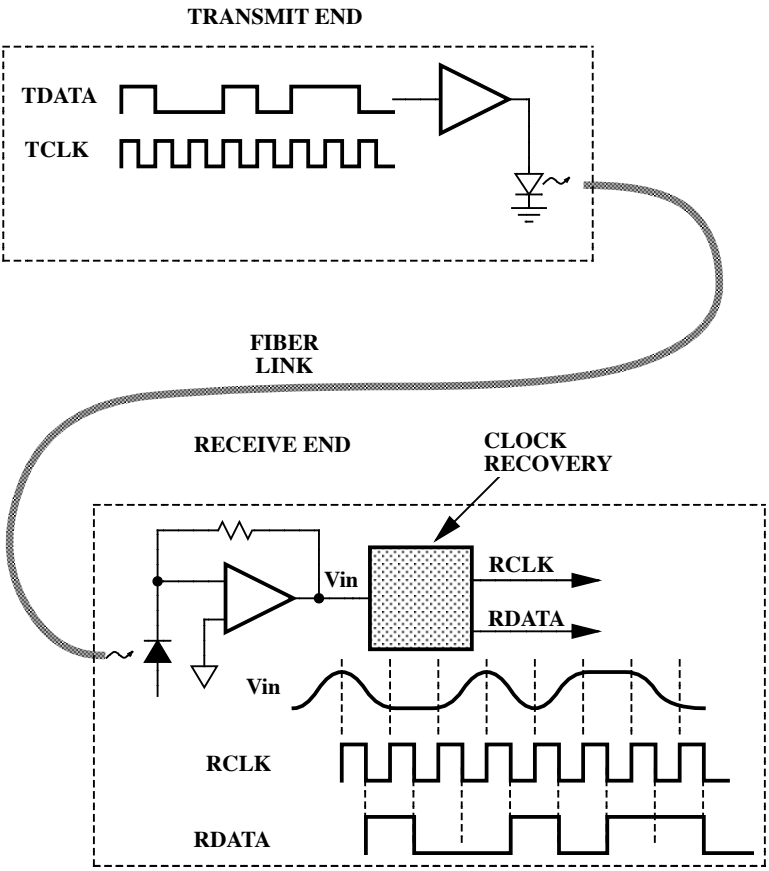


Fig. 1.1. Typical fiber optic serial data transmission system.

input at the transmit end, and noisy optical-to-electronic conversion at the receive end.

To assess the contribution of the clock recovery block to BER, the CDR function can be tested independently of the link, as shown in Figure 1.2. The input is an ideal data waveform; the recovered clock is then compared to the transmit clock in the time domain. Figure 1.3 is a typical measured waveform showing jitter in the threshold crossing of the recovered clock waveform. If there were no jitter, the phase difference between the clocks would be constant (due only to static phase and propagation delay differences). In the presence of jitter, there is a distribution of phase differences, approximated by the historgram shown in Figure 1.3. The standard deviation of this distribution σ_x is the end user's measure for characterizing the jitter performance of the clock recovery block in the time domain [7].

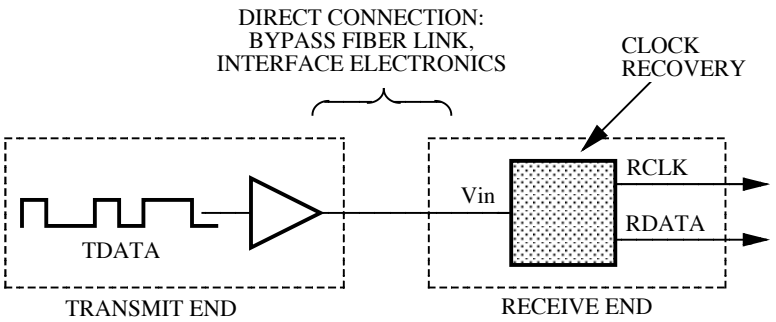


Fig. 1.2. Independent test of BER due to clock recovery function..

1.1.2 Methods of clock and data recovery

At moderate data rates, data can be recovered by oversampling the received signal to identify transitions in the data waveform [8]. At higher frequencies, however, techniques operating at or near the data rate are necessary. One method of recovering the bit clock is to apply the nonlinearly processed data waveform to a resonant circuit such as a surface acoustic wave (SAW) filter [9,10]. Nonlinear processing is required since a non-return-to-zero (NRZ) data waveform has a spectral null at the bit frequency [11]. The disadvantage of this approach is that SAW filters are incompatible with low cost IC fabrication technologies.

An alternative approach for generating the recovered clock is to use a phase-locked loop (PLL) [12–15]. This has the advantage of being integrable, and thus relatively inexpensive. This book will address techniques that can be applied to design for low jitter performance when a PLL is used for the clock recovery function. In Chapter 3, the example of the CDR system is examined

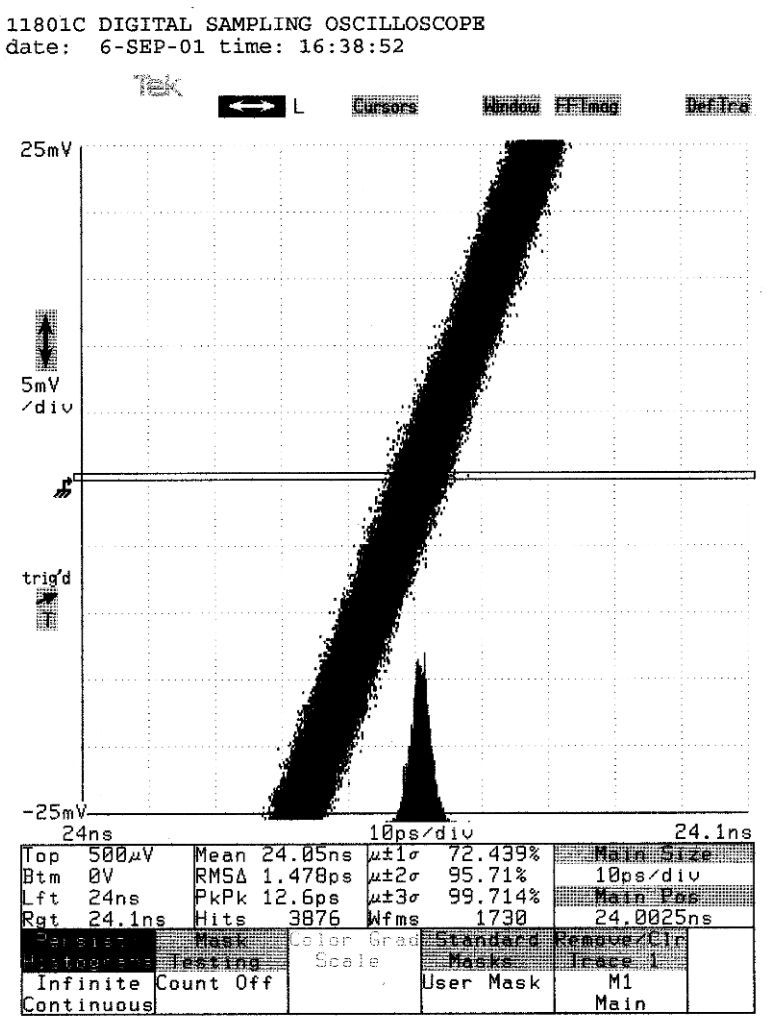


Fig. 1.3. Jitter on recovered clock waveform.

in more detail to show how performance is influenced by both circuit-level considerations such as jitter in the VCO as well as system-level considerations such as PLL loop bandwidth.

1.1.3 Other applications

Although the concepts in this book will be developed in the context of serial data transmission, there are several other applications requiring low jitter performance from PLLs:

Digital clock synthesis

Digital processors are capable of operating at clock rates of several GHz, but distributing such a high speed clock throughout a system is impractical if not impossible. One approach to solving this problem is to distribute a lower frequency clock, and multiply this clock to the higher frequency with an on-chip PLL [16–20]. Low jitter is necessary since any increase in jitter reduces timing margin for digital circuitry and signals that rely on the clock.

Serialize-Deserialize (SERDES)

To reduce the physical size of digital communication paths, a wide digital bus can be serialized to transmit data at higher speed [2]. At the receive end, data is recovered and demultiplexed to parallel form. Integrating SERDES solutions on chip allows substantial reduction in package pin count as well as in backplane interconnect. System issues are much the same as in the fiber optic transmission system; however, in the case of SERDES the physical channel is usually all electrical. Similar BER issues arise due to nonidealities in the physical transmission medium, for example, attenuation and dispersion in a backplane signal transmission path. Low jitter performance is necessary to ensure adequate BER for the SERDES function.

Frequency Synthesis

PLLs are widely used for frequency synthesis in RF communication systems. One example is shown in Figure 1.4, in which a PLL is used to generate local oscillator (LO) waveforms in signal modulation and demodulation [21, 22]. In this case, system performance is described in the frequency domain, relative to specifications such as adjacent channel interference and spurious power output. Figure 1.5 shows a typical measurement of an oscillator power spectrum. For an ideal waveform, the spectrum would be an impulse at a single frequency. The frequency domain manifestation of jitter is phase noise: the "skirts" of excess noise power at frequencies close to the ideal impulse.

Oversampling ADC clock synthesis

A PLL can be used to generate the high-speed clock required for delta-sigma A/D and D/A conversion in digital audio applications. Low jitter is necessary since phase noise on the clock can be aliased into the audio band to produce audible, objectionable artifacts in the reconstructed analog waveform [23, 24].

1.1.4 Summary

Many applications require low jitter PLL performance, characterized by time domain or frequency domain measures. The work in this book grew out of the need to develop tools for low jitter PLL design, while always being able to

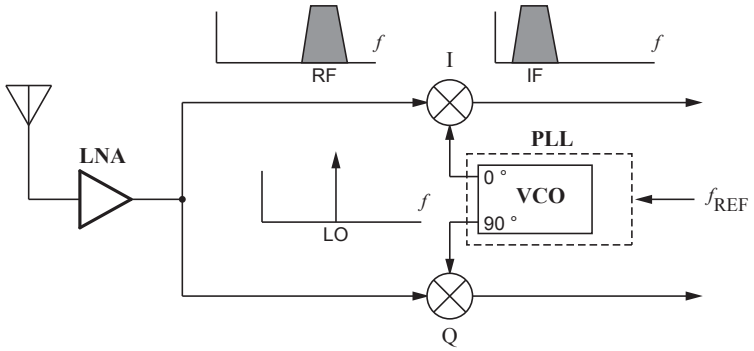


Fig. 1.4. Typical wireless communication system.

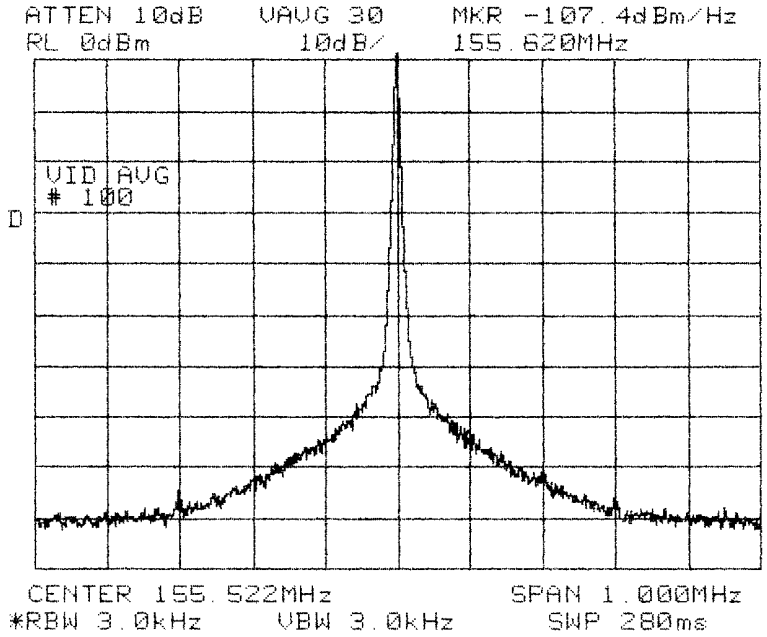


Fig. 1.5. Typical measurement of oscillator power spectrum.

relate circuit-level design decision to the end user's requirement for system-level jitter performance.

1.2 Types of VCOs

This section briefly describes different types of VCOs that are used in clock recovery and other PLLs. They will be discussed in more detail in Chapters 2, 6, and 7.

1.2.1 LC resonant

Figure 1.6 shows a conceptual LC resonant oscillator . The oscillation frequency is determined primarily by the resonance of an LC network (or equivalent, for example, a quartz crystal). Active circuitry stabilizes the oscillation amplitude and provides energy to balance losses in the L and C elements. Tuning is achieved by varying an element value, usually capacitance with a votlage controlled capacitance such as a varactor [25, 26]

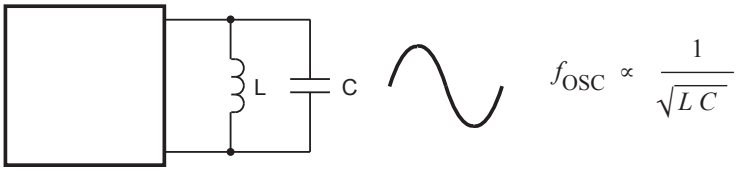


Fig. 1.6. Conceptual LC resonant oscillator.

VCOs based on a resonant circuit (such as an LC tank or quartz crystal) are known to have excellent jitter performance [27–30]. Analysis of noise in resonant-based VCOs is well developed in the literature [31–34], and design techniques for realizing low jitter performance are relatively well understood.

Use of an off-chip tank or crystal defeats the purpose of integrating the PLL function, so discussion in this section will be limited to integrable techniques. In the 100MHz to 1GHz frequency range, inductor values typically require an impractically large amount of die are to be integrated economically. Integrated inductors are practical in at frequencies in the GHz frequency range and above [35]. Typical Q values are of order 10 due to resistive and substrate losses. Even though higher frequencies will in general require lower inducatance values, die area may still be significant depending on metal options available in the process.

It will be seen in Chapter 7 that, for a given power dissipation, LC oscillators are inherently capable of better jitter performance than ring oscillators. For this reason, in the most demanding applications, the designer's options are limited to LC oscillators. However, for applications with moderate jitter requirements or in which die area is at a premium, avoiding integrated inductors and their associated die area consumption may be a reasonable option.

1.2.2 Multivibrator

Figure 1.7 shows a conceptual multivibrator oscillator, also sometimes alternatively known as a relaxation oscillator. In this example, active circuitry monitors the capacitor voltage and switches a reference current I_{REF} to charge and discharge the capacitor voltage between reference voltages $\pm V_{REF}$. The oscillation frequency is determined primarily by V_{REF}, I_{REF}, and the capacitor value. Tuning is achieved by varying one of these values, usually the current I_{REF} [13].

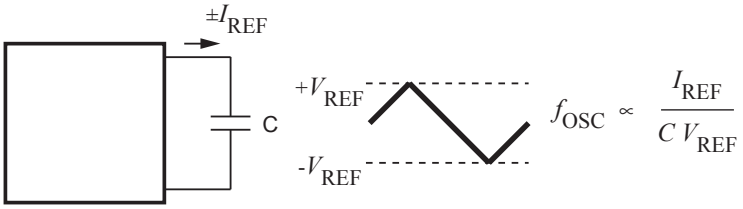


Fig. 1.7. Conceptual multivibrator oscillator.

A multivibrator oscillator VCO can be fully integrable. Much work on multivibrator VCOs has concentrated on their potential for excellent linearity [36–40], which is an important requirement when the PLL is being used for measurement or to demodulate a PM or FM signal. However, linearity is not as critical a requirement in clock recovery. Fully integrated clock recovery PLLs have been described using multivibrator VCOs [13, 41–44]. The jitter performance of multivibrators is known to be worse than harmonic oscillators. The literature contains some analysis of jitter in multivibrators [45–47], and some design techniques for improving jitter are available [48–51]. Nevertheless, there is a need for improvement of jitter beyond the best achieved by relaxation VCOs

1.2.3 Ring oscillator

For the ring oscillator, shown in conceptual form in Figure 1.8, the oscillation frequency is determined by the propagation delay t_{PD} of each stage in the ring. Controlling the stage delay t_{PD} provides control of the oscillator frequency.

Voltage controlled ring oscillators have been widely employed as an alternative to the multivibrator for fully integrated, lower jitter clock recovery PLLs [12, 20, 52–60] and in other applications as well [3]. Like the multivibrator, a ring oscillator is fully integrable. In addition, empirical results show promise of excellent jitter performance [58].

Several analyses of jitter in ring oscillators have been published in the literature [61–64]. The purpose of this book is to explore the issues associated

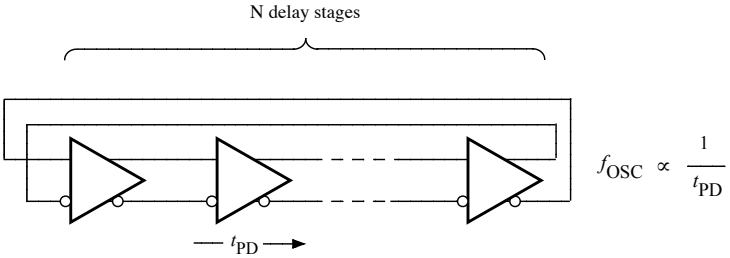


Fig. 1.8. Conceptual ring oscillator.

with low jitter design in greater detail, primarily from a time domain point of view, so that designers may realize a deeper understanding of the fundamental circuit-level mechanisms underlying jitter, and how to design to meet a given system-level jitter requirement.

1.3 Motivation and goals of this book

There are many applications for low jitter, PLL-based clock recovery. Fully integrated PLLs have a substantial cost and size advantage over PLLs requiring off-chip resonant elements. Ring oscillators offer the possibility of reduced die area relative to integrated inductor approaches in moderate jitter applications. The need is for an intuitive design methodology to predict and design for jitter in ring oscillators. Thus the primary goals of this book are:

Develop design tools for ring VCO jitter

This book will focus on techniques for designing ring oscillators to achieve a desired (low) jitter. In particular, this book will address design questions such as:

- How is jitter affected by the number of delay stages in the ring? That is, at a given frequency, which is better for low jitter: many fast delay stages, or fewer slow delay stages?
- Within the delay stage itself, what affects jitter? That is, how should circuit parameters (such as bias currents, resistor values, etc.) be chosen to achieve a given desired jitter?
- What are the fundamental limits on jitter that can be achieved? That is, is there any simple relationship between jitter and system-level considerations such as power dissipation or die area?

To ease design, the tools should also allow the designer flexibility to work in either the time or frequency domain, whichever gives the most insight; while

relating the effect of design decisions to the domain in which system performance is specified. For example, in the clock and data recovery application although σ_x is defined in the time domain, insight for guiding some design decisions (e.g., effects of the loop filter and aliasing of noise sources [50, 65]) is more apparent in the frequency domain.

Simulation of PLL jitter

Once we have a tentative design, it is desirable to have a simulation tool to verify the design before going to the expense of fabricating silicon. Although we have modeled the PLL as a linear system, the VCO itself is a nonlinear circuit. One approach to jitter simulation uses transient analysis with explicit noise sources [66], which is simpler to perform for the open loop VCO. Other loop components may be nonlinear as well, for example, the "bang-bang" phase detection used in some clock and data recovery applications [67–69]. Additionally, some RF simulators are specifically designed to simulate phase noise or jitter performance of oscillators [70–72]. In each case, it is beneficial if the designer is able to relate performance measures from the time and frequency domains.

Technique for relating time/frequency, open/closed loop jitter measures

A technique for relating performance measures between the time and frequency domains enables simplified design and simulation of a low jitter VCO. The difficulty is that design and simulation are easiest on the stand-alone, open loop VCO - where nonstationary noise precludes the use of transform tools to move between the time and frequency domains. The ultimate concern is the jitter of the closed loop PLL system. With this time/frequency technique the designer can work in whatever domain is easiest while still being able to accurately predict performance when measured by the end user.

Other benefits

Although the techniques in this book are developed for PLL ring VCO design, they are applicable to any oscillator with a $1/f^2$ phase noise power spectrum. This will be demonstrated in Chapter 7 where the time/frequency technique of Chapter 5 is applied to a harmonic oscillator spectrum and gives the same result as previous analyses in the literature.

This work also can be used to simplify evaluation of actual devices. For example, in a self-test mode, it is possible to open the PLL loop, set the VCO to a fixed frequency, and measure the stand alone, open loop VCO performance. From this measurement we can predict what the closed loop performance should be if limited only by the VCO jitter. Then we can compare this prediction with actual measurements to determine if other components (such as the phase detector or loop filter) are degrading the closed loop performance.

1.4 Chapter summary

This chapter has reviewed applications requiring a low jitter oscillator function. Performance may be specified in the time domain as jitter, or in the frequency domain as phase noise. A review of different types of oscillators shows that ring oscillators are of interest in many of these applications. The goal of this book is an intuitive methodology for ring oscillator design. The next step, in Chapter 2, is a survey of various techniques at the circuit level for realizing the ring VCO function. Moving up to the system level, a review of PLL system concepts and random process fundamentals is presented in Chapters 3 and 4. A simple technique for relating time/frequency, open/closed loop jitter measurements is developed in Chapter 5, as well as a discussion of instrumentation options for measuring jitter and phase noise performance. In Chapters 6-7, the time/frequency technique is used to develop design tools for ring VCOs at various levels of detail, resulting in a general methodology presented in Chapter 8. Example designs in both CMOS and bipolar processes are presented in Chapter 9. The applications of these principles to simulation is implicit in the results presented in Chapters 7-8, as well as in Appendix 7B.

2

Classification of ring oscillators

In this chapter we consider a classification of ring oscillators for the purpose of evaluating different oscillators in the literature, and guiding designers in choosing an architecture that will meet the needs of a particular system for both functionality and jitter performance.

In this approach, oscillators are characterized by

- Type of signal in the ring
- Method of tuning
- Format of signal(s) at output of the ring

In each case, examples will be used to illustrate the various classifications. Qualitative observations will also be made regarding the advantages and disadvantages of each approach with regard to performance aspects such as jitter, immunity to power supply noise, tuning range, etc. Quantitative analysis will be covered in detail in Chapter 7.

Note that this system is not intended to be exhaustive or exclusive. It is not exhaustive in the sense that not all ring oscillators can be classified by this system; however, the majority of work in the literature can be covered by this scheme. It is not intended to be exclusive in that other schemes for organizing types of oscillators may be useful; however, the authors believe this scheme is useful for illustrating in a straightforward way the differences between design approaches .

2.1 Type of signal in the ring

The first aspect of classification is by the type of signal in the ring delay stage. We identify three general types:

- Single-ended
- True differential
- Pseudo differential