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Preface

The objective of this book is to provide a systematic and comprehensive insight into the design of integrated chip-scale power supplies. The focus is on miniaturized power supplies that run from the 120 V / 230 V mains supply or high-voltage DC sources of up to 400 V to power various low-voltage subsystems. Applications include sensor nodes, transmitters, receivers, actuators as well as auxiliary supplies in power electronics with supply voltages of 3.3 V to 10 V at power levels of up to 500 mW. Conventionally, these applications are supplied from batteries with the expense of high maintenance. Alternatively, energy harvesting would be suitable but has limited output power. Commercial power modules are relatively large and expensive, and suffer from poor conversion efficiency at power levels below 500 mW. Consequently, there is a gap in solutions for highly efficient and compact power supplies.

This book covers solutions on system and circuit level for isolated and non-isolated low-power-optimized high-voltage converters in standard high-voltage silicon-on-insulator (SOI) technologies. The implemented converters are not only suitable for all common AC grid voltages (120 V / 230 V) but also for a wide DC input-voltage range of 12.5 V to 400 V. Their high voltage-conversion ratios of up to 120 make them well-suitable for low-power target applications. Together with the presented low-power optimized subcircuits, innovative control techniques, and layout / technology optimizations, peak efficiencies of up to 84% are achieved.

The book deals in detail with the following main topics: (1) Low-power optimized high-voltage converter architectures and control approaches are evaluated for high voltage-conversion ratios. They enable a high converter efficiency over the whole targeted input-voltage and output-power range at a compact size. (2) Low-power subcircuits are presented for a reliable converter operation with a high common-mode-transient immunity at low steady-state losses and low high-voltage-related capacitive and resistive losses. (3) A comprehensive analysis enables the size and loss reduction of the power inductor and transformer. An active zero-crossing buffer is described to reduce the size of the mandatory buffer capacitor in the AC interface. (4) Design techniques in SOI technologies are presented. It includes capacitive-loss-reduction techniques to reduce high-voltage-related capac-

itive losses to a minimum. Techniques for a reduction of substrate coupling as one major disturbance mechanism are explained. The performance of state-of-the-art on-chip high-voltage power switches is analyzed to enable a size and loss reduction by selecting a well-suited power-switch type for each converter architecture.

The book is intended as a comprehensive all-in-one source on the design of chip-scale high-voltage power supplies for low-power DC-link and grid applications. It is written in handbook style with systematic guidelines, including many implementation examples. It covers the full range from technology fundamentals to circuit implementation details. It includes guidelines for the application-specific selection of the converter topology, design guidelines for the inductive components, and a detailed description of low-power optimized control approaches and subcircuits.

This book is based on our research at the Institute for Microelectronic Systems at Leibniz University Hannover, Hannover, Germany. We are grateful to many team members at the university as well as to our industry partners.

A special thanks goes to our families; without their love and support, this book would not have been possible.

Dresden, Germany — Christoph Rindfleisch
Hannover, Germany — Bernhard Wicht
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Contents

Acronyms

List of Abbreviations

ADC	Analog-to-Digital Converter
BCM	Boundary-Conduction Mode
BOX	Buried Oxide
BUR	Buried Layer
CCM	Continuous-Conduction Mode
CMOS	Complementary Metal-Oxide-Semiconductor
CMTI	Common-Mode-Transient Immunity
DCM	Discontinuous-Conduction Mode
DTI	Deep-Trench Isolation
EMI	Electromagnetic Interference
GaN	Gallium Nitrite
HSGND	High-Side Ground
HV	High Voltage
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
IoT	Internet of Things
IR	Infrared
LCD	Liquid-Crystal Display
LDMOS	Lateral Double-Diffused MOSFET
LED	Light-Emitting Diode
MIM	Metal-Insulator-Metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	n-Type MOSFET
PCB	Printed-Circuit Board
PMOS	p-Type MOSFET
PWM	Pulse-Width Modulated Signal
RESURF	Reduced Surface Field
RF	Radio Frequency

SC	Switched Capacitor
SiC	Silicon Carbide
SJ-LIGBT	Lateral Super-Junction IGBT
SJ-MOSFET	Lateral Super-Junction MOSFET
SMD	Surface-Mounted Device
SMU	Source Measurement Unit
SOI	Silicon on Insulator
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Symbols

$A_{\mathrm{e,core}}$	m^2	Effective Cross-sectional Area of a Magnetic Core
AL	H	Inductance Rating of a Magnetic Core per $N_{L\mathrm{p}}^2$
A_{wire}	m^2	Cross-sectional Area of a Wire
B_{core}	Gs	Magnetic Flux Density in a Magnetic Core
$B_{\mathrm{core,max}}$	Gs	Maximum Value of B_{core}
$B_{\mathrm{core,min}}$	Gs	Minimum Value of B_{core}
$B_{\mathrm{core,peak}}$	Gs	Peak Value of B_{core}
$B_{\mathrm{sat,core}}$	Gs	Magnetic Saturation Flux Density of a Magnetic Core
BU		Buffer
C_{BOX}	F	Capacitance Across the Buried Oxide
$C_{\mathrm{BOX,J}}$	F	Total Capacitance of C_{Box} in Series to C_{J}
C_{bst}	F	Bootstrap Capacitor
C_{buf}	F	Buffer Capacitor
$C_{\mathrm{CA,Dbst}}$	F	Cathode-Anode Capacitance of $\mathrm{D_{bst}}$
C_{clp}	F	Clamp Capacitor
$C_{\mathrm{CP,1}}$	F	Charge-Pump Capacitor Number One
$C_{\mathrm{CP,2}}$	F	Charge-Pump Capacitor Number Two
C_{cpl}	F	Coupling Capacitance
C_{d}	F	Capacitor of an RC-Delay Gate
C_{DG}	F	Drain-Gate Capacitance of a Transistor
C_{DS}	F	Drain-Source Capacitance of a Transistor
C_{DTI}	F	Capacitance Across the Deep Trench
$C_{\mathrm{DTI,total}}$	F	Total Capacitance Across Multiple Deep Trenches
C_{f}	F	Filter Capacitor
C_{fb}	F	Primary-Side Capacitor of a Fly-Buck Converter
C_{fly}	F	Flying Capacitor of an SC / a Multi-level Converter
$C_{\mathrm{fly,1}}$	F	First Flying Capacitor of an SC / a Multi-level Converter
$C_{\mathrm{fly},n}$	F	nth Flying Capacitor of an SC / a Multi-level Converter
C_{in}	F	Input Buffer Capacitor
$C_{\mathrm{in,AC-AC}}$	F	Input Capacitor of a Capacitive Voltage Divider

C_{iso}	F	Capacitor Used for the Signal Isolation
C_{J}	F	Junction Capacitance
C_{m}	W	First Steinmetz Parameter
$C_{\mathrm{MET-MET}}$	F	Capacitance Between Different Metal Layers
$C_{\mathrm{MET-SUB}}$	F	Capacitance Between Metal Layers and the Substrate
C_{off}	F	Coupling Capacitor in the Turn-Off Path
C_{on}	F	Coupling Capacitor in the Turn-On Path
C_{out}	F	Output Buffer Capacitor
C_{par}	F	Parasitic Capacitance
$C_{\mathrm{par,CEqv}}$	F	Charge-Equivalent Value of C_{par}
$C_{\mathrm{par,EEqv}}$	F	Energy-Equivalent Value of C_{par}
$C_{\mathrm{par,sub}}$	F	Parasitic Capacitance Towards the Substrate
C_{res}	F	Resonant Capacitor
$C_{\mathrm{sht,AC-AC}}$	F	Shunt Capacitor of a Capacitive Voltage Divider
C_{snub}	F	Snubber Capacitor
D		Diode
D		Duty Cycle
D-FF		Delay Flip-Flop
d_1	s	Delay One
d_2	s	Delay Two
d_3	s	Delay Three
d_4	s	Delay Four
$\mathrm{D_{bst}}$		Bootstrap Diode
$\mathrm{D_{clp}}$		Clamp Diode
$\mathrm{D_{CP,1}}$		Charg-Pump Diode Number One
$\mathrm{D_{CP,2}}$		Charg-Pump Diode Number Two
$\mathrm{D_{HV,1}}$		HV Power Diode Number One
$\mathrm{D_{HV,2}}$		HV Power Diode Number Two
$\mathrm{D_{HV,buf}}$		HV Diode of the Active Zero-Crossing Buffer
$\mathrm{D_{HV,out}}$		HV Freewheeling Power Diode of the Output Filter
$d_{\mathrm{i,core}}$	m	Inner Diameter of a Toroidal Core
$d_{\mathrm{o,core}}$	m	Outer Diameter of a Toroidal Core
$\mathrm{D_{out}}$		Freewheeling Power Diode of the Output Filter
$\mathrm{D_{ovp}}$		Over-Voltage-Protection Diode
$\mathrm{D_{rtf,1}}$		Rectifier Diode Number One
$\mathrm{D_{rtf,2}}$		Rectifier Diode Number Two
$\mathrm{D_{rtf,3}}$		Rectifier Diode Number Three
$\mathrm{D_{rtf,4}}$		Rectifier Diode Number Four
d_{sb}	s	Delay Until the Snubber is Turned On Again
$\mathrm{D_{uvp}}$		Under-Voltage-Protection Diode
$\mathrm{d}V/\mathrm{d}t$	V/s	Slew Rate
d_{wire}	m	Diameter of a Wire
$d_{\mathrm{wire,max}}$	m	Maximum Value of d_{wire}
$\mathrm{D_Z}$		Zener Diode

$D_{Z,clp}$		Zener Diode of the Passive Clamp
$D_{Z,ref}$		Reference Zener Diode
$E_{Cbuf,init}$	W s	Energy That is Initially Stored in C_{buf}
$E_{Cbuf,rem}$	W s	Energy That Remains in C_{buf} After t_{buf}
E_{clp}	W s	Energy Transferred to $C_{clp}/D_{Z,\,clp}$ During the Clamping
E_{Cout}	W s	Energy Transferred to C_{out} While HV1 is Turned On
$E_{Cres,max}$	W s	Peak Value of the Energy Stored in C_{res}
E_{crit}	V/m	Critical Electric Field Strength
E_{LmTp}	W s	Energy Transferred to L_m, T_p While HV1 is Turned On
E_{load}	W s	Energy Consumed by the Load
$E_{loss,charge}$	W s	Energy Loss at Charging
$E_{loss,core}$	W s	Core Loss per Switching Cycle
$E_{loss,discharge}$	W s	Energy Loss at Discharging
E_{Lp}	W s	Energy Transferred to L_p While HV1 is Turned On
E_{out}	W s	Energy Transferred to the Output
$E_{out,clp}$	W s	Energy Transferred to the Output During the Clamping
$E_{out,Llk,s,Tp}$	W s	Energy Transferred from $L_{lk,\,s,\,Tp}$ to the Output
$E_{out,Lm,Tp}$	W s	Energy Transferred from $L_{m,\,Tp}$ to the Output
E_{surf}	V/m	Field Strength Along the Surface of a Semiconductor
E_x	V/m	Electric Field Strength in x-Direction
f	Hz	Frequency
f_c	Hz	Frequency of the Current
f_{clk}	Hz	Clock Frequency
$f_{cut-off}$	Hz	Cut-Off Frequency
f_{eqv}	Hz	Equiv. Frequency of the Modified Steinmetz Equation
f_{grid}	Hz	Grid Frequency
f_{max}	Hz	Maximum Frequency
f_{res}	Hz	Resonant Frequency
FS-A		Input AND Gate of the Fault-Signal-Detection Circuit
f_{sw}	Hz	Switching Frequency
$f_{sw,max}$	Hz	Maximum Value of f_{sw}
h_{core}	m	Height of a Toroidal Core
H_{core}	A/m	Magnetic Field Strength in a Magnetic Core
$H_{core,Isat}$	A/m	$B_{sat,\,core}$-Dependent Maximum Value of H_{core}
H_{Iwire}	A/m	Magnetic Field Induced by I_{wire}
HS-BU		Buffer at the High Side
$HS\text{-}BU_{off}$		HS-BU for the Detection of the Turn-Off Signal
$HS\text{-}BU_{on}$		HS-BU for the Detection of the Turn-On Signal
HS-INV		Inverter at the High Side
$HS\text{-}INV_{off}$		HS-INV for the Detection of the Turn-Off Signal
$HS\text{-}INV_{on}$		HS-INV for the Detection of the Turn-On Signal
HS-SR		High-Side Shift Register
HV1		HV Power Switch Number One
$HV1_a$		HV Power Switch Number One a
$HV1_b$		HV Power Switch Number One b

$HV1_{rtf}$		HV Power Switch of the Rectifier Number One
$HV1_{\phi 1}$		HV Power Switch Number One of Phase One
$HV1_{\phi 2}$		HV Power Switch Number One of Phase Two
HV2		HV Power Switch Number Two
$HV2_{a}$		HV Power Switch Number Two a
$HV2_{b}$		HV Power Switch Number Two b
$HV2_{rtf}$		HV Power Switch of the Rectifier Number Two
$HV2_{\phi 1}$		HV Power Switch Number Two of Phase One
$HV2_{\phi 2}$		HV Power Switch Number Two of Phase Two
$HV3_{rtf}$		HV Power Switch of the Rectifier Number Three
$HV4_{rtf}$		HV Power Switch of the Rectifier Number Four
HV_{buf}		HV Power Switch of the Active Zero-Crossing Buffer
HV_{clp}		HV Clamp Switch
HVn_{a}		HV Power Switch Number na
HVn_{b}		HV Power Switch Number nb
I-FF		Initialization Flip-Flop
$I_{C\text{fly}}$	A	Current Through C_{fly}
I_{clp}	A	Current Through the Clamp
$I_{C\text{out}}$	A	Current Through C_{out}
I_{Dbst}	A	Current Through D_{bst}
$I_{\text{DHV,out}}$	A	Current Through $D_{\text{HV, out}}$
I_{eddy}	A	Eddy Current
I_{HV2}	A	Current Through the Drain of HV2
I_{in}	A	Input Current
I_{leak}	A	Leakage Current
$I_{L\text{lk,p,Tp}}$	A	Current Through $L_{\text{lk, p, Tp}}$
$I_{L\text{lk,s,Tp}}$	A	Current Through $L_{\text{lk, s, Tp}}$
$I_{L\text{m,Tp}}$	A	Current Through $L_{\text{m, Tp}}$
$I_{L\text{m,Tp,max}}$	A	Peak Value of $I_{L\text{m,Tp}}$
$I_{L\text{p}}$	A	Current Through L_{p}
$I_{L\text{p,DC}}$	A	DC Value of $I_{L\text{p}}$
$I_{L\text{p,max}}$	A	Peak Value of $I_{L\text{p}}$
I_{Mclp}	A	Current Through M_{clp}
I_{Ms}	A	Current Through M_{s}
I_{out}	A	Output Current
I_{p}	A	Current at the Primary Side of T_{p}
I_{par}	A	Parasitic Coupling Current
$I_{\text{par,max}}$	A	Maximum Value of I_{par}
I_{pu}	A	Pull-Up Current
I_{R}	A	Current Through R
I_{s}	A	Current at the Secondary Side of T_{p}
$I_{\text{sat},L\text{m,Tp}}$	A	Saturation Current of $L_{\text{m, Tp}}$
$I_{\text{sat},L\text{p}}$	A	Saturation Current of L_{p}
$I_{\text{sat,Ms}}$	A	Saturation Current of M_{s}
I_{snub}	A	Current Through the Snubber

I_{sub}	A	Parasitic Current Through the Substrate
I_{wire}	A	Current Through a Wire
$J_{\text{s,wire}}$	A/m^2	Surface Current Density of a Wire
J_{wire}	A/m^2	Current Density in a Wire
L	m	Device Length
$l_{\text{e,core}}$	m	Effective Magnetic Path Length of a Magnetic Core
LS − SR		Low-Side Shift Register
$L_{\text{lk,p,Tp}}$	H	Primary-Side Leakage Inductance of T_p
$L_{\text{lk,s,Tp}}$	H	Secondary-Side Leakage Inductance of T_p
$L_{\text{m,Tp}}$	H	Primary-Side Inductance of T_p
L_p	H	Power Inductor
LV1		Low-Voltage Power Switch Number One
LV2		Low-Voltage Power Switch Number Two
l_{winding}	m	Circumference of the Winding Layer
l_{wire}	m	Total Length of the Wire
M-FF		Mode-Saving Flip-Flop
M_clp		Clamp Transistor
M_pd		Pull-Down Transistor
$\text{M}_\text{pd,off}$		M_pd in the Turn-Off Path
$\text{M}_\text{pd,on}$		M_pd in the Turn-On Path
M_pu		Pull-Up Transistor
$\text{M}_\text{pu,off}$		M_pu in the Turn-Off Path
$\text{M}_\text{pu,on}$		M_pu in the Turn-On Path
M_ref		Transistor for the Generation of a Reference Voltage
M_rr		Transistor for the Reverse-Recovery-Loss Reduction
M_s		Transistor for the Signal Transmission
$\text{M}_\text{s,off}$		M_s in the Turn-Off Path
$\text{M}_\text{s,on}$		M_s in the Turn-On Path
M_shunt		Shunt Transistor of a Shunt Regulator
M_snub		Snubber Transistor
N_i	1	Intrinsic Voltage-Conversion Ratio of an SC Converter
$N_{L\text{p}}$	1	Number of Windings of L_p
$N_{L\text{p,max}}$	1	Maximum Value of $N_{L\text{p}}$
N_{Tp}	1	Winding Ratio Between Primary and Secondary Side
P-FF		Phase-Saving Flip-Flop
P_in	W	Input Power
P_loss	W	Power Loss
$P_{\text{loss,accum,}L\text{p}}$	W	Accumulated Power Loss Caused by L_p
$P_{\text{loss,}C\text{BOX}}$	W	Power Loss Caused by C_BOX
$P_{\text{loss,}C\text{DS}}$	W	Power Loss Caused by C_DS
$P_{\text{loss,}C\text{DTI}}$	W	Power Loss Caused by C_DTI
$P_{\text{loss,charge}}$	W	Power Loss During Charging
$P_{\text{loss,clp}}$	W	Power Loss Caused by $L_{\text{lk, p, Tp}}$ and $L_{\text{lk, s, Tp}}$
$P_{\text{loss,core}}$	W	Power Loss in a Magnetic Core

$P_{\mathrm{loss},C\mathrm{par}}$	W	Power Loss Caused by C_{par}
$P_{\mathrm{loss,discharge}}$	W	Power Loss During Discharging
$P_{\mathrm{loss},L\mathrm{p}}$	W	Power Loss Caused by L_{p}
$P_{\mathrm{loss,LR}}$	W	Power Loss in a Linear Regulator
$P_{\mathrm{loss},R,\mathrm{cur}}$	W	Current-Related Resistive Power Loss
$P_{\mathrm{loss},R,\mathrm{HV}}$	W	HV-Related Resistive Power Loss
$P_{\mathrm{loss,total},L\mathrm{p}}$	W	Total Power Loss Caused by L_{p}
P_{out}	W	Output Power
$P_{\mathrm{out,max}}$	W	Maximum Value of P_{out}
Q_{buf}	A s	Charge Delivered to V_{buf}
$Q_{C\mathrm{CP},1}$	A s	Charge Stored in $C_{\mathrm{CP},\,1}$
$Q_{C\mathrm{CP},2}$	A s	Charge Stored in $C_{\mathrm{CP},\,2}$
$Q_{C\mathrm{in,AC-AC}}$	A s	Charge Transferred to $C_{\mathrm{in},\,\mathrm{AC}-\mathrm{AC}}$
$Q_{\mathrm{circ,HS}}$	A s	Charge Stored in C_{par}
Q_{clp}	A s	Charge Transferred to C_{clp} or $\mathrm{D}_{\mathrm{Z},\,\mathrm{clp}}$ During Clamping
$Q_{C\mathrm{out}}$	A s	Charge Transferred to C_{out} While HV1 is Turned On
$Q_{C\mathrm{par}}$	A s	Charge Stored in C_{par}
$Q_{C\mathrm{sht,AC-AC}}$	A s	Charge Transferred to $C_{\mathrm{sht},\,\mathrm{AC}-\mathrm{AC}}$
$Q_{\mathrm{G,PS}}$	A s	Gate Charge of a Power Transistor
Q_{out}	A s	Charge Transferred to the Output in Each Phase
$Q_{\mathrm{rr,Dbst}}$	A s	Reverse-Recovery Charge of $\mathrm{D}_{\mathrm{bst}}$
$Q_{\phi 1}$	A s	Charge Transfered to C_{fly} in Phase One
$Q_{\phi 2}$	A s	Charge Transfered to C_{fly} in Phase Two
R	Ω	Resistor
R_1	Ω	Resistor One of a Voltage Divider
R_2	Ω	Resistor Two of a Voltage Divider
R_{ch}	Ω	Resistance in the Channel of a Transistor
R_{clp}	Ω	Clamp Resistor
R_{d}	Ω	Resistor of an RC-Delay Gate
$R_{\mathrm{DC,wire}}$	Ω	DC Resistance of a Wire
R_{drift}	Ω	Resistance in the Drift-Region of a Transistor
R_{load}	Ω	Load Resistor
R_{LR}	Ω	Variable Series Resistor of a Linear Regulator
R_{on}	Ω	On-Resistance
$R_{\mathrm{on,Mpu}}$	Ω	On-Resistance of M_{pu}
R_{osc}	Ω	Reference-Current Resistor of the Oscillator
R_{out}	Ω	Equivalent Output Resistance of an SC Converter
$R_{\mathrm{out,min}}$	Ω	Lowest Achievable Value of R_{out}
R_{p}	Ω	Permanent Losses in an SC Converter
R_{par}	Ω	Parasitic Resistor
R_{pu}	Ω	Pull-Up Resistor
R_{s}	Ω	Sensing Resistor
$R_{\mathrm{skin,wire}}$	Ω	Skin-Effect-Related AC Resistance of a Wire
R_{snub}	Ω	Snubber Resistor
S-FF		State-Saving Flip-Flop

SR	V/s	Slew Rate
SR-FF		Set-Reset Flip-Flop
s_{winding}	m	Spacing Between First and Last Turn of the Winding
t	s	Time
t_1	s	Point of Time Number One
t_2	s	Point of Time Number Two
t_3	s	Point of Time Number Three
t_4	s	Point of Time Number Four
t_5	s	Point of Time Number Five
t_6	s	Point of Time Number Six
t_7	s	Point of Time Number Seven
t_8	s	Point of Time Number Eight
t_{A}	s	Point of Time Number A
t_{B}	s	Point of Time Number B
t_{buf}	s	Buffer Time
$t_{\text{buf,1}}$	s	Buffer Time Number One
$t_{\text{buf,2}}$	s	Buffer Time Number Two
$t_{\text{buf,max}}$	s	Maximum Value of t_{buf}
$t_{\text{buf,min}}$	s	Minimum Value of t_{buf}
t_{clp}	s	Duration of the Clamping
t_{dead}	s	Dead Time Between Two Signals
$t_{\text{off,HV1}}$	s	Off-Time of HV1
t_{on}	s	On-Time of a Power Switch
$t_{\text{on,HV1}}$	s	On-Time of HV1
$t_{\text{on,HV1,max}}$	s	Maximum Value of $t_{\text{on, HV1}}$
$t_{\text{on,HV1,min}}$	s	Minimum Value of $t_{\text{on, HV1}}$
$t_{\text{on,HV2}}$	s	On-Time of HV2
$t_{\text{on,HV2,max}}$	s	Maximum Value of $t_{\text{on, HV2}}$
$t_{\text{on,HV2,min}}$	s	Minimum Value of $t_{\text{on, HV2}}$
$t_{\text{on,HVclp}}$	s	On-Time of HV_{clp}
$t_{\text{overshoot}}$	s	Duration Until $V_{\text{overshoot}}$ is Reached
T_p		Power Transformer
t_{pd}	s	Propagation Delay
$t_{\text{pd,off}}$	s	Propagation Delay at Turn-Off
$t_{\text{pd,on}}$	s	Propagation Delay at Turn-On
t_{stl}	s	Settling Time
$t_{\text{stl,min}}$	s	Minimum Settling Time
V	V	Voltage
V_{A}	V	Voltage Number A
V_{B}	V	Voltage Number B
V_{buf}	V	Buffered Voltage
$V_{\text{buf,min}}$	V	Minimum Value of V_{buf}
V_{BUR}	V	Voltage Across C_J
$V_{C\text{clp}}$	V	Voltage Across C_{clp}
$V_{C\text{CP,1}}$	V	Voltage Across $C_{\text{CP, 1}}$

$V_{C\mathrm{CP,2}}$	V	Voltage Across $C_{\mathrm{CP,\,2}}$
V_{CE}	V	Collector-Emitter Voltage
$V_{C\mathrm{fly}}$	V	Voltage Across C_{fly}
$V_{C\mathrm{fly},1}$	V	Voltage Across $C_{\mathrm{fly,\,1}}$
$V_{C\mathrm{fly},n}$	V	Voltage Across $C_{\mathrm{fly,\,n}}$
$V_{C\mathrm{fly},\phi 1}$	V	Steady-State Voltage Across C_{fly} in Phase One
$V_{C\mathrm{fly},\phi 2}$	V	Steady-State Voltage Across C_{fly} in Phase Two
V_{clp}	V	Clamp Voltage
$V_{C\mathrm{par}}$	V	Voltage Across C_{par}
$V'_{C\mathrm{par}}$	V	Voltage Across C_{par} in the Simplified Equivalent Circuit
VCR	1	Voltage-Conversion Ratio
VCR_{min}	1	Lowest Achievable Value of VCR
$V_{C\mathrm{res}}$	V	Voltage Across C_{res}
$V_{C\mathrm{sht,AC-AC}}$	V	Voltage Across $C_{\mathrm{sht,\,AC\,-\,AC}}$
V_{Dbst}	V	Forward-Conduction Voltage of $\mathrm{D_{bst}}$
V_{DCP1}	V	Forward-Conduction Voltage of $\mathrm{D_{CP,\,1}}$
V_{DCP2}	V	Forward-Conduction Voltage of $\mathrm{D_{CP,\,2}}$
V_{DD}	V	Supply Voltage at the Low Side
V'_{DD}	V	Input Voltage of the Voltage Regulator at the High Side
$V_{\mathrm{DD,HS}}$	V	Supply Voltage at the High Side
$V_{\mathrm{DD,HS,min}}$	V	Minimum Value of $V_{\mathrm{DD,\,HS}}$
$V_{\mathrm{DD,HS,nom}}$	V	Nominal Value of $V_{\mathrm{DD,\,HS}}$
V_{DHVout}	V	Forward-Conduction Voltage of $\mathrm{D_{HV,\,out}}$
V_{DS}	V	Drain-Source Voltage
$V_{\mathrm{DS,max}}$	V	Maximum Value of V_{DS}
$V_{\mathrm{G,Mclp}}$	V	Gate Voltage of $\mathrm{M_{clp}}$
$V_{\mathrm{G,Mrr}}$	V	Gate Voltage of $\mathrm{M_{rr}}$
$V_{\mathrm{GS,HV1}}$	V	Gate-Source Voltage of HV1
$V_{\mathrm{GS,HV1rtf}}$	V	Gate-Source Voltage of $\mathrm{HV1_{ref}}$
$V_{\mathrm{GS,HV2}}$	V	Gate-Source Voltage of HV2
$V_{\mathrm{GS,HVclp}}$	V	Gate-Source Voltage of $\mathrm{HV_{clp}}$
V_{HSGND}	V	Voltage at HSGND
$V_{\mathrm{HSGND,min}}$	V	Minimum Value of V_{HSGND}
V_{in}	V	Input Voltage
V'_{in}	V	Scaled Input Voltage
$V_{\mathrm{in,AC}}$	V	AC Input Voltage
$V_{\mathrm{in,AC,peak}}$	V	Peak Value of $V_{\mathrm{in,\,AC}}$
$V_{\mathrm{in,AC,RMS}}$	V	Root-Mean-Square of $V_{\mathrm{in,\,AC}}$
$V_{\mathrm{in,DC}}$	V	DC Input Voltage
$V_{\mathrm{in,DC,max}}$	V	Maximum Value of $V_{\mathrm{in,\,DC}}$
$V_{\mathrm{in,max}}$	V	Maximum Value of V_{in}
$V_{\mathrm{in,min}}$	V	Minium Value of V_{in}
$V_{L\mathrm{p}}$	V	Voltage Across L_{p}
$V_{L\mathrm{p,FFT}}$	V	Fourier Transform of $V_{L\mathrm{p}}$

V_{mag}	V	Magnetizing / Demagnetizing Voltage
$V_{\mathrm{mag},L\mathrm{lk,p,Tp}}$	V	Magnetizing / Demagnetizing Voltage of $L_{\mathrm{lk,\,p,\,Tp}}$
$V_{\mathrm{mag},L\mathrm{lk,s,Tp}}$	V	Magnetizing / Demagnetizing Voltage of $L_{\mathrm{lk,\,p,\,Tp}}$
V_{nhw}	V	Control Signal of $\mathrm{HV2_{rtf}}$ and $\mathrm{HV3_{rtf}}$
$Vol_{L\mathrm{p}}$	$\mathrm{m^3}$	Volume of L_{p}
V_{out}	V	Output Voltage
V'_{out}	V	Scaled Output Voltage
$V_{\mathrm{out,min}}$	V	Minium Value of V_{out}
$V_{\mathrm{out},N\mathrm{i}}$	V	Intrinsic Output Voltage of an SC Converter
$V_{\mathrm{overshoot}}$	V	Overshoot Voltage During Turn-Off of a Power Switch
V_{phw}	V	Control Signal of $\mathrm{HV1_{rtf}}$ and $\mathrm{HV4_{rtf}}$
V_{ref}	V	Reference Voltage
V_{ring}	V	Oscillating Voltage Across C_{par}
$V_{R\mathrm{LR}}$	V	Voltage Drop Across R_{LR}
$V_{R\mathrm{s,max}}$	V	Maximum Voltage Across R_{s}
V_{rtf}	V	Rectified Voltage
$V_{\mathrm{rtf,max}}$	V	Maximum Value of V_{rtf}
V_{S}	V	Source Voltage
$V_{\mathrm{S,HV1}}$	V	Source Voltage of HV1
V_{sw}	V	Voltage at the Switching Node
V_{th}	V	Threshold Voltage
$V_{\mathrm{th,HS\text{-}BU}}$	V	Threshold Voltage of $\mathrm{HS-BU}$
$V_{\mathrm{th,HS\text{-}BU,on/off}}$	V	Threshold Voltage of $\mathrm{HS-BU_{on}}$ and $\mathrm{HS-BU_{off}}$
$V_{\mathrm{th,HS\text{-}INV,on/off}}$	V	Threshold Voltage of $\mathrm{HS-INV_{on}}$ and $\mathrm{HS-INV_{off}}$
$V_{\mathrm{th,Mclp}}$	V	Threshold Voltage of $\mathrm{M_{CLP}}$
$V_{\mathrm{th,mode}}$	V	Threshold Voltage for the Mode Change
V_{Z}	V	Breakdown Voltage of a Zener Diode
$V_{\phi 1}$	V	Gate-Source Voltage of $\mathrm{HV1}_{\phi 1}$ and $\mathrm{HV2}_{\phi 1}$
$V_{\phi 2}$	V	Gate-Source Voltage of $\mathrm{HV1}_{\phi 2}$ and $\mathrm{HV2}_{\phi 2}$
W	m	Device Width
W_{ch}	m	Channel Width
w_{core}	m	Width of the Cross-Sectional Area of a Toroidal Core
$Z_{L\mathrm{p}}$	Ω	Impedance of L_{p}
α	1	Second Steinmetz Parameter
β	1	Third Steinmetz Parameter
δ	m	Skin Depth
$\Delta I_{L\mathrm{m,Tp}}$	A	Ripple-Current Through $L_{\mathrm{m,\,Tp}}$
$\Delta I_{L\mathrm{m,Tp},t\mathrm{off,HV1}}$	A	Ripple-Current Through $L_{\mathrm{m,\,Tp}}$ Caused During $t_{\mathrm{off,\,HV1}}$
$\Delta I_{L\mathrm{m,Tp},t\mathrm{on,HV1}}$	A	Ripple-Current Through $L_{\mathrm{m,\,Tp}}$ Caused During $t_{\mathrm{on,\,HV1}}$
$\Delta I_{L\mathrm{p}}$	A	Ripple-Current Through L_{p}
$\Delta I_{L\mathrm{p},t\mathrm{off,HV1}}$	A	Ripple-Current Through L_{p} Caused During $t_{\mathrm{off,\,HV1}}$
$\Delta I_{L\mathrm{p},t\mathrm{on,HV1}}$	A	Ripple-Current Through L_{p} Caused During $t_{\mathrm{on,\,HV1}}$
ΔQ	A s	Charge Difference
Δt	s	Time Difference
ΔV	V	Voltage Difference

ΔV_{out}	V	Output-Voltage Ripple
$\eta_{\text{AC-AC}}$	%	Efficiency of the AC-AC Converter Stage
$\eta_{\text{AC-DC}}$	%	Efficiency of the AC-DC Converter Stage
η_{buf}	%	Efficiency of the Buffer Stage
$\eta_{\text{DC-DC}}$	%	Efficiency of the DC-DC Converter Stage
$\eta_{\text{DC-DC,1}}$	%	Efficiency of the First DC-DC Converter Stage
$\eta_{\text{DC-DC},n}$	%	Efficiency of the nth DC-DC Converter Stage
η_{LR}	%	Efficiency of a Linear Regulator
η_{max}	%	Peak Efficiency
η_{rtf}	%	Efficiency of the Rectifier Stage
η_{SC}	%	Efficiency of an SC Converter
$\eta_{\text{SC,max}}$	%	Maximum Value of η_{SC}
$\eta_{\text{SC,min}}$	%	Minimum Value of η_{SC}
μ_0	Vs/Am	Magnetic Constant
$\mu_{\text{r,core}}$	1	Permeability of the Core Material
$\mu_{\text{r,DC,core}}$	1	DC Permeability of the Core Material
$\mu_{\text{r,wire}}$	1	Permeability of the Wire Material
ρ	Ω m	Specific Electric Resistance
$\phi 1$		Phase Phi Number One
$\phi 2$		Phase Phi Number Two
ϕn		Phase Phi Number n

Chapter 1
Introduction

The continuously growing field of applications for IoT and smart homes leads to a trend toward both miniaturization and decentralization [1]. This trend is further driven by the increasing complexity of electric vehicles and industrial applications that demand smaller and smarter decentralized electronics to enable higher functionality and higher productivity [2].

Figure 1.1 illustrates typical IoT and smart-home applications. They range from simple tasks, such as remotely controlled light bulbs and temperature control in every room of a building, up to complex home-automation systems [1]. Thereby, the number of the required sensor nodes, transmitters, receivers, and actuators increases drastically with the complexity of the system. In order to realize their tasks, they usually need to be distributed over the whole building. For example, the control panel of a heater must be easily accessible to the user, whereas the actuator must be directly connected to the heater, and temperature sensors need to be distributed in the room. To reduce the wiring, the communication between components is realized wirelessly via transmitters and receivers.

In electric vehicles, more and more sensors, actuators, and control units for lighting and entertainment are used to improve safety and driving comfort [3]. Examples are airbag and distance sensors in the bumper, small electrical motors in the seats that are used to adjust the seat position, and rear-view cameras. A similar trend is observed in the context of Industry 4.0 / 5.0. Industry 4.0 / 5.0 targets increased productivity and reduced cost by smart autonomous systems [4, 5]. These systems require many sensors and actuators everywhere in the production line for comprehensive monitoring and control of the production process [2].

A huge challenge that all of these applications have in common is their power supply. The trend toward decentralization leads to large distances between subsystems and, thus, demands a separate power supply for each of them. Conventionally, batteries are used to supply each subsystem [6], which has the drawback of high maintenance. An approach that significantly reduces maintenance requirements is energy harvesting [6]. However, its typical output power is limited to

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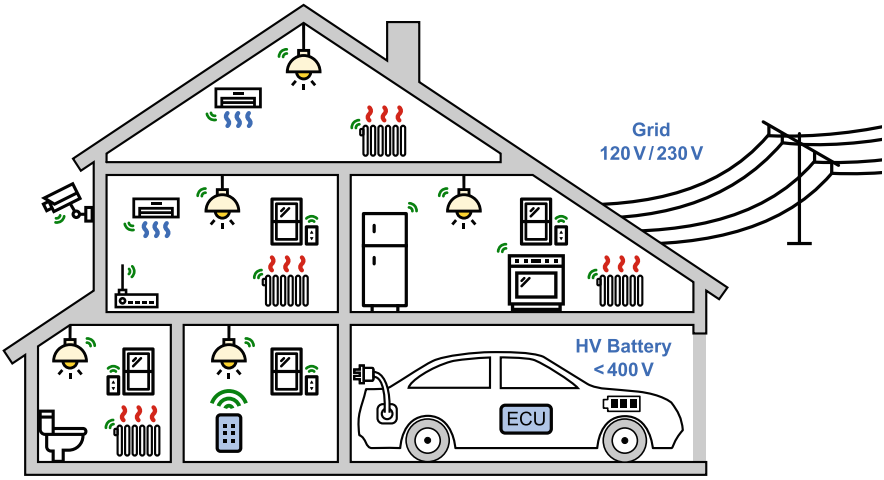

Fig. 1.1 Increasing demand for smaller, cheaper, and efficient AC–DC and DC–DC converters

below 1 mW [7], which is not enough for the continuously growing functionality and complexity of the target applications with a power consumption of up to several tens or even hundreds of milliwatts [4, 8–10]. The limitations of these conventionally used power sources demand alternative solutions that supply powers of up to several hundred milliwatts, have a compact size, and low maintenance requirements.

Figure 1.1 indicates power sources that enable the targeted high output powers and are readily available in every building and every electric vehicle: the AC grid and high-voltage (HV) DC sources, such as the HV battery in electric cars or the DC link in industrial applications. However, most target applications require a supply voltage below 5 V. This demands efficient and compact HV low-power converters that are suitable for all common AC grid voltages (120 V / 230 V) and DC input voltages of up to 400 V [11, 12].

Conventionally, HV conversion is achieved by expensive and relatively large power modules [13–17], as shown on the left in Fig. 1.2. They have poor efficiency below 500 mW, along with low power density. Hence, they are not well-suitable to supply the target applications. The converter-module photos in Fig. 1.2 confirm that their size is mainly defined not only by passive components, such as inductors and capacitors, but also by power switches and diodes.

Prior-art publications [18–21] use a capacitive-coupled AC–AC interface to reduce the HV requirements of the power stage and, thus, to achieve an on-chip integration of the converter at output powers below 1 mW [18–20]. However, for the targeted output powers up to several hundred milliwatts, their HV capacitor in the AC interface needs to be a large external component [21]. This results in power densities below 50 mW/cm^3. In addition, they only allow for AC but not for DC input voltages, which significantly reduces their range of applications. The direct-coupled approach in [22] can be used to achieve higher power densities and

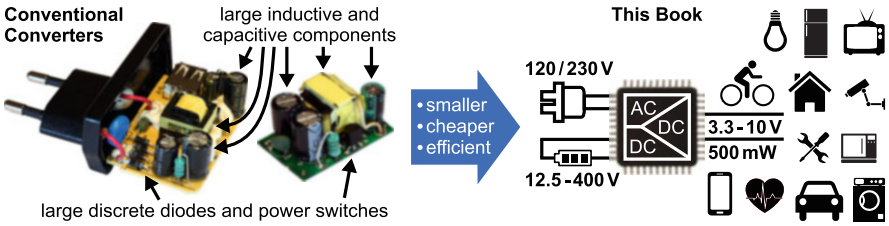

Fig. 1.2 Conventional HV power converters and the target of this book

resistive coupling [23] to enable a wide AC and DC input-voltage range. However, their efficiencies have not shown to exceed 30 %. The large size at sufficient high output power and the low efficiency make these approaches not well-suitable for the targeted decentralized low-power applications.

This book presents solutions for a chip-scale HV AC–DC and DC–DC conversion with higher power density compared to existing solutions. As depicted in Fig. 1.2, the implemented converters are optimized to efficiently supply low-power applications from the grid and from HV DC sources.

1.1 Scope of This Book

The scope of this book is summarized and depicted in Fig. 1.3. It is strongly related to the trend toward miniaturization and decentralization of more and more complex systems and the resulting demand for an efficient and compact power supply for each of the low-power subsystems. The grid and HV DC sources represent a convenient way to supply these applications with sufficient output power and low maintenance effort. However, existing HV power solutions are bulky, inefficient, or cannot provide the required power. This book covers solutions for isolated and non-isolated low-power-optimized HV converters in standard HV silicon-on-insulator (SOI) technologies. The implemented converters are not only suitable for all common grid voltages (120 V / 230 V) but also for a wide DC input-voltage range $\left(12.5\,\mathrm{V} \leq V_{\mathrm{in,DC}} \leq 400\,\mathrm{V}\right)$. Their maximum output power of up to 500 mW and their high power density of up to $752\,\mathrm{mW/cm^3}$ make the implemented converters well-suitable for IoT and smart-home applications as well as for e-mobility and industry.

Figure 1.3 indicates that the size reduction of the passive and discrete components of the power stage is one of the major challenges toward a high power density of HV power supplies. The second major challenge is the reduction of steady-state losses as well as HV-related capacitive and resistive losses to achieve high converter efficiencies even at light-load conditions. The third major challenge is the targeted high-voltage-conversion ratio between the input and output voltages. The wide input-voltage and output-power range is the fourth major challenge.

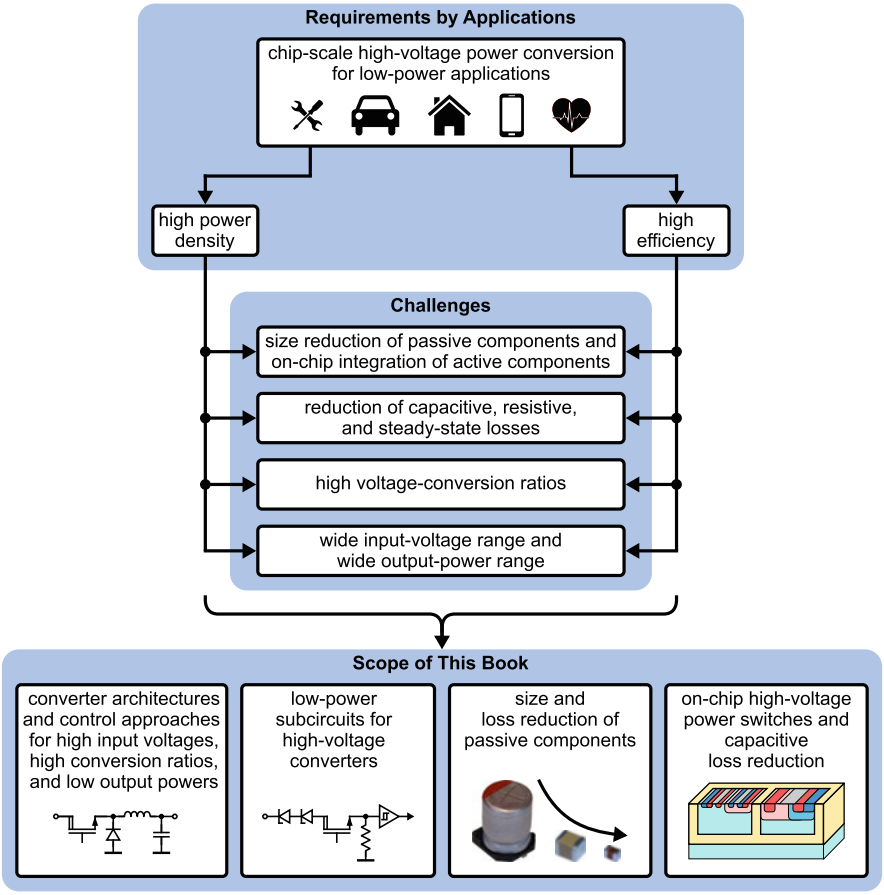

Fig. 1.3 Summary of the scope of this book

This book addresses these four major challenges through four main topics that are illustrated at the bottom of Fig. 1.3: (1) Low-power optimized HV converter architectures and control approaches are developed for the targeted high-voltage-conversion ratios. They enable a high converter efficiency over the whole targeted input-voltage and output-power range at a compact size. (2) Low-power subcircuits are developed for a reliable converter operation with a high common-mode-transient immunity (CMTI) at low steady-state losses and low HV-related capacitive and resistive losses. (3) A comprehensive analysis enables the size and loss reduction of the power inductor and transformer. An active zero-crossing buffer is developed to reduce the size of the mandatory buffer capacitor in the AC interface. (4) Capacitive-loss-reduction techniques are developed to reduce HV-related capacitive losses to a minimum. Techniques for a reduction of substrate coupling as one major disturbance mechanism are developed. The performance of state-of-the-art on-chip HV power

switches is analyzed to enable a size and loss reduction by selecting a well-suited power-switch type for each converter architecture.

1.2 Outline

This section shows the structure of this book and gives a short summary of the content of each chapter.

Chapter 2 highlights the motivation of this book. It discusses the requirements of power supplies for the target applications for IoT and smart homes as well as for e-mobility and industry. It further compares prior-art publications and commercially available power modules and discusses the challenges of compact and efficient converter designs at high-voltage-conversion ratios, low output powers, and a wide input-voltage and output-power range.

Chapter 3 presents HV power converters as a solution to the design challenges at high input voltages and low output powers identified in Sect. 2.3. Section 3.1 discusses the characteristics of state-of-the-art converter architectures and control approaches regarding their suitability for a chip-scale HV low-power conversion. The converter architectures developed and implemented in this work are presented in Sects. 3.2 to 3.5. Section 3.2 presents a step-down converter that uses a constant-on-time control to enable a high light-load efficiency even at input voltages of up to 400 V. The converter in Sect. 3.3 uses a resonant approach to enable an efficient and compact power conversion at high-voltage-conversion ratios. Section 3.4 explains how the resonant converter from Sect. 3.3 can be combined with the step-down converter from Sect. 3.2 to take advantage of both architectures. The active-clamp flyback presented in Sect. 3.5 gives a solution for applications requiring galvanic isolation. Section 3.6 compares the performance of the implemented converters to commercial products and prior-art publications. Section 3.7 discusses the design of the power inductor and transformer for light-load-optimized HV power converters.

Chapter 4 presents an offline chip-scale power supply as a solution to the design challenges at high AC input voltages identified in Sect. 2.3. Section 4.1 discusses state-of-the-art approaches for the different stages of an AC–DC converter. In Sect. 4.2, the structure of the implemented AC–DC converter is developed. It includes a detailed analysis of the developed active-zero-crossing buffer that enables the on-chip integration of the buffer capacitor up to several milliwatts of output power. The required control circuits for the AC–DC converter are presented in Sect. 4.4. Sections 4.5 and 4.6 show the loss breakdown and the experimental results of the implemented AC–DC converter, respectively. A comparison of the converter to prior-art publications and commercially available power modules is found in Sect. 4.7.

Chapter 5 describes the low-power subcircuits that are developed in this work to enable a reliable and efficient power conversion of the converters described in Chaps. 3 and 4, even at light-load conditions, and measured slew rates as high