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Edited by Hong Meng and Wei Huang

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Preface

With the advent of the digital and information age, flexible electronic technology has gained increasing attention from the academic and industrial worlds. The development of this technology has made electronic devices lighter, more durable, and capable of deploying electronic functions on various shapes and surfaces, opening up new possibilities for designing and manufacturing innovative products. As a cutting-edge technology with huge potential, flexible electronic technology is reshaping our everyday lives and could potentially have a profound impact on various industries. Flexible electronic packaging technology, as an important and key part of flexible electronic technology, is continually advancing with technological innovation. This powerful tool has had a profound impact on various fields, including the Internet of Things, consumer electronics, healthcare, and new energy vehicles. Given the rapid changes in this unpredictable field, we believe it is necessary to compile a professional book on flexible electronic packaging technology that systematically and straightforwardly introduces and discusses the basic theories, practical applications, and frontier developments of this technology. The rise of flexible electronic packaging technology is rooted in the pursuit of more portable, lighter, and humanized electronic devices. Today, as technology continues to advance, our demand and expectation for electronic devices are constantly increasing. What we pursue is not only functionality and powerful performance but also lightness, flexibility, and environmental friendliness. This requires us to adopt new materials and new manufacturing processes, and flexible electronic packaging technology is key to meeting these needs.

Chapters 1 and 2 will provide readers with a comprehensive background and basic concepts, including the historical development, basic components, working principles, and application areas of flexible electronic packaging technology. The goal of these two chapters is to help readers establish a comprehensive understanding and deep comprehension, providing a clear direction and solid foundation for subsequent learning and applications. In Chapters 3 and 4, we will focus on flexible substrates and related testing methods, two indispensable aspects of flexible electronic packaging. In these chapters, we provide detailed explanations and practical guides, aiming to help readers understand and master these key points. In Chapters 5 and 6, we will delve into the specific operations of flexible electronic packaging and discuss the development of flexible electronic packaging technology, including traditional packaging technology, the latest research results, and frontier technologies. Through these two chapters, we hope that readers can have a deeper understanding and knowledge of flexible electronic packaging technology and better prepare for its future development. In the following three chapters, we will explore the applications of flexible electronic packaging technology in various industries, introduce related testing standards, and reveal industry business models and success stories through case studies of flexible electronic packaging companies. Through these contents, we hope to help readers understand the practical applications and commercial value of flexible electronic packaging technology, enabling them to transform theoretical knowledge into practical skills and achieve success in their respective fields. In the final chapter, we will look forward to the development trend of flexible electronic packaging, including the development of technology, changes in the market, policy impacts, and social demands. Through this chapter, we aim to help readers have a clearer understanding and better preparation for the future.

In summary, this book offers a comprehensive overview of the development and innovative trends within the field of flexible electronic packaging technology, further underscoring its pivotal role in the advancement of future technology. Our aim is to provide a systematic understanding of this technology to our readers, regardless of whether they are newcomers to this field or have already built a certain foundation.

The chapters of this book were completed jointly by students and teachers from Northwestern Polytechnical University and Peking University Shenzhen Graduate School. Here, we would like to express our deepest gratitude to the teachers and students who contributed to this book: Chapter 1 was written by student Chen Yongji and Prof. Liu Zhenguo; Chapter 2 was written by Prof. Zong Peng'an; Chapter 3 was written by Prof. Chen Yanhui; Chapter 4 was written by student Yuan Junjie and Prof. Meng Hong; Chapter 5 was written by Prof. Yu Tao; Chapter 6 was written by student Rao Qiushi and Prof. Meng Hong; Chapter 7 was written by Prof. Zhang Yuezhou; Chapter 8 was written by student Yuan Junjie and Prof. Meng Hong; Chapter 9 was written by teacher Wei Zhenrong and Prof. Meng Hong; and Chapter 10 was written by student Liu Mingqiang and Prof. Meng Hong. The editing work of the book was completed under the personal deployment and careful guidance of academician Huang Wei. We thank them for their selfless contributions and for investing their valuable time. We also thank our families for their support and encouragement, and the contributions of students Chen Yongji and Yuan Junjie in the editing process of the book. We also appreciate our readers for choosing this book as part of their learning journey, and we look forward to your achievements and breakthroughs in this field. We are willing to accompany you on this path full of challenges and opportunities, witnessing the development and transformation of flexible electronic packaging technology together.

23 July 2023

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1

Overview of Flexible Electronic Encapsulating Technology

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1.1 Flexible Electronics Overview

Flexible electronics, with its unique flexibility, ductility and high efficiency and low cost manufacturing process, have wide application prospects in information, energy, medical, national defense and other fields. As with traditional integrated circuit (IC) technology, manufacturing processes and equipment are also the main drivers for the development of flexible electronics technology. Flexible electronics manufacturing technology level indicators include chip feature size and substrate area size; the key is how to create a smaller feature size of flexible electronic devices on a larger format substrate at a lower cost.

Compared to traditional electronics, flexible electronics have greater flexibility and can adapt to a certain extent to different working environments to meet the requirements of the device's deformation. Flexible electronics covers organic electronics, plastic electronics, bioelectronics, nanoelectronics, and printed electronics, including radio frequency identification (RFID), flexible display, organic electroluminescent (Organic Light-Emitting Diode, OLED) display and lighting, chemical and biological sensors, flexible photovoltaics (PVs), flexible memory or storage, flexible batteries, wearable devices, and many other applications. With its rapid development, the involved fields have been further expanded, and now it has become one of the research hotspots in cross-disciplinary research (Figure 1.1) [1].

In recent years, with the further improvement of flexible electronic technology, we have seen some unimaginable products. For example, the current attention is on folding-screen (Figure 1.2) and wrap-around-screen cell phones. In fact, whether it is a folding screen or a wrap-around screen, the essence of the use of flexible screen technology is that it is a form of flexible electronics technology. The flexible screen, flexible chip, and flexible electrode are only the tip of the iceberg of flexible electronics technology. In fact, information technology involves a variety of sensing, information transmission, information processing, energy storage, and other links that are expected to achieve flexibility [2].

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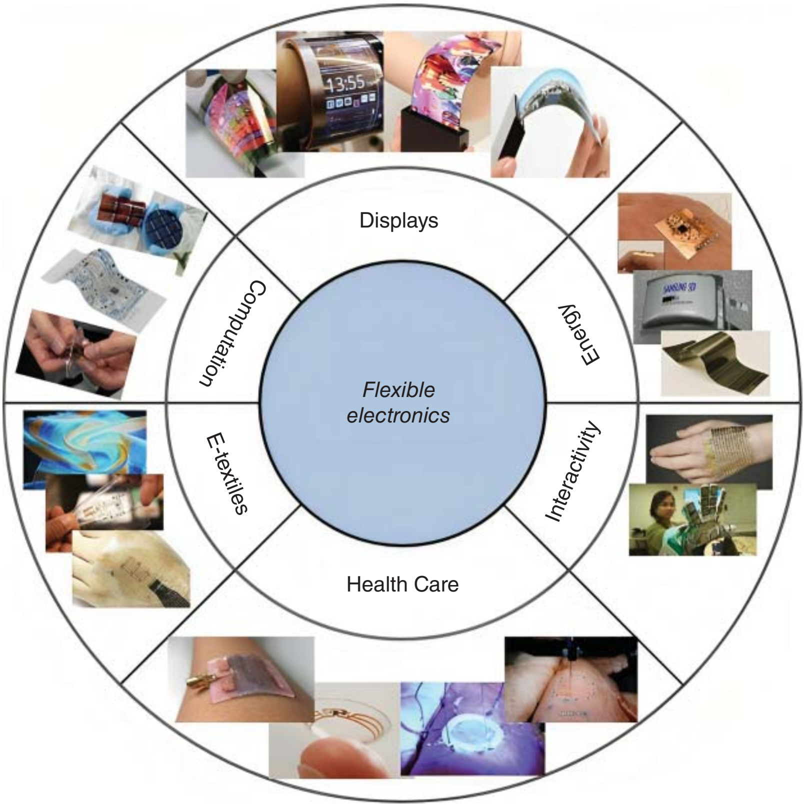


Figure 1.1 The fields of flexible electronics.

So, how exactly is flexible electronics achieved?

First, let us understand the materials used in flexible electronics. Common materials for flexible electronics include flexible substrates, metallic materials, organic materials, inorganic semiconductor materials, and carbon materials represented by graphene (Figure 1.3).

After the raw materials are available, let us look at how flexible electronic devices are manufactured. There are three common flexible electronics fabrication methods: transfer printing, inkjet printing, and fiber structure formation. Among them, transfer printing is a series of functional arrangement techniques used to deterministically assemble micromaterials and nanomaterials into spatially organized structures with two- and three-dimensional layouts [4]. Inkjet printing, on the other hand, as the name implies, allows the direct deposition of functional materials to form patterns on substrates [5]. Flexible electronics fabrication methods based on fiber structures are well suited for wearable electronics that are lightweight, durable, flexible, and comfortable [6].

Since, as mentioned above, flexible electronics have so many advantages and broad application prospects, why has their development been slow to open up?

Figure 1.2 Folding-screen phone.

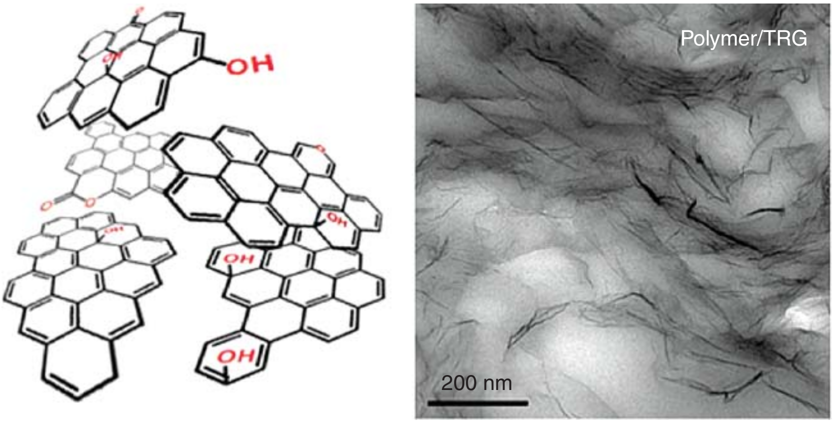


Figure 1.3 Thermally reduced graphite oxide (TRG). Source: Kim et.al. [3]; © 2010, Reproduced with permission from American Chemical Society.

Two major obstacles impede the development of flexible electronics: mechanics and encapsulation. Shen Yang, vice president of the School of Materials at Tsinghua University, has said that the first challenge in the development of flexible electronics is the mechanics of the problem: flexible electronic components in repeated folding and bending will be constantly subjected to alternating stress over time, making them easy to crack. This problem can be overcome mainly through structural design. The second challenge is the problem of electronic encapsulating, which is to integrate the components on the flexible substrate tightly encapsulated together and achieve the desired function.

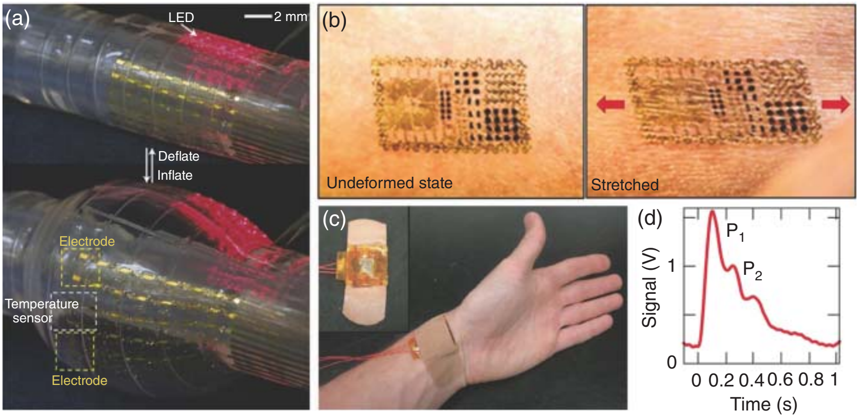


Figure 1.4 Flexible sensors. Source: Hammock et al. [7]; 2013, Reproduced with permission from John Wiley and Sons.

Furthermore, the slow progress in the development of flexible electronics can be attributed to the absence of a significant "viral effect" in terms of application scenes. In other words, the folding-screen cell phone is not an industry pain point. However, another application of flexible electronics – flexible sensors – may be the real revolutionary change in the industry application scene.

Using flexible sensors and conductors, scientists can convert the external force or heat into electrical signals, which are transmitted to the robot's computer for signal processing, so that it can be made transparent, flexible, extensible, freely bendable, foldable, and wearable electronic skin in order to monitor the human body indicators in real time and accurately [7], as shown in Figure 1.4.

Recently, the Institute of Mechanics of the Chinese Academy of Sciences, in cooperation with researchers from Dalian University of Technology and Beijing University of Aeronautics and Astronautics, has developed a thin-film patch-type flexible curvature sensor for wearable devices from the mechanical structure design (see Figure 1.5). This sensor can accurately measure the dynamic bending curvature and bending angle of the measured surface, and its bending measurement results are not affected by tensile deformation. So, in practical application, it does not require the sensor to be perfectly bonded to the measured surface but simply fit, so it is no problem at all even with gloves or tights on. Also, this sensor is very suitable for integration with wearable apparel and can be applied to flexible smart wearable devices such as joint flexion monitoring, gesture recognition, and sitting posture monitoring [8].

Currently, there are two main approaches to the selection of flexible electronic materials internationally. One approach is to shift from traditional inorganic materials to organic materials, such as polymer materials and organic semiconductors, for flexible electronic applications. Another approach involves the combination of organic and inorganic materials, utilizing composite materials to develop flexible electronic devices.

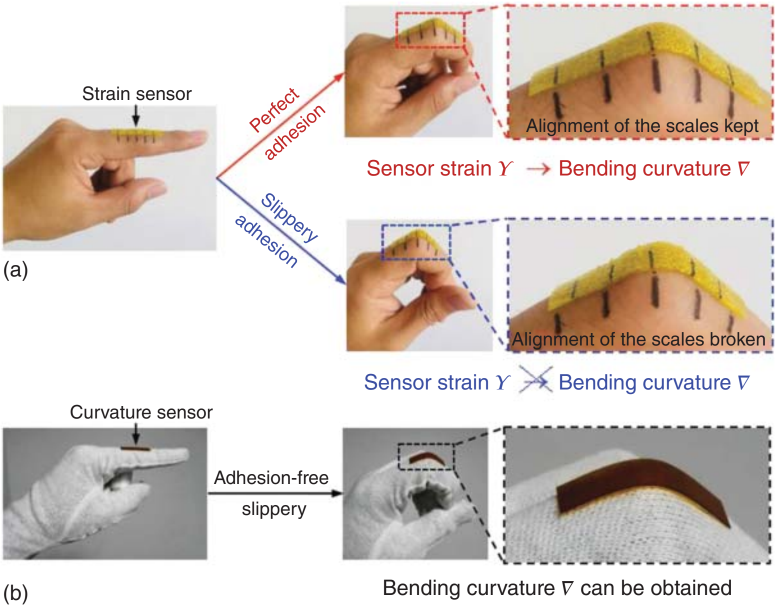


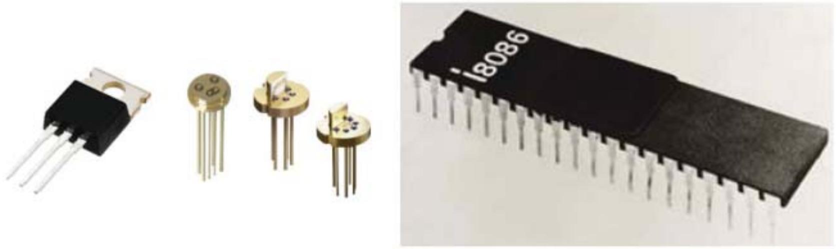
Figure 1.5 Curvature sensors for joint flexion deformation, gesture recognition, and sitting posture monitoring. (a) Strain sensor. (b) Curvature sensor. Source: Liu et al. [8]; © 2018, Reproduced with permission from John Wiley and Sons.

Since the discovery of graphene, two-dimensional materials consisting of single layers of atoms, such as boron nitride, molybdenum disulfide, and black phosphorus, have garnered attention from the semiconductor industry. Research related to these two-dimensional materials holds promise for the advancement of flexible electronics.

The successful application of flexible displays, flexible sensors, and other flexible electronic components signifies the transition of flexible electronics from theory to practice. This advancement may herald a new era of electronic device revolution, bridging the gap between humans and machines and fostering closer interactions.

1.2 Development of Flexible Electronic Encapsulating Technology

One generation of encapsulating, one generation of products. One generation of encapsulating, one generation of products. After the flexible electronic device is manufactured, before it is brought to market as a product, it needs to be packaged to isolate water vapor to ensure its stable operation and complete function. The encapsulating of flexible electronic devices is the same as the encapsulating of traditional electronic devices and is a branch of the encapsulating of electronic devices. When it comes to the word encapsulating, it first originated from the encapsulating of ICs,



(a) (b)

Figure 1.6 TO-type encapsulation (a) and double inline encapsulation (b). Source: Reproduced with permission from huangye88.com / http://yiqiyibiao.huangye88.com/xinxi/5529un9e0ef8b2.html / last accessed 02 August 2023.

and the development of IC encapsulating was developed along with the development of IC chips. The history of the development of encapsulating is also the history of the continuous improvement of chip performance and the continuous miniaturization of the system. As the size of IC devices shrinks and the operating speed increases, new and higher encapsulating requirements are placed on ICs.

Therefore, before introducing flexible electronic device encapsulating, we review the development history of the IC encapsulating industry, which will inspire us to learn as well as develop flexible electronic device encapsulating. The history of the IC encapsulation industry can be divided into two stages: traditional encapsulation and advanced encapsulation, with the year 2000 serving as a crucial boundary [9].

Traditional encapsulating: The development of traditional encapsulating technology can be further subdivided into three phases.

- **Phase 1 (before 1980)**: This phase corresponds to the through hole (TH) era, characterized by jack mounting to printed circuit boards (PCBs), pin counts below 64, fixed pitch, a maximum mounting density of 10 pins/cm^2, and encapsulation types such as transistor outline (Transistor Outline Encapsulation, TO) and dual inline (Dual Inline Encapsulation, DIP), as represented in Figure 1.6.
- **Phase 2 (1980–1990):** This phase marks the surface mount technology (SMT) era, characterized by the use of leads instead of pins, wing-shaped or ding-shaped leads, two-sided or four-sided leads, pitch ranging from 1.27 to 0.44 mm, suitable for 3–300 leads, mounting density of 10–50 pins/cm^2, and encapsulation types such as small outline encapsulation (SOP) and quad-edge flat Packaging (QFP), as depicted in Figures 1.7 and 1.8.
- **Phase 3 (1990–2000):** This phase corresponds to the area array encapsulation era, represented by ball grid array (BGA) and chip scale encapsulation (CSP). In this phase, solder balls are used for encapsulation, greatly reducing the distance between the chip and the system. Moreover, the multi-chip module (MCM) represents the integration of multiple chips on a high-density multilayer interconnected substrate using SMT, enabling the assembly of various electronic components and subsystems, as shown in Figure 1.9.


(a) (b) (c)

Figure 1.7 Narrow pitch small outline encapsulation (SSOP) (a), thin small outline encapsulation (TSOP) (b), and thin shrink small outline packaging (TSSOP) (c). Source: Reproduced with permission from Guangzhou Nuode Electronics Co., Ltd / https://www.nodpcba.com/news/2769-cn.html / last accessed 02 August 2023.

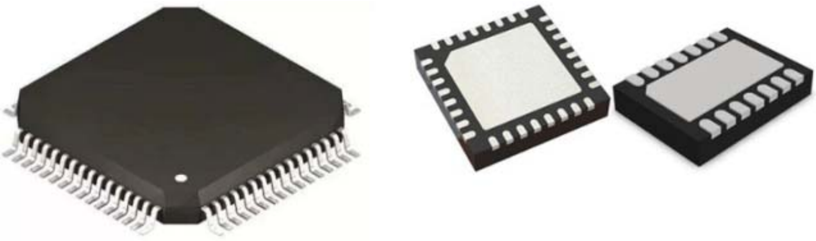
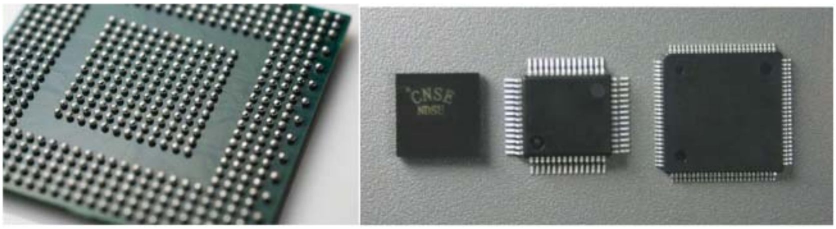

(a) (b)

Figure 1.8 Quad-edge flat encapsulation (QFP) (a), Quad (dual) edge pinless flat encapsulation QFN/DFN (b). Source: Reproduced with permission from Guangzhou Nuode Electronics Co., Ltd / https://www.nodpcba.com/news/2769-cn.html / last accessed 02 August 02 2023.



(a) (b)

Figure 1.9 Solder ball array encapsulation BGA (a), chip level encapsulation (CSP) (b). Source: Reproduced with permission from biyuzg / http://www.biyuzg.com/ / last accessed 02 August 02 2023.

Advanced encapsulation: Since the mid-1990s, driven by the demand for multifunctional system products and advancements in CSP encapsulation and multilayer substrate technology, the IC encapsulation industry has entered the era of three-dimensional (3D) stacked encapsulation. The key features of advanced encapsulation include: (i) the evolution from encapsulating components to encapsulating systems; (ii) the shift from single-chip to multi-chip development; (iii) the transition from multi-chip module (MCM) flat encapsulation to 3D encapsulation; and (iv) the adoption of flip chip (FC) connection and

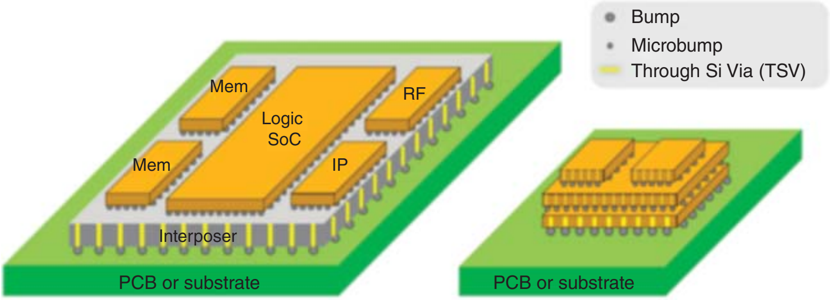


Figure 1.10 2.5D IC encapsulation (a), 3D IC encapsulation (b). Source: Reproduce with permission fromANSYScorporation.

silicon through-hole connection (Through Silicon Vias, TSV) as the main bonding methods. Advanced encapsulation technologies include FC, wafer-level encapsulation, and encapsulation-on-encapsulation (PoP)/system-in-a-encapsulation (Sip)/TSV, which exhibit the following characteristics.

3D encapsulating technology: Multi-chip component planar encapsulating technology integrates multiple IC chips to achieve the integration of encapsulated products in terms of area, then allows chip integration to achieve vertical integration, which is the main efficacy of 3D encapsulating technology. 3D encapsulating can be achieved in two ways: die stacking and encapsulation stacking within the encapsulation. 3D encapsulating is a combination of FC, wafer-level, and POP/Sip/TSV encapsulating technologies, and its development is divided into three stages: the first stage uses lead and FC bonding technology to stack chips; the second stage uses encapsulation body stacking (POP); and the third stage uses through-silicon-via technology to achieve chip stacking (Figure 1.10).

FC technology is not a specific encapsulation type but a circuit interconnection technology that facilitates direct connection between the chip's bare face and the substrate. Unlike wire bond (WB) and tape automated bonding (TAB) technologies that restrict the chip pads to the periphery of the chip, FC technology allows for better electrical performance by utilizing the entire chip area, eliminating the need for interconnection leads. The general structure of FC encapsulation is illustrated in Figure 1.11.

Wafer-level encapsulation (WLP) technology is a product of the combination of FC technology with surfacemount technology and solder ball array encapsulating technology under the continuous pursuit of miniaturization in the market and is an improved and enhanced chip-level encapsulation. WLP is very different from the traditional encapsulating method (first cut and then sealed, after the encapsulation area is at least greater than 20% of the original chip area). WLP technology is first applied to the whole wafer at the same time for many chip encapsulations, testing, and finally cutting into a single device and directly mounted on the substrate or PCB, so the volume after the encapsulation is equal to the original size of the chip, and production costs are also significantly reduced. WLP technology can also be called standard WLP (fan-in WLP) and then evolved into diffusion WLP (fan-out

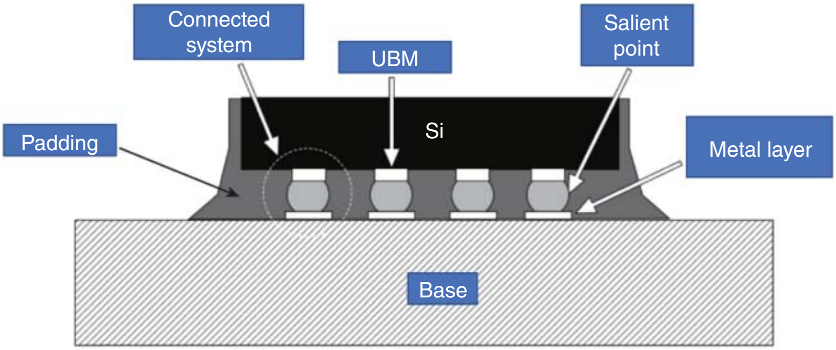
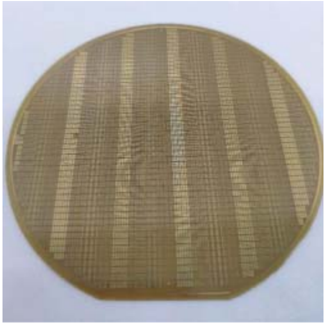


Figure 1.11 General structure of flip chip encapsulation body. Source: Reproduced with permission from www.dymek.cn.

WLP), which is based on wafer reconfiguration technology, rearranging the chip on an artificial wafer and then following similar steps to the standard WLP process for encapsulating, as depicted in Figure 1.12.

PoP is an out-of-encapsulation encapsulation, which refers to the longitudinal arrangement of logic and storage components of the IC encapsulation form. It uses two or more BGA stacks with generally strong resistance under the logic operation located at the bottom and storage components located in the upper, using solder balls to combine the two encapsulations. It is mainly used in the manufacture of advanced portable devices and smartphones used in advanced mobile communication platforms, as shown in Figure 1.13.

Figure 1.12 Wafer-level encapsulation devices. Source: Reproduced with permission from Daimei Instrument Technology Service (Shanghai) Co., Ltd / https://www.dymek.cn/ / last accessed 02 August 2023.



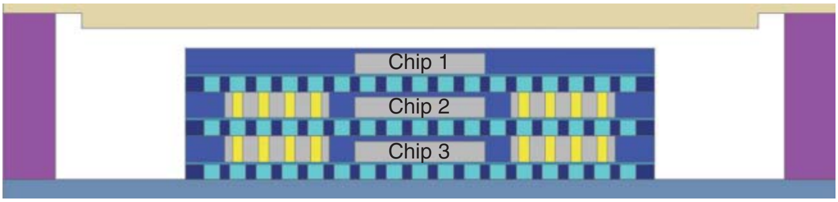


Figure 1.13 Three-dimensional chip stacking structure. Source: Reproduced with permission from www.dymek.cn.

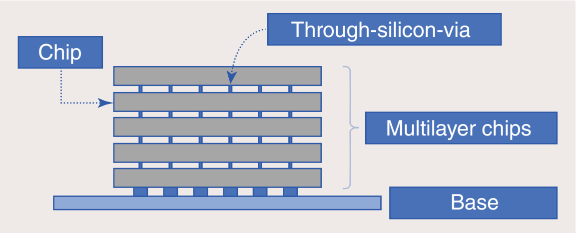
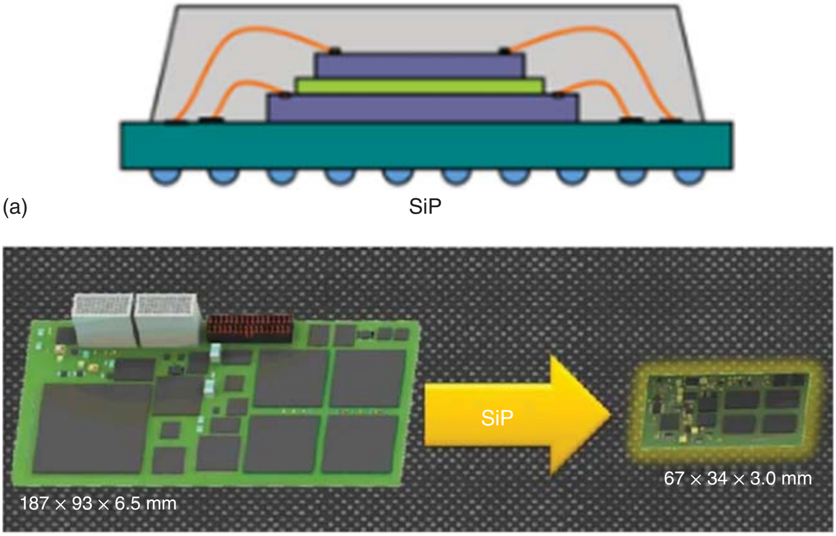


Figure 1.14 3D encapsulation structure using silicon through-hole technology. Source: Reproduced with permission from https://zhuanlan.zhihu.com/p/396703245.



(b)

Figure 1.15 System-level encapsulation structure schematic (a) and system-level encapsulation devices (b). Source: Reproduced with permission from https://smartwear.zol.com.cn/458/4582055.html.

TSV technology is also a circuit interconnection technology that interconnects chips by creating vertical conduction between chip and chip and wafer to wafer. Unlike previous IC encapsulation bonding and stacking techniques that use bumps, TSV enables the highest density of chip stacking in the three-dimensional direction, the smallest form factor, and greatly improves chip speed and low power performance. TSV is a key technology for 2.5D and 3D encapsulations, as illustrated in Figure 1.14.

System in a encapsulation (SIP) technology is the integration of multiple functional chips, including processors, memories, and other functional chips, into a single encapsulation to achieve an essentially complete function. It corresponds to a system on a chip (SOC). The difference is that SOC is an encapsulation in which different chips are encapsulated side by side or stacked, while SOC is a highly integrated chip product (Figure 1.15).

Overall, encapsulating technology has evolved from traditional encapsulations (DIP, SOP, QFP, PGA, etc.) to advanced encapsulations (BGA, CSP, FC, WLP, TSV, 3D stacking, SIP, etc.). In terms of structure, encapsulations have evolved from the early transistor outline encapsulation (TO) to DIP and to SMT in the 1980s. The SOP was derived from SMT in the 1980s, and gradually the small outline J-lead (SOJ), Thin Small Outline Encapsulation (TSOP), and Very Small Outline Encapsulation (VSOP) were derived. SOP, Shrink Small Outline Encapsulation (SSOP), Thin Shrink Small Outline Encapsulation (TSSOP), Small Outline Transistor (SOT), SOJ, TSOP, VSOP, SSOP, SOT, small outline integrated circuit (SOIC), etc., and the later plastic leaded chip carrier (PLCC), QFP. After the IC function and the number of I/O pins gradually increased, Intel took the lead in updating the QFP package to the ball grid array package (BGA) in 1997. The recent mainstream packaging methods are chip scale package (CSP) and overlay package or flip chip package (Flip Chip). From the encapsulating materials, including metal, ceramic, plastic, and other materials used for encapsulating, many high-intensity working conditions of the circuit such as military and aerospace level still have a large number of metal encapsulating. Therefore, the general development process of IC encapsulation can be summarized as follows:

Structure: TO-DIP (Dual In-Line Encapsulation) – PLCC – QFP – BGA – CSP.
Material aspects: (metal, ceramic) – (ceramic, plastic) – plastic.
Pin shape: long-lead direct insertion – short-lead or leadless placement – ball-and-bump soldering.
Assembly method: TH cartridge – surface assembly – direct mounting.

The current global mainstream encapsulating technology of ICs is the third-generation encapsulating technology, namely BGA encapsulation, chip-level encapsulation (CSP), and FC. Among them, FC encapsulating technology, which is considered necessary to promote low-cost, high-density portable electronic device manufacturing process, has been widely used in the consumer electronics industry. The fourth-generation encapsulating technologies, such as WLP, silicon through-hole technology (TSV), and system-level encapsulating (SIP), are still being promoted on a small scale, but they will become the mainstream of future encapsulating methods under the technology upgrade.

In the encapsulating of flexible electronics, the above encapsulating technologies are borrowed and improved, and now the following two processes are mainly used in flexible electronics encapsulating.

1.2.1 Flip Chip Process

FC technology is widely used in traditional microelectronic encapsulating, which has the following characteristics [10]: (i) provides a good point connection for the signal, which can make more effective use of the chip area and has an ultrahigh encapsulating density; (ii) has light mass and small form factor; and (iii) the lead inductance becomes smaller, crosstalk becomes weaker, the signal transmission time is shortened, and thus has excellent high-frequency performance. In flexible electronic encapsulating, FC technology also has these characteristics, and because of the flexible substrate as a carrier, making the product bendable and flexible can

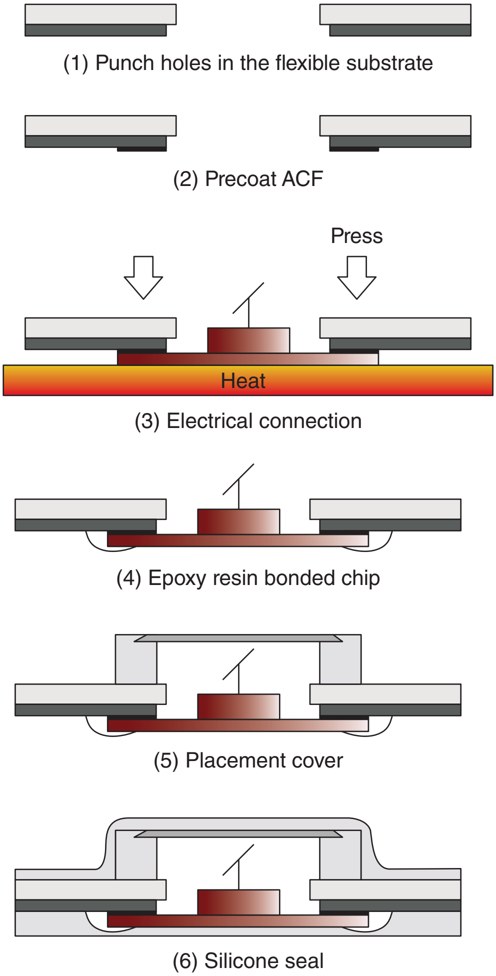


Figure 1.16 The encapsulating process of flip chip. Source: Reproduced with permission from Zhang and Pan. [11]; © 2010, Springer-Verlag.

make full use of space to reduce the size. FC encapsulating methods are solder bump method and conductive adhesive bonding. The former uses the reflow process between the chip and the substrate to form a solder ball, but the reflow requires a high temperature, and commonly used flexible substrate materials including polyimide and polyester (PET) are only suitable for low-temperature (less than 200 °C) bonding technology, so flexible electronic encapsulating is often used in the conductive adhesive connection. Figure 1.16 shows an application of FC technology for flexible encapsulating, and its main process includes [11]: (i) cutting a hole in the flexible substrate that has been made to place the chip; (ii) pasting the anisotropic conductive film (ACF) to the substrate pad for subsequent electrical connection; (iii) adjusting the chip pad so that it is aligned with the pads on the substrate and realizing the physical and electrical connection of the assembly through heating and compression; (iv) filling the side of the chip with epoxy resin to strengthen the structural strength of the assembly to prevent cracks when bending;