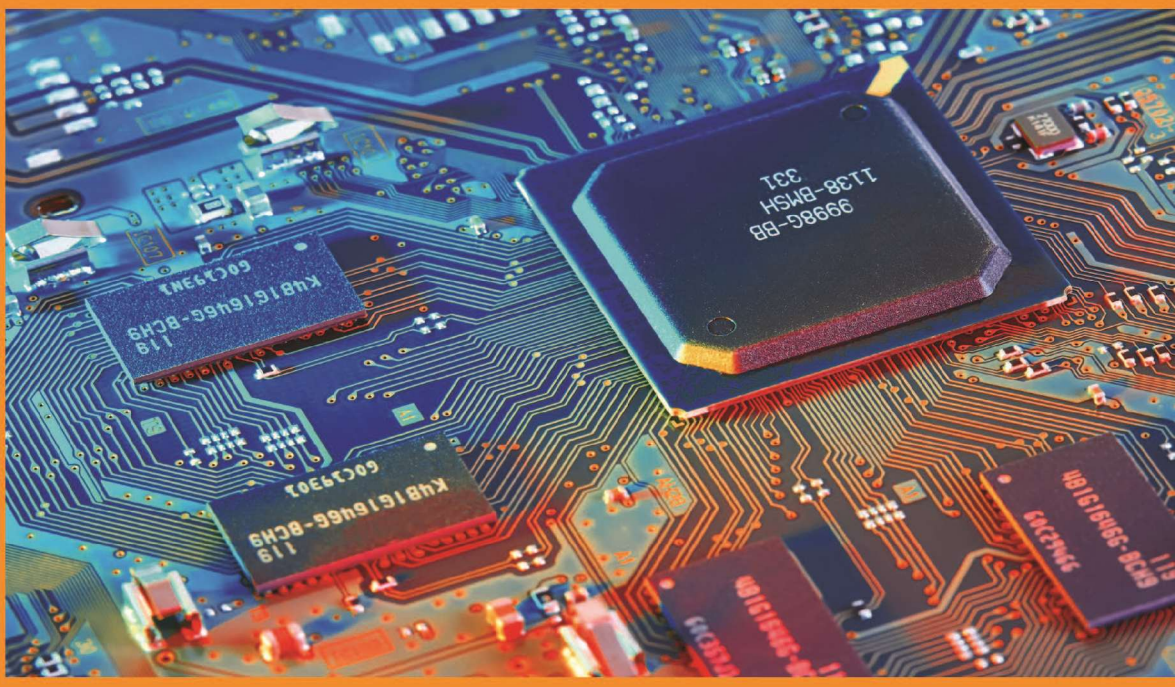
ELECTRONICS ENGINEERING SERIES

Analog Devices and Circuits 2

Analog Circuits

Christian Gontrand



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Preface

At the end of the Second World War, a new technological trend was born: integrated electronics. This relied on the enormous rise of integrable electronic circuits. This field has invaded our societies, and it is far from over!

Since the 1970s, modeling has contributed a great deal to the understanding of basic electric functions, making it possible to carry out "*numerical* experiments", accelerating the effective development of circuits. In these studies, we hope to detect assembly errors as quickly as possible; for example, the arrows of currents, indicated in the diagrams of devices and circuits, allow us to verify that there is no break in the current flow between the plus and minus "rails", typically correcting any "assembly" error of the circuit.

But, of course, this simulation has allowed for significant productivity gains, avoiding, in particular, the effective and overly-upstream manufacture of demonstrators.

This book is in fact a second volume, wherein the first discusses analog devices constituting these circuits. Of course, in this volume we will focus a little more on the "flagship chip": the operational amplifier.

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November 2023

1

On Analog Circuits

1.1. Introduction: miscellaneous

1.1.1. *SPICE*

SPICE (Simulation Program with Integrated Circuit Emphasis) is the standard for simulating analog circuits. Anyone who does not know this does not belong to the fraternity of electronic circuit analogists.

SPICE was created at the University of California (Berkeley) in the early 1970s by Ron Rohrer's team, including Larry Nagel (see his famous thesis). It later became the standard for analog simulators. Three versions followed one another, including SPICE3, dated 1985.

1.1.1.1. *A brief history of SPICE*

The need for a circuit simulation program, "smart" people with a vision and hardworking teams of students and professionals have all contributed to the realization and evolution of SPICE. A brief history of this powerful simulator is explained below, which is organized primarily according to the different versions of SPICE.

CANCER

– In the early 1970s, Ron Rohrer hoped to develop a simulation program for his work on optimization at the University of California, Berkeley.

– Rohrer's students, including Larry Nagel, created CANCER (Computer Analysis of Nonlinear Circuits Excluding Radiation).

– It performs DC, AC, and transient analysis.

– The devices include diodes (Shockely equations) and bipolar junction transistors (Ebers–Moll equations).

Other simulation programs at the time included ECAP (Electronic Circuit Analysis Program) and IBM's Autonetics TRAC.

SPICE1

– In 1972, Nagel and Pederson launched SPICE1 (Simulation Program with IC Emphasis) in the public domain.

– SPICE became the industry standard simulation tool.

– Bipolar junction transistor models were replaced by Gummel–Poon equations.

– JFET and MOSFET templates were added.

– It was based on nodal analysis.

– It was written in FORTRAN code and runs on large computers.

SPICE2

– Nagel's 1975 version offered significant improvements.

– Modified nodal analysis (MNA), replacing the old analysis, supported voltage sources and inductors from this point onwards.

– Memory was dynamically allocated to accommodate the increasing size and complexity of circuits.

– It has adjustable simulation of time step control speeds.

– The MOSFET and bipolar models were revised and extended.

– SPICE2G.6 (1983) is the latest version of FORTRAN.

At present, it is still available in Berkeley. Many commercial simulators today are based on SPICE2G.6.

SPICE3

– SPICE code was rewritten in programming language C (1985).

– It has a graphical interface to display the results.

– It included polynomial capacitors, inductors and voltage-controlled sources.

– The new version eliminated many convergence problems.

– Models added were as follows: MESFET, lossy transmission line and nonideal switch.

– Improved semiconductor models adapted to smaller transistor geometries.

– It is not backward compatible with SPICE2.

1980s and beyond

– Published commercial versions include HSPICE, IS_SPICE and MICROCAP.

– MicroSim launched PSPICE, the first PC version of SPICE.

– SPICE attracted many more users in industry and academia.

– EDLO is dedicated to RF.

– HICUM is dedicated to microwaves.

– Companies integrated SPICE versions into their “schematics” entry and layout packages (geometry/pattern).

1.1.1.2. *A SPICE program*

SPICE is therefore the essential software for studying analog circuits.

1.1.1.3. *Program example*

The program example is given as follows.

```
I-V characteristics for SS model of CMOS devices
 MODEL NSS NMOS  LEVEL =3  RSH=0  TOX=275E-10  LD=0 . 1E-6  XJ=0 . 14E-6
+  CJ=1 . 6E-4  CJSW=1  8E-10  UO550  VTO=1 . 022 CGSO=1 . 3E10
+  CGDO=1  3E-10  NSUB=4E15  NFS=1E10
+  VMAX=12E4  PB=0 . 7  MJ=0 . 5  MJSW=0 . 3  THETA=0 . 06 KAPPA=0 . 4  ETA=0 . 14
. MODEL PSS  PMOS  LEVEL=3RSH=0  TOX=275E-10  LD=0 . 3E-6  XJ=0 . 42E-6
+  CJ=7 .  7E-4  CJSW=5 . 4E-10  UO=180  VTO=-1 . 046  CGSO=4E-10
+  CGDO=4E-10  TPG=-1  NSUB=7E15  NFS=1E10
+  VMAX=12E4  PB=0 . 7  MJ=0 . 5  MJSW=0 . 3  ETA=0 . 06  THETA=0 . 03
KAPPA=0 . 4
M1  1  10  0  0  NSS  W=13 . 2U  L=2 .  25U
VDS  20  0
```

```
* VGS is positive for nMOS and negative for pMOS
VGS 10 0 5V
* VIDS defines current direction for drain
VIDS 20 1
.DC VDS 0 5 0.05
.PRINT DC I(VIDS)
.PLOT DC I(VIDS)
.WIDTH IN=75 OUT=75
.END
```

Calculation of current-voltage characteristics of .CMOS

Used for the SPICE (Simulation Program with Integrated Circuits Emphasis) simulation program.

```
* CMOS OPERATIONAL AMPLIFIER *
****  INPUT LISTING                    TEMPERATURE =   27.000 DEG C
******************************************************************************
*************
.MODEL MP1 PMOS (LEVEL=3 TOX=250E-10 VTO=0.55
+ GAMMA=0.38 KP=25.2E-6 NSUB=2E16 THETA=0.163
+VMAX=1E5 FTA=0 DELTA=0 KAPPA=0.8 CGSO=0.65N CGDO=0.65N )
.MODEL MN1 NMOS (LEVEL=3 TOX=250E-10 VTO=0.55
+ GAMMA=0.1 KP=86.8E-6 NSUB=2E16 THETA=0.08
+ VMAX=1E5 FTA=0 DELTA=0 KAPPA=0.8 CGSO=0.42N CGDO= 0.42N )

VDD 10 0 DC 5
VSS 11 0 DC -5
CCR  4 5 10P
CCH  5 0 20P
RIN 16 0 1

* AMPLIFIER
```

```
M1 2 2 10 10 MP1 L = 7.7U W = 8.5U
M2 3 2 10 10 MP1 L = 7.7U W = 8.5U
M3 2 15 1 11 MN1 L = 4.9U W = 25U
M4 3 16 1 11 MN1 L = 4.9U W = 25U
M5 1 6 11 11 MN1 L = 7.9U W = 5U
M6 5 6 11 11 MN1 L = 7.9U W = 19U
M7 5 3 10 10 MP1 L = 7.7U W = 64U
M8 3 9 4 10 MP1 L = 7.7U W = 4U
*VOLTAGE SOURCE
M9 7 7 10 10MP1 L = 7.7U W = 8.5U
M10 6 6 7 10 MP1 L = 7.7U W = 8.5U
M11 6 6 11 11 MN1 L = 7.9U W = 20U
M12 8 8 10 10 MP1 L = 7.7U W = 64U
M13 9 9 8 10 MP1 L = 7.7U W = 50
M14 9 6 11 11 MN1 L = 7.9U W = 19U
```

} Voltage sources

```
VIN 15 0 AC 1

.AC DEC 5 100 100MEG
.PLOT AC VD8 (5) VP (5)
.WIDTH OUT =80
.END
```

1.1.2. *Technologies: conception-aided design*

CMOS operational amplifier

Technology

The technology used is as follows:

– passivation: e_{sio2}: $0.5 - 1$ µm;

– N^{++}: heavily doped buried layer → low resistance;

– P^{+} zones: insulation wells;

– P^{+}-N junction in reverse → insulation;

– N^{++} zone: only for “beep”;

– Si_3N_4: silicon nitride (mask for implants);

– Si_3N_4: prevents oxide growth (but beaks of parasitic birds at the edge of masks: birds peaks).

Below, we shall resume the basic steps of manufacturing the two preferred devices of microelectronics. Diagrams for this have been given in Volume 1.

Bipolar junction transistor

N_epitaxy collector region (0.1–10 Ω.cm):

e_{Nepi} = 2–15 µm

Opening windows are used to create the base and insulation wells. Opening in the base region is used to create the emitter.

Base: a few $\frac{1}{10}$ µµ

N^+: ohmic collector contact

Evaporation of contacts

P-channel MOS:

i) thermal oxidation: $\frac{1}{2}$ µm;

ii) P^+ implementation for drain.

Reoxidation takes place and then so does photo-etching of the oxide.

Gate oxide (dry O_2 for good dielectric quality); thickness: 0.1–0.15 µm.

Field oxide (FOX: Field OXide; LOCOS: LOCal Oxide on Silicon); very thick: 1–1.5 µm.

Self-aligned gate

I^2: (ionic implantation) = 80 keV; the oxide lets boron through (a very small atom), but the gate stops it, and therefore serves as a natural mask.

Polysilicon gate NMOS inverter

Fabrication process steps:

– $Si_3 N_4$ is impermeable to O_2;

– boron: P type;

– LOCOS: $Si_3 N_4$;

– Bird beak: SiO_2;

– threshold voltage adjustment is expressed as: $V_T$adjust;

– phosphorus ⟶ N type.

The I^2 of phosphorus creates source and drain zones and, at the same time, dopes the polysilicone.

The polysilicone "embedded" in the oxide makes it possible to manufacture several levels of interconnections.

Self-aligned polysilicon gate

$$\begin{cases} - \ Creation\ of\ a\ well\ P(10\ \mu m) \\ - \ Ocide\ growth\ \ (1\ \mu) \end{cases}$$

$$\begin{cases} - \ Window + thermal\ oxide\ (0.1\ \mu m) \\ - \ \text{Gate oxide} \end{cases}$$

$$\begin{cases} 0.6\ \mu\ \text{CD}\ polysilicon\ deposit \\ except\ for\ drain - source\ regions \end{cases}$$

$$\begin{cases} Deposition\ of\ boron - doped\ p\ oxide\ (p, cf. ductility) \\ \quad which\ is\ removed\ from\ the\ (left)\ side\ of\ the \\ \quad \underline{N}MOS; then\ phosphorus - doped\ oxide\ (n) \end{cases}$$

{Furnace → impurities drive in silicon: metallization

– Phase 1: Local oxidation:

a) Thermal growth of a thin layer of silicon oxide.

b) Engraving according to level 1:

- field insulation implantation (B^+ ion);

- annealing of the implantation (annealing, for redistribution).

c) Localized thermal oxidation, followed by the removal of the resin from the nitride and the thin oxide.

– Phase 2: Implementation of depletion:

a) Thin gate oxide growth ($\simeq$ 500 Å).

b) Implementation of depletion (P−) according to level 2.

– Phase 3: Adjustment of enhancement transistors:

a) Adjustment implementation (B+) according to level 3.

– Phase 4: Buried contacts or pre-contacts:

a) Etching of the thin oxide according to level 4.

– Phase 5: Gates:

a) Uniform deposition of polycrystalline silicon and etching thereof according to level 5.

b) Source and drain implementation (P or As), annealing and oxidation.

– Phase 6: Contacts:

a) Deposition of insulating oxide and etching of contacts according to level 6.

– Phase 7: Metallization:

a) Uniform deposition of aluminum and then etching according to level 7.

– Phase 8: Deposition of final protective oxide and then etching according to level 8. This level only concerns the electric accesses of the circuit: contact and test pads.

Insulated multi-collector outputs

This device operates in reverse mode (the emitter is replaced by the collector and vice versa).

Here, the buried layer serves as the emitter.

It has five manufacturing steps, as follows:

– I^2 N^-;

– I^2 P;

– $-I^2$ N^-;

– contact window;

– metallization.

Power transistor

Double diffusion D.MOS

To ensure a high voltage withstand, we need to create weakly doped areas that are highly resistive, which “take in” the potential differences.

Purpose: Reducing the channel

$L < 1\ \mu m$

Note: Asymmetric field region → high breakdown voltage.

L: effective length of the channel.

– Highly N-doped substrate is used (→ N-channel MOS).

– Boron implantation is performed (P type).

– Epitaxy (p) from silane (exodiffusion of impurities P from N^- to P): the N^- resting zone will be the field region of the transistor; and the P region (1 µm) will be the channel zone. The drain region is then protected by $SiO_2 - Si_3N_4 – SiO_2$ (•) during the growth of the field oxide (*).

– The oxynitride is then removed, and the thick oxide is etched to implant the source region.

Then oxidation occurs. V-shaped anisotropic chemical attack (direction 100>) takes place faster than 111>.

– Growth of the gate oxide; metallization: source, gate and drain.

– Advantages are as follows: the channel lengths obtained are of the order of 1 µm, without using electronic lithography.

– Extending source-drain space loads are essentially vertical → channel shortening effects are negligible.

- P-type diffusion → substrate;

- $I^2\ N^+$ → source.

The polycrystalline silicon gate is in the form of a hexagonal mesh network burying the source regions: at a given surface, the greatest channel density is obtained.

Manufacturing integrated bipolar/CMOS circuits

a) Wafer thickness (wafer, slice, waffle) = 250 µm.

Doping: $10^{16}\ at/cm^3$.

Low value diffused resistance for collector (20–50 $\mu/\square$).

(As or P because of low diffusivity; large atoms).

Recap: what is resistance per square?

Resistance of a conductive track of length L and width W (a parallelepiped): where L and W characterize the design of the masks, while $R_{\square}$ characterizes the technology. The L/W ratio can be considered as a "number of squares", hence the name of $R_{\square}$: "resistance per square".

$R_{\square} = \rho\ L/S = \rho\ L/(We) = (\rho/e)\ L/(W)$; if $L = nW$, where n is an integer, then:

$R_{\square} = n*(\rho/e)$: Ω.

b) Growth of an epitaxial layer (the thickness determines the breakdown voltage): BV_{CE0}, where,

BV is the beakdown voltage.

c) Oxide growth.

Boron diffusion (channel stop: isolate devices from each other by reverse P/N junctions): several hours at 1,200°C (20–40 Ω/□).

d) Manufacturing the base: 100–300 Ω/□ and a depth of 1–3 μ after diffusion.

e) Emitter: 2–10 Ω/□ and a depth of 0.5–2.5 μm after diffusion.

Creation of the collector contact takes place.

f) Manufacture of contacts: additional layer of aluminum over the entire surface and etching of aluminum out of contacts occurs. The electrically active region (in the live active region) is the base portion under the emitter.

Integrated circuit NPN transistor

(Recap: the layout concerns mask drawing).

Keep in mind the existence, at the contacts, of some "resistor and capacitance contact" parasitics.

In an integrated circuit, characteristic parameters of a transistor can be modified by modifying its geometry. For example, to have a high current transistor, the width of the device is increased, but emitter-base, collector-base and collector-substrate capacitances are then increased (compromise, etc.):

Hence, the modified frequency response is obtained.

r_{b1} "ends" and r_{b2} "begins" at the front of the emitter diffusion:

$$\leftarrow r_{b1} = \frac{10}{25}\ 100\ \Omega = 40\ \Omega$$

For r_{b2}, two-dimensional effect occurs.

Crowding effects (overpopulation, defocusing of minority carriers in the base, injected from the emitter, attracted by the base contact(s)).

Injecting carriers from the emitter into the base

At very high currents, the injection takes place at the periphery of the diffusion of the emitter $r_b = r_{b1}$.

For low-noise or high-frequency transistors of low r_b, the periphery of the emitter adjacent to the base contact is maximized. For HF transistors, numerous narrow bands connected by base contacts are used as emitter geometry.

Collector resistance: 3D (see Laplace resolution)

$$R = \frac{eT}{WL} \cdot \frac{Lg\frac{a}{b}}{a-b} \qquad [1.1]$$

where:

– T = thickness of the region;

– e = resistance of the material;

– $\left.\begin{matrix} W = width \\ L = length \end{matrix}\right\}$ of upper rectangle;

– a (respectively, b) = ratio of the width (respectively, length) of the lower rectangle to the width (respectively, length) of the upper rectangle.

Bases are equipotential and current flows vertically. Holes are injected from the emitter, parallel to the surface through the N-type base region, and are picked up by the P-type collector before reaching its contact. The base is more doped than the collector → the desertion/depletion zone extends rather into the collector (more resistive).

The base must be wide enough so that the depletion zone does not reach the collector. When $V_{ce\ max}$ is applied:

$\underset{\text{min}}{\text{Wb}} = 8\ \mu\text{m}$ for $V_{ce} \nearrow_0^{40v}$ deserted zone (Wb: base width)

It ranges from 6 to 8 µm:

$$t_B(\ transit\ time\ in\ the\ base)\frac{Wb^2}{2\ Dp} = \frac{(8\mu)^2}{2\times 10 cm^2/s} = 32\ ns \qquad [1.2]$$

PNP to substrate transistor

One reason for the poor performance of high current side PNPs is the relatively small effective square cross-section of the emitter.

The PNP often operates in class B for output stages → $I_c = 10$ mA.

The substrate is used as a collector.

pb: lightly doped substrate → high series resistance of the collector:

→ If strong currents: large voltage drops in the substrate.

→ Deteriorated performance can occur if no real collector is processed.

Because of the low doping of the N epitaxial material, the series base resistance can be very high if the base contact is far from the base active region. In this structure, the base contact (N^+) can touch the diffusion of the emitter P in order to obtain a base contact diffusion as close as possible to the active base.

Disadvantage: Breakdown voltage of $V_{BC} \simeq 7$ V is used; to increase it, it is necessary to separate the diffusion p from the n^+.

1.1.3. *Resistor technologies*

Diffused resistors

The areas that can be used as resistance are base diffusions, emitter diffusions, the epitaxial layer, the active base region area and the epitaxial layer pinched between the base diffusion and the P-type substrate.

Diffused emitter and base resistors

The diffused base resistor is formed from the P-type base diffusion for the NPNs and is located in an isolated region. The epitaxial region containing this resistor is biased in such a way that the PN junction between this resistor and the epi. layer is reversed. Hence the creation of a contact occurs in the N-type epi., which is

connected to the end of the most positive resistor or to a potential that is more positive than any end of the resistor:

$$R = \frac{L}{W} R_{\square} \qquad [1.3]$$

where L is the length of the resistor and W is the width.

$R_{\square}$: sheet resistance: 100–200 $\Omega/\square$:

$\longrightarrow R = 50\ \Omega - 50\ k\Omega$

$(W \geq 5\mu)$

With broadcast emitters, we get $R_{\square}$ values up to 10 $\Omega/\square$.

Base pinch resistance

Pinched zone is found between the collector N and emitter N^+; it can be electrically insulated by reverse biasing the emitter-base and collector-base junctions (in practice, N-type regions are connected to the most positive end of the resistor).

$R_{\square}$= 5–15 $k\Omega/\square$ (interesting because wide range).

Since the N region is lightly doped, it is highly dependent on temperature.

Voltage drop on the resistor is ~6 V, breakdown voltage between the top of the diffused emitter and the base diffusion.

Capacitors of integrated circuits

Capacitor of integrated circuits is given as:

$C = 4.0$ to 60pF/cm^2

The breakdown voltage ranges from 60 to 100 V.

The capacitance of the substrate/epi layer junction is negligeable.

High capacitance capacitors (tens of pF) take up a lot of the surface area on the circuit. However, at present, thanks to the design of these circuits, it is possible to reduce the capa. values in order to achieve performances which require large, identical or even better values (see compensation in op. amplifiers). Capacitors can be used by mounting them in shunt, for example, on an amp. Multiplying this capacitance by the gain of the amp. This is the Miller effect.

Two categories are found:

1) P.N junction polarized in reverse → capa. of depletion

- V_{BE} is low ~0.7 V (for V_{BC}, it is stronger but the capa per unit area is lower).

2) MOS capa.

Epitaxial and pinch resistors

To increase the $R_{\square}$, we diffuse P on the top of the epitaxial resistance (behavior identical to a junction FET, JFET).

The pinch-off voltage is a function of the thickness of the epi. and doping.

Limiting the pinch-off resistor to low-level operating voltages does not allow its use in circuits where a low bias current must be derived directly from the supply voltage using a high value resistor. The epitaxial layer itself has a much larger square resistance than the base diffusion, and for this application the epi. layer is often used as resistance. For example, the square resistance of an epitaxial layer with a thickness of 17 µm and a thickness of 5 µcm is equal to:

$$R_{\square} = \frac{1}{q\mu m\, N_d T} = \frac{\ell\, epi}{T} = \frac{R\ \mu\text{cm}}{17\ \mu\text{m}} = 2.9\ \Omega/\square$$

Compatible process for high-performance active devices

Some types of circuits require specific devices such as JFETs for switching and low input current amps, as well as MOSFETs and super-beta NPNs for fast analog circuits. Structures require additional masking steps compared to the conventional manufacturing process.

a) Double diffusion JFET

JFETs can be manufactured on the same surface with bipolar devices, using a different technique mode. If the base region of a standard integrated bipolar circuit is used for the JFET channel, as in the pinch resistor, the pinch voltage is too high because of the channel width of the resulting structure. A narrow-channel double-diffused device can be manufactured on the same surface however, by adding diffusion into the process.

The JFET channel is narrower than the NPN base (the grid is made at the same time as the base: redistribution and pre-deposit of the emitter).

Typically,

– U_p (pinch-off) = 2–5 V;

– gate leakage current: 10–100 pA.

This technique is widely used for 3.OPs with FET input stages.

– Pb: breakdown voltage V_{GD} ~ 0.7 V (as V_{RE}).

b) Ion-implanted JFETs

Ion implantation makes it possible to distribute impurities in the channel in a precise manner; the profile is well controlled. Good control of the pinch-off voltage is then obtained (which is not the case with double-diffusion JFETs). In addition, the breakdown voltage V_{GD} may be high insofar as the peak of the doping profile is $\simeq 10^6$ at/cm^3.

One way to reduce bias currents is to increase the current gains of the input stages of circuits.

A reduction in base width improves the transport factor ($\propto_T$) of the base and the efficiency of the emitter (γ; current gain increases with the decrease in (W_β):

$$(\propto = \frac{\beta_F}{1+\beta_F} = \propto_T . \gamma \ \ with \propto_T = \frac{1}{1+\frac{W_\beta^2}{2\tau_\beta Dn}} \ \ and \gamma \ = \frac{1}{1+\frac{D_p}{D_n}\frac{W_\beta}{L_p}\frac{W_A}{N_D}} \qquad [1.4]$$

Thus, current gain can be increased by increasing the diffusion time in the emitter or by decreasing the base width. But an increase in the current gain decreases the breakdown voltage B_{CE0} (BV: breakdown voltage).

Flat C-β breakdown voltage

In practice, a standard transistor and a super-beta (b >>100) are constructed on the same surface by a second diffusion. A very narrow base can lead to piercing (punch through; no more neutral base).

MOS transistor

The MOS transistor shows the following characteristics:

– high switching performance;