Lecture Notes in Networks and Systems 908

Amit Joshi
Mufti Mahmud
Roshan G. Ragel
S. Kartik *Editors*

ICT: Applications and Social Interfaces

Proceedings of ICTCS 2023, Volume 1

Springer

Lecture Notes in Networks and Systems

Volume 908

The series "Lecture Notes in Networks and Systems" publishes the latest developments in Networks and Systems—quickly, informally and with high quality. Original research reported in proceedings and post-proceedings represents the core of LNNS.

Volumes published in LNNS embrace all aspects and subfields of, as well as new challenges in, Networks and Systems.

The series contains proceedings and edited volumes in systems and networks, spanning the areas of Cyber-Physical Systems, Autonomous Systems, Sensor Networks, Control Systems, Energy Systems, Automotive Systems, Biological Systems, Vehicular Networking and Connected Vehicles, Aerospace Systems, Automation, Manufacturing, Smart Grids, Nonlinear Systems, Power Systems, Robotics, Social Systems, Economic Systems and other. Of particular value to both the contributors and the readership are the short publication timeframe and the world-wide distribution and exposure which enable both a wide and rapid dissemination of research output.

The series covers the theory, applications, and perspectives on the state of the art and future developments relevant to systems and networks, decision making, control, complex processes and related areas, as embedded in the fields of interdisciplinary and applied sciences, engineering, computer science, physics, economics, social, and life sciences, as well as the paradigms and methodologies behind them.

Indexed by SCOPUS, INSPEC, WTI Frankfurt eG, zbMATH, SCImago.

All books published in the series are submitted for consideration in Web of Science.

For proposals from Asia please contact Aninda Bose (aninda.bose@springer.com).

Amit Joshi · Mufti Mahmud · Roshan G. Ragel ·
S. Kartik
Editors

ICT: Applications and Social Interfaces

Proceedings of ICTCS 2023, Volume 1

Springer

Editors
Amit Joshi
Global Knowledge Research Foundation
Ahmedabad, Gujarat, India

Mufti Mahmud
Nottingham Trent University
Nottingham, UK

Roshan G. Ragel
University of Peradeniya
Galaha, Sri Lanka

S. Kartik
Department of CSE
SNS College of Technology
Coimbatore, Tamil Nadu, India

ISSN 2367-3370 ISSN 2367-3389 (electronic)
Lecture Notes in Networks and Systems
ISBN 978-981-97-0209-1 ISBN 978-981-97-0210-7 (eBook)
https://doi.org/10.1007/978-981-97-0210-7

Preface ICTCS 2023

Eighth International Conference on Information and Communication Technology for Competitive Strategies (ICTCS 2023) targets state-of-the-art as well as emerging topics pertaining to information and communication technologies (ICTs) and effective strategies for its implementation for engineering and intelligent applications.

The conference is anticipated to attract a large number of high-quality submissions, stimulate the cutting-edge research discussions among many academic pioneering researchers, scientists, industrial engineers, students from all around the world and provide a forum to researcher; propose new technologies, share their experiences, and discuss future solutions for design infrastructure for ICT; provide a common platform for academic pioneering researchers, scientists, engineers, and students to share their views and achievements; enrich technocrats and academicians by presenting their innovative and constructive ideas; and focus on innovative issues at international level by bringing together the experts from different countries.

The conference was held during 8 and 9 December 2023, physically at Hotel—Four Points by Sheraton Jaipur, India—and digitally on Zoom organized by Global Knowledge Research Foundation and managed by GR Scholastic LLP.

Research submissions in various advanced technology areas were received, and after a rigorous peer review process with the help of program committee members and external reviewer, 200 papers were accepted with an acceptance rate of 17%. All 200 papers of the conference are accommodated in 5 volumes, also papers in the book comprise authors from 22 countries.

This event success was possible only with the help and support of our team and organizations. With immense pleasure and honor, we would like to express our sincere thanks to the authors for their remarkable contributions, all the Technical Program Committee members for their time and expertise in reviewing the papers within a very tight schedule, and the publisher Springer for their professional help.

We are overwhelmed by our distinguished scholars and appreciate them for accepting our invitation to join us through the virtual platform and deliver keynote speeches and technical session chairs for analyzing the research work presented by the researchers. Most importantly, we are also grateful to our local support team for their hard work for the conference. This series has already been made a continuous series which will be hosted at different locations every year.

Ahmedabad, India — Amit Joshi
Nottingham, UK — Mufti Mahmud
Galaha, Sri Lanka — Roshan G. Ragel
Coimbatore, India — S. Kartik

Contents

Editors and Contributors

About the Editors

Dr. Amit Joshi is currently the Director of Global Knowledge Research Foundation, also an Entrepreneur Researcher who has completed his Masters and research in the areas of cloud computing and cryptography in medical imaging. Dr. Joshi has an experience of around 10 years in academic and industry in prestigious organizations. Dr. Joshi is an active member of ACM, IEEE, CSI, AMIE, IACSIT-Singapore, IDES, ACEEE, NPA and many other professional societies. Currently, Dr. Joshi is the International Chair of InterYIT at International Federation of Information Processing (IFIP, Austria). He has presented and published more than 50 papers in national and international journals/conferences of IEEE and ACM. Dr. Joshi has also edited more than 40 books which are published by Springer, ACM and other reputed publishers. Dr. Joshi has also organized more than 50 national and international conferences and programs in association with ACM, Springer, IEEE to name a few across different countries including India, UK, Europe, USA, Canada, Thailand, Egypt and many more.

Dr. Mufti Mahmud received his Ph.D. degree in Information Engineering (specialized in neuroengineering) from the University of Padova—Italy in 2011. A recipient of the Marie-Curie postdoctoral fellowship, Dr. Mahmud has served at various positions in the industry and academia in India, Bangladesh, Italy, Belgium, and the UK during the last 17 years. Dr. Mahmud aims to leave behind a healthy, secure, and smart world to live in. As an expert of neuroengineering, computational intelligence and data science, his research aims to build predictive, secure and adaptive systems for personalized services to improve quality of life through advancement of healthcare access in low-resource settings. A Senior Member of IEEE and ACM, and Professional Member of BCS, Dr. Mahmud holds leadership roles at many technical committees, such as Vice Chair of the Intelligent System Application Technical Committee of IEEE Computational Intelligence Society, Member of the IEEE CIS

Task Force on Intelligence Systems for Health, Co-Chair of the IEEE P2733 Standard on Intelligent systems design, with AI/ML, Member of the IEEE R8 Humanitarian Activities Subcommittee, and Project Liaison Officer of the IEEE UK and Ireland Special Interest Group on Humanitarian Technology. Dr. Mahmud serves as an Associate Editor of the Cognitive Computation, IEEE Access, Brain Informatics, and Big Data Analytics journals. He also serves at many technical, programme and organisation committees of high-rank conferences including the local organising chair of IEEE-WCCI2020; general chair of BI2020; and programme chair of IEEE-CICARE2020.

Dr. Roshan G. Ragel is a full professor in Computer Engineering at the University of Peradeniya, Sri Lanka. He is a skilled university lecturer and researcher with a doctorate in computer science and engineering and a passion for teaching, research and administration. His research interest is in the areas of fault-tolerant and dependable computing, accelerated and high-performance computing, wearable computing and synthesis of secure and reliable embedded processors. Prof. Ragel received his Ph.D. in Computer Science and Engineering from the University of New South Wales, Australia in 2007 and his B.Sc in Engineering from the University of Peradeniya, Sri Lanka in 2001. He was appointed a Senior Lecturer in Computer Engineering at the University of Peradeniya December 2007 and a full professor since October 2017. Prof. Ragel has co-authored about 150 peer-reviewed articles in topics including Micro- Architectural Support for Reliability and Security in Embedded Processors (SoC), Internet of Things (IoT), Side-Channel Attacks and Countermeasures, Application Specific Processor Design, High-Performance Computing such as Hardware/Software Acceleration of Bioinformatics Algorithms, Wearable Computing, Format-Preserving Digitisation and OCR of Local Language Text, and Completely Automated Public Turing test to tell Computers and Humans Apart (CAPTCHAs) in the Context of Mobile Applications. He has won several best paper awards in conference papers, the most prolific Sri Lankan author award from Elsevier Research in 2017 and the Presidential award for scientific publication in Sri Lanka in 2018. He was a visiting research scholar at the UNSW, Sydney a few times and UIUC, Illinois once. He is a Senior Member of the IEEE and the IEEE Computer Society.

Dr. S. Kartik is presently Professor & Dean in the Department of Computer Science & Engineering, SNS College of Technology, affiliated to Anna University-Chennai, Tamil Nadu, India. He received the M.E. and Ph.D. degree from Anna University, Chennai. His research interests include network security, big data, cloud computing, web services and wireless systems. In particular, he is currently working in a research group developing new Internet security architectures and active defence systems against DDoS attacks. Dr. S. Kartik published more than 200 papers in refereed international journals and 125 papers in conferences and has been involved in many international conferences as Technical Chair and tutorial presenter. He is an active member of IEEE, ISTE, IAENG, IACSIT and Indian Computer Society.

Contributors

Sreejith Alathur Information Systems, Indian Institute of Management Kozhikode, Kunnamangalam, India

T. A. Alka Amrita School of Business, Amrita Vishwa Vidyapeetham, Coimbatore, India

Abhishek Anand Symbiosis Institute of Technology, Symbiosis International (Deemed University), Pune, India

L. Sherly Puspha Annabel Department of Artificial Intelligence and Machine Learning, St. Joseph's College of Engineering, Chennai, 600119, India

Mahin Anup Microsoft India (R&D) Pvt. Ltd., Hyderabad, Telangana, India

Sandhya Arora Cummins College of Engineering, Pune, India

K. Ashwitha Department of MCA, Nitte Meenakshi Institute of Technology, Bangalore, India;
Nitte (Deemed to be University), Deralakatte, Mangalore, India

Sukijan Athoillah Sultan Agung Islamic University, Semarang, Indonesia

Meryeme Ayache STRS Laboratory, National Institute of Posts and Telecommunications (INPT), Rabat, Morocco

Dyuti Banarjee Koneru Lakshmaiah Education Foundation, Vijayawada, Andhra Pradesh, India

Mohamed Bellouch STRS Laboratory, National Institute of Posts and Telecommunications (INPT), Rabat, Morocco

Diptendu Bhattacharya Associate Professor, National Institute of Technology Agartala, Department of Computer Science and Engineering, Agartala, Tripura, India

Pratya Bhowmik National Institute of Technology Agartala, Department of Computer Science and Engineering, Agartala, Tripura, India

Tamal Biswas PHD Scholar, National Institute of Technology Agartala, Department of Computer Science and Engineering, Agartala, Tripura, India

Kaoutar Boussaoud STRS Laboratory, National Institute of Posts and Telecommunications (INPT), Rabat, Morocco

Suneeta V. Budihal ECE, KLE Technological University, Hubli, Karnataka, India

R. Dakshayani Department of Computer Engineering, Fr Conceicao Rodrigues Institute of Technology, Vashi Navi Mumbai, India

Lydia R. Darla Electronics and Communication, KLE Technological University, Hubli, India

Smita Das National Institute of Technology Agartala, Department of Computer Science and Engineering, Agartala, Tripura, India

Nutan Deshmukh Cummins College of Engineering, Pune, India

Abhimanyu Dhiman IEC University, Baddi, Himachal Pradesh, India

Jorge Duque ISLA—Polytechnic Institute of Management and Technology, V. N. Gaia, Portugal

Imadeldin Elsayed Department Electrical and Electronic Engineering, University Malaysia Pahang, Pahang, Malaysia

Abdeslam En-Nouaary STRS Laboratory, National Institute of Posts and Telecommunications (INPT), Rabat, Morocco

Muhammad Farhan Sultan Agung Islamic University, Semarang, Indonesia

Hema Gaikwad Symbiosis Institute of Computer Studies and Research, Symbiosis International (Deemed University), Pune, India

Sharik Gazi Indian Institute of Information Technology Allahabad, Prayagraj, U.P., India

Reena Gupta Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore, Madhya Pradesh, India

Khalid Hamid Department Electronics and Communication, University of Science and Technology, Khartoum, Sudan

Azmil Hashim Universiti Pendidikan Sultan Idris, Tanjong Malim, Malaysia

Mohamed Hassan Department of Wireless Communication, Lovely Professional University, Punjab, India

Wenqi He College of Physics and Optoelectronic Engineering, Shenzhen University, Shenzhen, P. R. China

Miftachul Huda Sultan Idris Education University, Tanjong Malim, Malaysia

Varsha Iyer Symbiosis Institute of Technology, Symbiosis International (Deemed University), Pune, India

Sammita Jadhav Symbiosis Institute of Health Sciences, Symbiosis International (Deemed University), Maharashtra, Pune, India

Vardhaman Jain Symbiosis Institute of Technology, Symbiosis International (Deemed University), Pune, India

Abhishek Karmakar Indian Institute of Information Technology Allahabad, Prayagraj, U.P., India

Kushal B. Kokatnur ECE, KLE Technological University, Hubballi, Karnataka, India

Sonali Kothari Symbiosis Institute of Technology, Symbiosis International (Deemed University), Pune, India

Srinidhi S. Kulkarni ECE, KLE Technological University, Hubballi, Karnataka, India

Ashish Kumar Department of Mathematics and Statistics, Manipal University Jaipur, Jaipur, India

N. G. Hemanth Kumar Department of ECE, B. M. S College of Engineering, Bangalore, India

Nitish Kumar LPU University, Phagwara, Punjab, India

Muhammad Anas Maárif Institut Pesantren KH. Abdul Chalim, Mojokerto, Indonesia

Gouranga Mandal Assistant Professor, Vellore Institute of Technology, Andhra Pradesh, Andhra Pradesh, India

Ruchir Mathur Symbiosis Institute of Technology, Symbiosis International (Deemed University), Pune, India

Mita Mehta Symbiosis Institute of Health Sciences, Symbiosis International (Deemed University), Maharashtra, Pune, India

Ojas Mhatre Department of Computer Engineering, Fr Conceicao Rodrigues Institute of Technology, Vashi Navi Mumbai, India

Deepak Kumar Mishra Amity University Madhya Pradesh, Gwalior, India

O. Mphale University of Botswana, Gaborone, Botswana

Ahmad Muflihin Sultan Agung Islamic University, Semarang, Indonesia

Norhisham Muhamad Universiti Pendidikan Sultan Idris, Tanjong Malim, Malaysia

Fauzi Muharom State Islamic University of Surakarta, Solo, Indonesia

V. Lakshmi Narasimhan Srikar and Associates, Greenville, USA

Nirav M. Patel Department of Civil Engineering, Parul Institute of Engineering and Technology, Parul University, Waghodia, Gujarat, India

Swasti N. Patel Department of Computer Science and Engineering, PIT, Parul University, Waghodia, Gujarat, India

Kanchan Patil Symbiosis Centre for Research and Innovation, Symbiosis International (Deemed University), Pune, India

Xiang Peng College of Physics and Optoelectronic Engineering, Shenzhen University, Shenzhen, P. R. China

Varsha Pimprale Cummins College of Engineering, Pune, India

Md. Golam Rabiul Alam Department of Computer Science and Engineering, BRAC University, Dhaka, Bangladesh

S. Ramaswamy iWorks Corporation, McLean, USA

M. Rohini Department of Information Technology, St. Joseph's College of Engineering, Chennai, India

Srijan Roy M. Tech Student, National Institute of Technology Agartala, Department of Computer Science and Engineering, Agartala, Tripura, India

Rozihan Sultan Agung Islamic University, Semarang, Indonesia

Dwijen Rudrapal Assistant Professor, National Institute of Technology Agartala, Department of Computer Science and Engineering, Agartala, Tripura, India

Smita Rukhande Department of Computer Engineering, Fr Conceicao Rodrigues Institute of Technology, Vashi Navi Mumbai, India

Abinash Sahoo Department of Civil Engineering, OUTR Bhubaneswar, Bhubaneswar, Odisha, India

Jatinderkumar R. Saini Symbiosis Institute of Computer Studies and Research, Symbiosis International (Deemed University), Pune, India

Sandeep Samantaray Department of Civil Engineering, NIT Srinagar, Srinagar, Jammu and Kashmir, India

Tapsi D. Sata Department of Civil Engineering, Parul Institute of Engineering and Technology, Parul University, Waghodia, Gujarat, India

Deba P. Satapathy Department of Civil Engineering, OUTR Bhubaneswar, Bhubaneswar, Odisha, India

K. R. Seeja Department of Computer Science and Engineering, Indira Gandhi Delhi Technical University for Women, Delhi, India

K. Shamshuddin ECE, KLE Technological University, Hubballi, Karnataka, India

D. Monika Sharma Department of ECE, B. M. S College of Engineering, Bangalore, India

Kapil Sharma Amity University Madhya Pradesh, Gwalior, India

Prerna Sharma Department of Computer Science and Engineering, Indira Gandhi Delhi Technical University for Women, Delhi, India

Rahul Sharma Department of Computer Science and Engineering, PIT, Parul University, Waghodia, Gujarat, India

Sanjiv Sharma Madhav Institute of Technology & Science, Gwalior, India

Suresh Sheena School of Humanities, Social Sciences and Management, National Institute of Technology Karnataka, Mangaluru, India

Nidhi Shrivastav Department of Computer Engineering, Fr Conceicao Rodrigues Institute of Technology, Vashi Navi Mumbai, India

Lochana Singh B. K. Birla Institute of Higher Education, Pilani, Rajasthan, India

Abhishek Singhal Amity University Madhya Pradesh, Gwalior, India

Manwinder Singh Department of Wireless Communication, Lovely Professional University, Punjab, India

Varsha Singh Indian Institute of Information Technology Allahabad, Prayagraj, U.P., India

Akruti Sinha North Carolina State University, Raleigh, NC, USA

Deepak Sinwar Department of Computer and Communication Engineering, Manipal University Jaipur, Jaipur, India

Aswathy Sreenivasan Amrita School of Business, Amrita Vishwa Vidyapeetham, Coimbatore, India

Shashi Kant Srivastava Indian Institute of Management Sirmaur, Paonta Sahib, Himachal Pradesh, India

B. Sai Sruthi Department of Information Technology, St. Joseph's College of Engineering, Chennai, India

D. Abdus Subhahan Department of Networking and Communications, College of Engineering and Technology, SRM Institute of Science and Technology, Kattankulathur, Chennai, India

Suraj Symbiosis Centre for Research and Innovation, Symbiosis International (Deemed University), Pune, India

M. Suresh Amrita School of Business, Amrita Vishwa Vidyapeetham, Coimbatore, India

Atharva Suryavanshi Department of Computer Engineering, Fr Conceicao Rodrigues Institute of Technology, Vashi Navi Mumbai, India

S. Sushitha Department of MCA, M. S. Ramaiah Institute of Technology, Bangalore, India

B. Sai Svetha Department of Information Technology, St. Joseph's College of Engineering, Chennai, India

Abhishek Talawar School of Humanities, Social Sciences and Management, National Institute of Technology Karnataka, Mangaluru, India

Nirali G. Tripathi Department of Civil Engineering, Parul Institute of Engineering and Technology, Parul University, Waghodia, Gujarat, India

Masum Uddin Ahmed Department of Computer Science and Engineering, BRAC University, Dhaka, Bangladesh

Deepak Chandra Uprety IEC University, Baddi, Himachal Pradesh, India

M. B. Veena Department of ECE, B. M. S College of Engineering, Bangalore, India

Gaurav Verma Department of Electronics and Communication Engineering, B. K. Birla Institute of Engineering and Technology, Pilani, Rajasthan, India

C. N. S. Vinoth Kumar Department of Networking and Communications, College of Engineering and Technology, SRM Institute of Science and Technology, Kattankulathur, Chennai, India

Arvind Vishnubhatla Electronics and Communications Department, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad, India

Z. A. Tabrani Universitas Serambi Mekkah, Aceh, Indonesia

Controlled Oscillator for ADC Unit

Lydia R. Darla and Suneeta V. Budihal

Abstract We are here proposing a sub-system for the main system the company is working on, which must produce an 84 MHz RF output from a 56 MHz RF input. This is done by using a mixer, harmonic filters, and an external local oscillator input to the system, which is provided to the system in varied steps of 10 kHz frequency to achieve the desired results. A regulated oscillator is crucial to a low-frequency receiver's operation. To modify a signal's frequency to that required by a radio frequency receiver, an oscillator is utilized with a mixer. The effectiveness of a radio frequency receiver is increased by signal processing at a certain frequency.

Keywords Local oscillator · Controlled oscillator · Mixer · RF signal

1 Introduction

The radio receiver is an electrical device used during radio communications that takes up radio waves and turns the data they convey into a usable form. It is often addressed to as a receiver, wireless, or merely a radio. With an antenna, it is utilized. The receiver is subsequently exposed to the antenna's captured radio frequency electromagnetic waves after being transformed into minute alternating currents by the antenna, which subsequently extracts the necessary information. To distinguish the required radio frequency signal from all other signals picked up by the antenna, the receiver uses electronic filters. Electronically boosting a signal's power allows it to be processed further; after that, demodulation retrieves the required data.

A significant system comprises a low-frequency receiver-controlled oscillator. We require a system that can change an input RF frequency from one to the required frequency. The signal's frequency is altered using a local oscillator and a mixer. In

L. R. Darla (✉) · S. V. Budihal
Electronics and Communication, KLE Technological University, Hubli, India
e-mail: dlydia97@gmail.com

S. V. Budihal
e-mail: suneeta_vb@kletech.ac.in

A. Joshi et al. (eds.), *ICT: Applications and Social Interfaces*, Lecture Notes in Networks and Systems 908, https://doi.org/10.1007/978-981-97-0210-7_1

order to enable wireless communication, an integrated radio chip must be affordable and power efficient. In an RF transceiver, a regulated oscillator plays a crucial role [1].

2 Controlled Oscillator Block Diagram

Figure 1 demonstrates to us the controlled oscillator's block diagram. The input signal of 56 MHz must be capable of passing through it with low-pass filter to cut off all unwanted signals above the cut-off frequency.

Here, we use Pi-pad attenuator with equal impedances. A symmetrical attenuator includes the Pi-pad attenuator, whose linear construction permits rotation of its input and output terminals where the network is shaped as Greek letter Π. It is made entirely of passive resistor components. As the Pi-pad attenuator may be positioned between two same impedances, it is ideal for lowering signal levels (ZS = ZL).

The Pi-pad attenuator circuit's resistor allows for impedance matching at any desired attenuation values which are derived using the following equations:

$$N = \frac{V_{in}}{V_{oou}} \tag{1}$$

$$R3 = R_o \frac{N+1}{N-1} \tag{2}$$

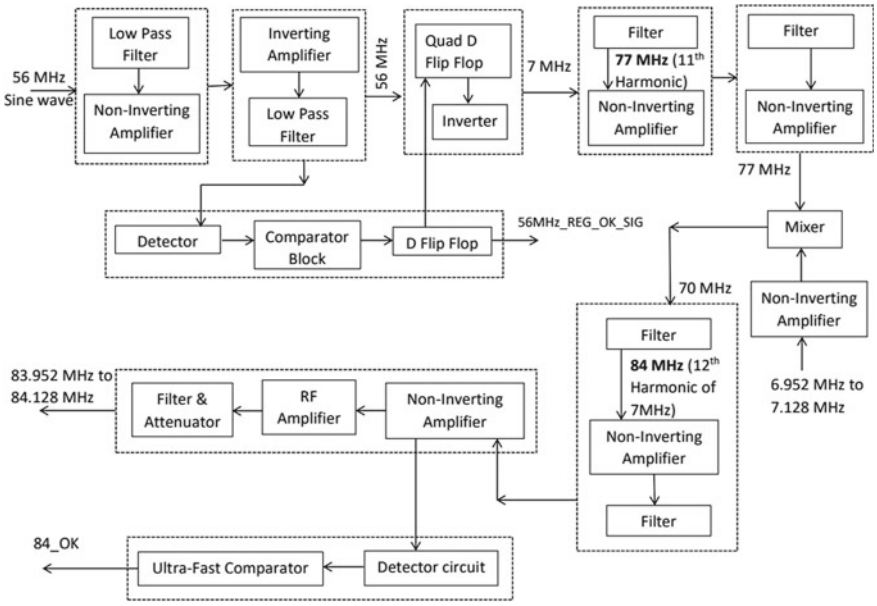

Fig. 1 Block diagram of controlled oscillator

$$R2 = R_o\left(\frac{N^2+1}{2N}\right) \tag{3}$$

where Z is the source or load impedance and K appears to be the impedance factor.

In order to retrieve the exact signal after modulation, a Pi filter is created to pass through the output of the Pi-pad attenuator. Shunt capacitor, an L-section filter that is repeated twice, and a shunt capacitor are all present on the Pi filter's input side. The capacitor receives the output from the preceding component directly. The pulsing DC output voltage is filtered in that order by the input side capacitor, a choke coil, and a second shunt capacitor. The way the components are put together resembles the Greek letter Pi. This leads to the Pi filter. The capacitor is also located on the input side. There are more configurations available, even though low-pass filters are the most typical application for Pi filters. The main components of a Pi filter, which is an LC filter, a capacitor, and an inductor. As a result, it is often referred to as a capacitor input filter.

The signal is then sent via a non-inverting amplifier after that. The power supply for this non-inverting amplifier is 5 V, accordingly. Gain is 2 dB for the non-inverting amplifier. The non-inverting amplifier offers six separate inverters with standard push–pull outputs. The device is designed to operate with power sources ranging from 2.0 V to 6.0 V.

The main contributors to the op-amplification are the two feedback resistors R2 and R6, which are connected in a voltage divider arrangement. A feedback resistor is what is known as this R6 resistor (Rf). The output of the voltage divider that is connected to the operational amplifier's inverting pin is identical to V_{in} since V_{in} and the voltage divider's junction points are placed across a shared ground node. As a result, the V_{out} is reliant on the feedback network.

You may represent the amount of current flowing through the R2 resistor as V_{in}/R2 to get the voltage gain. Since neither of the inputs pulls any current in accordance with the current rule to find the current flowing over the branch, here the current will flow over R6.

$V_{out} = V_{in} + (V_{in}/R2)*R6$ may then be used to compute the output voltage (Vo). A non-inverting op-gain amp's is calculated using the formula $Av = V_{out}/V_{in} = 1 +$ (R6/R2). In this case, the gain value shouldn't be less than 1. Thus, the non-inverting op-enhanced amp's signal will be in phase with the input.

The inverting amplifier receives the output from the non-inverting amplifier. The inverting operational amplifier is simply a constant or fixed-gain amplifier with a negative output voltage since its gain is always negative.

Because the open-loop DC gain of an operational amplifier is unusually high, the total gain of the amplifier can be limited and regulated by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal. This leads in what is typically referred to as negative feedback, which creates an operational amplifier-based system that is highly stable.

Due to the influence of a closed-loop circuit on the amplifier, the gain of the device is now referred to as its closed-loop gain. The amplifier's gain is then decreased by

a closed-loop inverting amplifier at the price of properly managing the amplifier's total gain.

Since the input voltage and the negative feedback voltage are summed together, giving the terminal the moniker of a summation point, the inverting input terminal experiences a signal that is different from the input voltage as a result of the negative feedback. In order to separate the real input signal from the inverting input, we must employ an input resistor (R_{in}).

The equation's negative sign indicates that the output signal is inverted since it is 180° out of phase with the input. This is due to the poor value of the feedback. The equation for the output voltage, V_{out}, also shows that the circuit is linear for a fixed amplifier gain since $V_{out} = V_{in} \times$ Gain. This property may be very useful when converting a little sensor signal to a much higher voltage.

$$
\begin{aligned}
i &= \frac{V_{in} - V_{out}}{R_{in} + R_f} \\
\text{hence, } i &= \frac{V_{in} - V2}{R_{in}} = \frac{V2 - V_{out}}{R_f} \\
i &= \frac{V_{in}}{R_{in}} - \frac{V2}{R_{in}} = \frac{V2}{R_f} - \frac{V_{out}}{R_f} \\
\frac{V_{in}}{R_{in}} &= V2\left[\frac{1}{R_{in}} + \frac{1}{R_f}\right] - \frac{V_{out}}{R_f} \\
i &= \frac{V_{in} - 0}{R_{in}} = \frac{0 - V_{out}}{R_f}\frac{R_f}{R_{in}} = \frac{0 - V_{out}}{V_{in} - 0}
\end{aligned}
\tag{4}
$$

the closed-loop gain is given by

$$
\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}} \tag{5}
$$

In order to determine the voltage gain, function is performed by the gate: Y = A.

In this case, a T-pad attenuator with equal impedances is being used. Therefore, the resistors R17 and R20 in resistive network have the same value because it is possible to reverse the input and output terminals. Because of this, the T-pad attenuator works well to lower signal levels when put between two impedances that have the same value (ZS = ZL).

The three resistive parts are used in this case to ensure that the input and output impedances match the load impedance that is a part of the attenuator network. Because the input and output impedances of the T-pad are specifically designed to match the load, this figure is referred to as the "characteristic impedance" of the symmetrical T-pad network. The following formulae are provided to calculate the resistor values for a T-pad attenuator circuit used for impedance matching at any given attenuation:

$$R1 = R2 = Z\left(\frac{K-1}{K+1}\right) \tag{6}$$

$$R3 = 2Z\left(\frac{K}{K^2-1}\right) \tag{7}$$

where K is the impedance factor and Z is the source/load impedance.

The T-pad attenuator's signal is being amplified by a capacitor since an AC-coupled source is required to drive the pin. This signal is delivered to the detector IC's RFIN pin. This experiment used a mean-responding power detector for use in high-frequency receiver and transmitter signal chains, up to 2.5 GHz. Applying is fairly easy. A single supply between 2.7 V and 5.5 V, a power supply decoupling capacitor, and an input coupling capacitor are all that are often required. The output is a linear-responding DC voltage with a 7.5 V/V rms conversion gain. An external capacitor to the filter is added to increase the average time constant.

The VPOS pin is isolated using 100 pF and 0.01 F capacitors. The input impedance for the AC-coupled device is paired with a 75 external shunt resistance to provide a nearly 50 overall broadband input impedance. The high-pass corner frequency indicated by the equation is created by the interaction of the internal input resistance and input coupling capacitor:

$$f_{3dB} = \frac{1}{2\pi \times C_c \times R_{IN}} \tag{8}$$

The VRMS pin receives the detector's output, which is then supplied to the comparator block's IN + pin. A high signal is supplied to the comparator block when the 56 MHz signal is detected. The high signal is received by the comparator block, which then compares it to the reference voltage of 1.73 V. The QA pin is set HIGH and connected to the dual flip-flop's RESET pin if the signal exceeds the reference voltage.

In the inverting amplifier, the output signal is 180° phase shifted and a gain of − 3.1 dB is added to the signal. This output is given to a quad flip-flop as clock pulse through a low-pass filter and also a detector block as discussed earlier. This signal is given to the RFIN pin of detector IC. The signal is sent through a voltage divider network passing through a capacitor as the pin must be driven from an AC-coupled source. When IREF pin is open, the Internal Reference Mode is enabled (as per the datasheet). A 5 V positive supply is given to the VPOS pin of the IC, the output of the detector is taken from the VRMS pin and fed to the IN + pin of the comparator block. When the signal of 56 MHz is detected a High Signal is sent to the comparator block.

The IC must be properly designed and laid out in order to work at their best with a high-speed comparator or amplifier. High-speed circuitry's maximum performance may be constrained by excessive stray capacitance or poor grounding. The latch input of the IC can store data at the comparator's output when the VCC supply is at a

nominal 5 V. The output voltage maintains its prior condition while the latch voltage is high, regardless of changes in the input voltage.

The IC's setup and hold times are each 0.5 ns. The minimal amount of time the input voltage must remain in a valid state prior to the latch being activated for the latch to operate as intended is known as setup time. Hold time is the amount of time after the latch voltage spikes that the input must remain stable in order for the output to stay latched to that voltage. A logic high is defined as having a minimum voltage of 2.0 V and a maximum voltage of 0.8 V for the latch input, which is TTL and CMOS compatible. There is no hysteresis built into the latch circuitry in the IC.

The IC typically has an input capacitance of 3 pF. A 5 k source resistance is connected in series with the input to monitor the propagation delay change.

The inverting input of the comparator is directly connected to the input signal. Through R1 and R2, the output is fed back into the non-inverting input. The hysteresis window's width is determined by the relationship between R1 and R1 + R2, while the window's center, or average switching voltage, is determined by VREF. According to Eq. 1, the QA or QB output switches low when the input voltage is higher than VHI and does not switch high again until the input voltage is lower than VLO.

The Comparator Block receives the high signal and compares it with the reference voltage of 1.73 V. If the signal is greater than the reference voltage, the QA pin is set HIGH and is given to the RESET pin of the dual flip-flop (Fig. 2).

The output from the comparator is given as the input to the dual flip-flop 2 at the RESET pin. The output of the inverting amplifier is given as the clock input to the dual flip-flop. When the RESET pin of the second flip-flop goes HIGH it makes the Transistor Q1 go HIGH, which in turn makes the RESET pin of dual flip-flop 1 go HIGH. Hence, the Q1 goes HIGH to enable divider, i.e., quad flip-flop. We cross-check if the 56 MHz signal is present or not using a test point at the /Q1 pin of the dual flip-flop, as per the data given in Table 1, we can find the status. The output of the dual flip-flop is also given as input to the quad flip-flop.

The output frequency of 84 MHz from the filter is also given to detector block. This signal is given to the detector IC. The signal is sent from a voltage divider network passing through a capacitor as the pin must be driven from an AC-coupled source. Later it is given to the RFIN pin of the IC. When IREF pin is open, the Internal Reference Mode is enabled. When the signal is detected, a high signal from VRMS is sent to the comparator block. The comparator block receives the high signal and

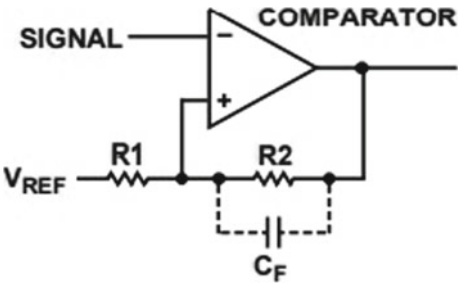

Fig. 2 Configuring the comparator IC with hysteresis

Table 1 Obtained output frequency values for the given input radio frequency signal

RF input in MHz	Local oscillator input in MHz	Output frequency in MHz
56	6.98	83.98
56	6.99	83.99
56	7.00	84.00
56	7.01	84.01
56	7.02	84.02
56	6.98	83.98

compares it with the reference voltage 3.33 V. The output of the comparator gives us the OK signal which tells us that the 84 MHz signal is received as expected.

The output from the inverting amplifier is given to the input to the master reset pin of the quad flip-flop. The output from the low-pass filter is given as the clock input to the quad flip-flop. The quad flip-flop has four flip-flops. The flip-flops are connected in a way that they are cascaded. Here we use only three flip-flops to attain the desired signal. The signal is taken from /Q1 as the frequency is each divided by three times. The output here is in the form of square waveform.

A high-speed quad D-type flip-flop is the quad flip-flop IC. When universal flip-flop requirements exist and clock and clear inputs are frequently used, the device is helpful. During the LOW-to-HIGH clock transition, the data on the D-type inputs is saved. Each flip-flop has true and supplemented outputs available.

When LOW, a Master Reset input resets all flip-flops without regard to the clock or D-type inputs.

It is possible to create a divide by N with a 50% duty cycle using a ringed arrangement with N of the flip-flops that are triggered at the specialized level. Even if N is an odd number, this still holds true. The outputs of the flip-flops can be made to transition on either a rising or falling edge by dynamically driving the 0 inputs of the flip-flops, depending on the state of other flip-flops in the circuit. The feedback is flipped, and each flip-flop's output controls the input of the one after it. Each flip-flop's input receives input from the flip-flop after it.

Hence, when the 56 MHz frequency is divided by three times we attain our required output which is 7 MHz. The output here is in the shape of a square signal which is made to pass an inverter again to bring the phase shift back to its original state. The output from the inverter is further sent to the filter for harmonic functions.

This square wave output is given as input to the next block. This signal is made to pass through a filter. The filter gives an output of 77 MHz. The output from the filter is given to a non-inverting amplifier with an additional gain of 5.88 dB. The output of the non-inverting amplifier is again given to the filter. The output is given to the non-inverting amplifier with an additional gain of 5.88 dB.

An external input of 6.952–7.128 MHz is given from the local oscillator which is a varying frequency in order to collect the result analysis. This signal is conditioned and sent to the mixer block for further filtering.

In a communication system, the local oscillator (LO) path supplies the mixing tone for up-converting low-frequency modulated signals in the transmitter and down-converting received signals in order to demodulate them. On LO channel frequencies may interfere and contaminate each other. Signals that were received and delivered require the employment of an off LO channel dividing the LO is one technique to prevent this by three, then to double or quadruple the frequency. By doing this, it is ensured that neither the LO nor any of its harmonics relate to the transmitted or received frequency [2].

The output from the non-inverting amplifier is given as input to the local oscillator input pin (LON) of mixer.

The mixer IC is a low distortion, wide dynamic range, monolithic mixer used in a variety of processes, including direct-to-baseband conversion, quadrature modulation and demodulation, and doppler shift detection in ultrasound imaging applications. It is also used as the second mixer in DMR base stations. The mixer has a third-order intercept point and user-programmable power consumption. It also has a LO driver and a low-noise output amplifier.

When compared to passive mixers, the AD831 offers a +24 dBm third-order intercept point for a −10 dBm LO power, enhancing system performance and lowering system costs by doing away with the necessity for a high-power LO driver and the associated shielding and isolation issues. When the mixer is powered by 5 V supplies, the RF, IF, and LO ports can be either DC or AC coupled or AC coupled when powered by a single 9 V minimum supply. Up to 500 MHz of RF and LO inputs are supported by the mixer.

At 70 MHz, the mixer's SSB noise figure is 10.3 dB when its output amplifier and ideal source impedance are used. The mixer does not have insertion loss, a passive termination, or an external diplexer, in contrast to passive mixers.

When the RF and LO inputs are ac coupled, an on-chip network provides the bias current; this network is removed when the mixer is dc coupled. An external frequency of 7 MHz is given to the RF input pin (RFP) of the mixer. Both of these inputs are subtracted from each other and an output of 70 MHz is obtained. Hence, the mixer gives an output of 70 MHz.

The output from the RF amplifier is given as an input to the filter and the attenuator block. Attenuators (or attenuator pads) are used, for example, at the input of an electronic instrument in order to reduce a voltage or current to a value which can be handled by the instrument.

A filter is a circuit which attenuates certain frequencies, while allowing others to pass with very little attenuation. The final output from this block will be 83.952–84.128 MHz.

3 Results

The RF input value is 56 MHz. This value is kept constant by keeping the constant input frequency of 56 MHz and the local oscillator's values varying through 6.952 MHz and 7.128 MHz in steps of 10 kHz which can be seen in Table 1.

The challenges faced during the implementation was to maintain the efficiency of the system with respect to the components that were used such as the amplifiers and mixers.

The selection of specific components is made in the proposed system by ensuring there is enough negative resistance to start oscillations and help them develop into steady states in the design process. Next, the entire closed-loop oscillator circuit is examined. The component values mentioned above have been designed to make a circuit capable of oscillating at desired frequencies.

References

1. Selvajyothi K, Janakiraman PA (2008) Extraction of harmonics using composite observers. IEEE 23(1)
2. Magoon R, Molnar A (2002) RF local oscillator path for GSM direct conversion transceiver with true 50 percent duty cycle divide by three and active third harmonic cancellation. IEEE

Person Identification Through Ear Biometrics—A Systematic Survey

Prerna Sharma and K. R. Seeja

Abstract Biometrics plays a significant role in many sectors of modern society, like banking transactions, person identification, and surveillance. The ear is used as a biometric trait because the human ear shape is stable between the ages of 8 and 70 and has a uniform color distribution. Ear is visible even after wearing a face mask. Ear biometrics is an example of passive biometrics as it can be used for person identification without their knowledge. Hence, it can be used to develop a completely automatic biometric authentication system. In this paper, the state-of-the-art literature on ear biometrics from 2010 is critically reviewed. This literature review also covers various studies on ear detection, feature extraction, and classification techniques, as well as the various benchmark datasets available for ear biometric research. The intuition, methodology, limitations, and future scope of these articles have been summarized. Finally, major challenges and future scopes of ear biometrics have also been discussed. Hence, this review will provide an overview for researchers interested in further research in this domain.

Keywords Ear biometrics · Ear detection · Person identification

1 Introduction

Biometrics is a field in which identification can be made based on the physical or behavioral characteristics of a person. In terms of physical traits, face and fingerprints gave the most promising results, but in the case of surveillance, they are not feasible because they belong to active biometrics. Ear biometrics has also gained popularity in the last decade due to many reasons like ear is a unique trait [1] and it can be used

P. Sharma (✉) · K. R. Seeja
Department of Computer Science and Engineering, Indira Gandhi Delhi Technical University for Women, Kashmere Gate, Delhi, India
e-mail: sharma.prerna.13spt@gmail.com

K. R. Seeja
e-mail: seeja@igdtuw.ac.in

A. Joshi et al. (eds.), *ICT: Applications and Social Interfaces*, Lecture Notes in Networks and Systems 908, https://doi.org/10.1007/978-981-97-0210-7_2

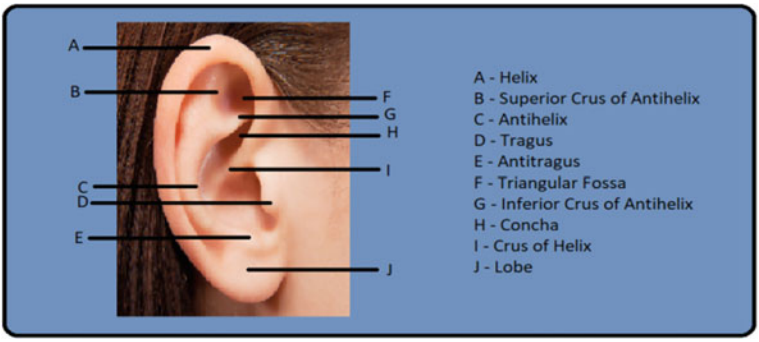

Fig. 1 Basic structure of the ear

for person identification purposes for forensic science [2]. The basic ear structure of a person is depicted in Fig. 1.

Ear biometrics is suitable over other modalities because the human ear shape is stable between 8 and 70 years [3]. For passive biometrics, ear biometrics is a good choice because less or even no cooperation is needed from the user. Images can be captured at far distances without any cooperation from the user. Hence, it is a suitable option for surveillance purposes [2]. They are free from expressions, make-up, masks, and they are contactless biometrics which helps in the prevention of COVID-19 virus [4]. In the case of occluded ear images, body heat patterns can help to detect the location of the ear; this can be achieved through infrared images [5]. According to Amazon's patent idea, phone calls can be answered directly after scanning and matching the ear images of the person when you put the phone on the ear; there is no need to answer manually [4].

1.1 Ear Biometrics System

A Basic Ear Biometrics system flow can be elaborated through Fig. 2.

This article is organized into sections: Image acquisition covers benchmark ear datasets and the next section is pre-processing. In the next phases, techniques of ear detection, feature extraction, and person identification were critically reviewed.

Gupta [6] introduced the concept of ear cavity and addressed various drawbacks in ear detection and recognition due to occlusion in images. Abaza [7] presented a detailed review of ear biometrics that focuses on the ear detection and recognition

Fig. 2 Basic ear biometrics system