



MACHINE LEARNING TECHNIQUES FOR VLSI CHIP DESIGN

Edited By
Abhishek Kumar, Suman Lata Tripathi
and K. Srinivasa Rao

Machine Learning for VLSI Chip Design

Scrivener Publishing

100 Cummings Center, Suite 541J
Beverly, MA 01915-6106

Publishers at Scrivener

Martin Scrivener (martin@scrivenerpublishing.com)
Phillip Carmical (pcarmical@scrivenerpublishing.com)

Machine Learning for VLSI Chip Design

Edited by
Abhishek Kumar
Suman Lata Tripathi
and
K. Srinivasa Rao



WILEY

This edition first published 2023 by John Wiley & Sons, Inc., 111 River Street, Hoboken, NJ 07030, USA and Scrivener Publishing LLC, 100 Cummings Center, Suite 541J, Beverly, MA 01915, USA

© 2023 Scrivener Publishing LLC

For more information about Scrivener publications please visit www.scrivenerpublishing.com.

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, except as permitted by law. Advice on how to obtain permission to reuse material from this title is available at <http://www.wiley.com/go/permissions>.

Wiley Global Headquarters

111 River Street, Hoboken, NJ 07030, USA

For details of our global editorial offices, customer services, and more information about Wiley products visit us at www.wiley.com.

Limit of Liability/Disclaimer of Warranty

While the publisher and authors have used their best efforts in preparing this work, they make no representations or warranties with respect to the accuracy or completeness of the contents of this work and specifically disclaim all warranties, including without limitation any implied warranties of merchantability or fitness for a particular purpose. No warranty may be created or extended by sales representatives, written sales materials, or promotional statements for this work. The fact that an organization, website, or product is referred to in this work as a citation and/or potential source of further information does not mean that the publisher and authors endorse the information or services the organization, website, or product may provide or recommendations it may make. This work is sold with the understanding that the publisher is not engaged in rendering professional services. The advice and strategies contained herein may not be suitable for your situation. You should consult with a specialist where appropriate. Neither the publisher nor authors shall be liable for any loss of profit or any other commercial damages, including but not limited to special, incidental, consequential, or other damages. Further, readers should be aware that websites listed in this work may have changed or disappeared between when this work was written and when it is read.

Library of Congress Cataloging-in-Publication Data

ISBN 9781119910398

Front cover images supplied by Pixabay.com

Cover design by Russell Richardson

Set in size of 11pt and Minion Pro by Manila Typesetting Company, Makati, Philippines

Printed in the USA

10 9 8 7 6 5 4 3 2 1

Contents

List of Contributors	xiii
Preface	xix
1 Applications of VLSI Design in Artificial Intelligence and Machine Learning	1
<i>Imran Ullah Khan, Nupur Mittal and Mohd. Amir Ansari</i>	
1.1 Introduction	2
1.2 Artificial Intelligence	4
1.3 Artificial Intelligence & VLSI (AI and VLSI)	4
1.4 Applications of AI	4
1.5 Machine Learning	5
1.6 Applications of ML	6
1.6.1 Role of ML in Manufacturing Process	6
1.6.2 Reducing Maintenance Costs and Improving Reliability	6
1.6.3 Enhancing New Design	7
1.7 Role of ML in Mask Synthesis	7
1.8 Applications in Physical Design	8
1.8.1 Lithography Hotspot Detection	9
1.8.2 Pattern Matching Approach	9
1.9 Improving Analysis Correlation	10
1.10 Role of ML in Data Path Placement	12
1.11 Role of ML on Route Ability Prediction	12
1.12 Conclusion	13
References	14
2 Design of an Accelerated Squarer Architecture Based on Yavadunam Sutra for Machine Learning	19
<i>A.V. Ananthalakshmi, P. Divyaparameswari and P. Kanimozhi</i>	
2.1 Introduction	20
2.2 Methods and Methodology	21
2.2.1 Design of an n-Bit Squaring Circuit Based on (n-1)-Bit Squaring Circuit Architecture	22

2.2.1.1	Architecture for Case 1: $A < B$	22
2.2.1.2	Architecture for Case 2: $A > B$	24
2.2.1.3	Architecture for Case 3: $A = B$	24
2.3	Results and Discussion	25
2.4	Conclusion	29
	References	30
3	Machine Learning–Based VLSI Test and Verification	33
	<i>Jyoti Kandpal</i>	
3.1	Introduction	33
3.2	The VLSI Testing Process	35
3.2.1	Off-Chip Testing	35
3.2.2	On-Chip Testing	35
3.2.3	Combinational Circuit Testing	36
3.2.3.1	Fault Model	36
3.2.3.2	Path Sensitizing	36
3.2.4	Sequential Circuit Testing	36
3.2.4.1	Scan Path Test	36
3.2.4.2	Built-In-Self Test (BIST)	36
3.2.4.3	Boundary Scan Test (BST)	37
3.2.5	The Advantages of VLSI Testing	37
3.3	Machine Learning’s Advantages in VLSI Design	38
3.3.1	Ease in the Verification Process	38
3.3.2	Time-Saving	38
3.3.3	3Ps (Power, Performance, Price)	38
3.4	Electronic Design Automation (EDA)	39
3.4.1	System-Level Design	40
3.4.2	Logic Synthesis and Physical Design	42
3.4.3	Test, Diagnosis, and Validation	43
3.5	Verification	44
3.6	Challenges	47
3.7	Conclusion	47
	References	48
4	IoT-Based Smart Home Security Alert System for Continuous Supervision	51
	<i>Rajeswari, N. Vinod Kumar, K. M. Suresh, N. Sai Kumar and K. Girija Sravani</i>	
4.1	Introduction	52
4.2	Literature Survey	53
4.3	Results and Discussions	54

4.3.1	Raspberry Pi-3 B+Module	54
4.3.2	Pi Camera	56
4.3.3	Relay	56
4.3.4	Power Source	56
4.3.5	Sensors	56
4.3.5.1	IR & Ultrasonic Sensor	56
4.3.5.2	Gas Sensor	56
4.3.5.3	Fire Sensor	57
4.3.5.4	GSM Module	57
4.3.5.5	Buzzer	57
4.3.5.6	Cloud	57
4.3.5.7	Mobile	57
4.4	Conclusions	62
	References	62
5	A Detailed Roadmap from Conventional-MOSFET to Nanowire-MOSFET	65
	<i>P. Kiran Kumar, B. Balaji, M. Suman, P. Syam Sundar, E. Padmaja and K. Girija Sravani</i>	
5.1	Introduction	66
5.2	Scaling Challenges Beyond 100nm Node	67
5.3	Alternate Concepts in MOFSETs	69
5.4	Thin-Body Field-Effect Transistors	70
5.4.1	Single-Gate Ultrathin-Body Field-Effect Transistor	71
5.4.2	Multiple-Gate Ultrathin-Body Field-Effect Transistor	73
5.5	Fin-FET Devices	74
5.6	GAA Nanowire-MOSFETS	77
5.7	Conclusion	86
	References	86
6	Gate All Around MOSFETs-A Futuristic Approach	95
	<i>Ritu Yadav and Kiran Ahuja</i>	
6.1	Introduction	95
6.1.1	Semiconductor Technology: History	96
6.2	Importance of Scaling in CMOS Technology	98
6.2.1	Scaling Rules	99
6.2.2	The End of Planar Scaling	100
6.2.3	Enhance Power Efficiency	101
6.2.4	Scaling Challenges	102
6.2.4.1	Poly Silicon Depletion Effect	102
6.2.4.2	Quantum Effect	103

6.2.4.3	Gate Tunneling	103
6.2.5	Horizontal Scaling Challenges	103
6.2.5.1	Threshold Voltage Roll-Off	103
6.2.5.2	Drain Induce Barrier Lowering (DIBL)	103
6.2.5.3	Trap Charge Carrier	104
6.2.5.4	Mobility Degradation	104
6.3	Remedies of Scaling Challenges	104
6.3.1	By Channel Engineering (Horizontal)	104
6.3.1.1	Shallow S/D Junction	105
6.3.1.2	Multi-Material Gate	105
6.3.2	By Gate Engineering (Vertical)	105
6.3.2.1	High-K Dielectric	105
6.3.2.2	Metal Gate	105
6.3.2.3	Multiple Gate	105
6.4	Role of High-K in CMOS Miniaturization	106
6.5	Current Mosfet Technologies	108
6.6	Conclusion	108
	References	109
7	Investigation of Diabetic Retinopathy Level Based on Convolution Neural Network Using Fundus Images	113
	<i>K. Sasi Bhushan, U. Preethi, P. Naga Sai Navya, R. Abhilash, T. Pavan and K. Girija Sravani</i>	
7.1	Introduction	114
7.2	The Proposed Methodology	115
7.3	Dataset Description and Feature Extraction	116
7.3.1	Depiction of Datasets	116
7.3.2	Preprocessing	116
7.3.3	Detection of Blood Vessels	117
7.3.4	Microaneurysm Detection	118
7.4	Results and Discussions	120
7.5	Conclusions	123
	References	123
8	Anti-Theft Technology of Museum Cultural Relics Using RFID Technology	127
	<i>B. Ramesh Reddy, K. Bhargav Manikanta, P.V.V.N.S. Jaya Sai, R. Mohan Chandra, M. Greeshma Vyas and K. Girija Sravani</i>	
8.1	Introduction	128

8.2	Literature Survey	128
8.3	Software Implementation	129
8.4	Components	130
8.4.1	Arduino UNO	130
8.4.2	EM18 Reader Module	130
8.4.3	RFID Tag	131
8.4.4	LCD Display	131
8.4.5	Sensors	132
8.4.5.1	Fire Sensor	132
8.4.5.2	IR Sensor	132
8.4.6	Relay	133
8.5	Working Principle	134
8.5.1	Working Principle	134
8.6	Results and Discussions	135
8.7	Conclusions	137
	References	138
9	Smart Irrigation System Using Machine Learning Techniques	139
	<i>B. V. Anil Sai Kumar, Suryavamsham Prem Kumar, Konduru Jaswanth, Kola Vishnu and Abhishek Kumar</i>	
9.1	Introduction	139
9.2	Hardware Module	141
9.2.1	Soil Moisture Sensor	141
9.2.2	LM35-Temperature Sensor	143
9.2.3	POT Resistor	143
9.2.4	BC-547 Transistor	143
9.2.5	Sounder	144
9.2.6	LCD 16x2	145
9.2.7	Relay	145
9.2.8	Push Button	146
9.2.9	LED	146
9.2.10	Motor	147
9.3	Software Module	148
9.3.1	Proteus Tool	148
9.3.2	Arduino Based Prototyping	149
9.4	Machine Learning (ML) Into Irrigation	155
9.5	Conclusion	158
	References	158

10	Design of Smart Wheelchair with Health Monitoring System	161
	<i>Narendra Babu Alur, Kurapati Poorna Durga, Boddu Ganesh, Manda Devakaruna, Lakkimsetti Nandini, A. Praneetha, T. Satyanarayana and K. Girija Sravani</i>	
10.1	Introduction	162
10.2	Proposed Methodology	163
10.3	The Proposed System	164
10.4	Results and Discussions	168
10.5	Conclusions	169
	References	169
11	Design and Analysis of Anti-Poaching Alert System for Red Sandalwood Safety	171
	<i>K. Rani Rudrama, Mounika Ramala, Poorna sasank Galaparti, Manikanta Chary Darla, Siva Sai Prasad Loya and K. Srinivasa Rao</i>	
11.1	Introduction	172
11.2	Various Existing Proposed Anti-Poaching Systems	173
11.3	System Framework and Construction	174
11.4	Results and Discussions	176
11.5	Conclusion and Future Scope	182
	References	182
12	Tumor Detection Using Morphological Image Segmentation with DSP Processor TMS320C6748	185
	<i>T. Anil Raju, K. Srihari Reddy, Sk. Arifulla Rabbani, G. Suresh, K. Saikumar Reddy and K. Girija Sravani</i>	
12.1	Introduction	186
12.2	Image Processing	186
	12.2.1 Image Acquisition	186
	12.2.2 Image Segmentation Method	186
12.3	TMS320C6748 DSP Processor	187
12.4	Code Composer Studio	188
12.5	Morphological Image Segmentation	188
	12.5.1 Optimization	190
12.6	Results and Discussions	192
12.7	Conclusions	193
	References	193
13	Design Challenges for Machine/Deep Learning Algorithms	195
	<i>Rajesh C. Dharmik and Bhushan U. Bawankar</i>	
13.1	Introduction	196
13.2	Design Challenges of Machine Learning	197

13.2.1	Data of Low Quality	197
13.2.2	Training Data Underfitting	197
13.2.3	Training Data Overfitting	198
13.2.4	Insufficient Training Data	198
13.2.5	Uncommon Training Data	199
13.2.6	Machine Learning Is a Time-Consuming Process	199
13.2.7	Unwanted Features	200
13.2.8	Implementation is Taking Longer Than Expected	200
13.2.9	Flaws When Data Grows	200
13.2.10	The Model's Offline Learning and Deployment	200
13.2.11	Bad Recommendations	201
13.2.12	Abuse of Talent	201
13.2.13	Implementation	201
13.2.14	Assumption are Made in the Wrong Way	202
13.2.15	Infrastructure Deficiency	202
13.2.16	When Data Grows, Algorithms Become Obsolete	202
13.2.17	Skilled Resources are Not Available	203
13.2.18	Separation of Customers	203
13.2.19	Complexity	203
13.2.20	Results Take Time	203
13.2.21	Maintenance	204
13.2.22	Drift in Ideas	204
13.2.23	Bias in Data	204
13.2.24	Error Probability	204
13.2.25	Inability to Explain	204
13.3	Commonly Used Algorithms in Machine Learning	205
13.3.1	Algorithms for Supervised Learning	205
13.3.2	Algorithms for Unsupervised Learning	206
13.3.3	Algorithm for Reinforcement Learning	206
13.4	Applications of Machine Learning	207
13.4.1	Image Recognition	207
13.4.2	Speech Recognition	207
13.4.3	Traffic Prediction	207
13.4.4	Product Recommendations	208
13.4.5	Email Spam and Malware Filtering	208
13.5	Conclusion	208
	References	208
	About the Editors	211
	Index	213

List of Contributors

Imran Ullah Khan

Dept. of Electronics and Communication Engineering, Integral University,
Lucknow, India

Nupur Mittal

Dept. of Electronics and Communication Engineering, Integral University,
Lucknow, India

Mohd. Amir Ansari

Dept. of Electronics and Communication Engineering, Integral University,
Lucknow, India

A.V. Ananthalakshmi

Department of ECE, Puducherry Technological University, Puducherry,
India

P. Divyaparameswari

Department of ECE, Puducherry Technological University, Puducherry,
India

P. Kanimozhi

Department of ECE, Puducherry Technological University, Puducherry,
India

Jyoti Kandpal

Dept. of Electronics and Communication Engineering, NIT Arunachal
Pradesh, India

Rajeswari

Department of ECE, Lakireddy Bali Reddy College of Engineering,
Mylavaram, India

N. Vinod Kumar

Department of ECE, Lakireddy Bali Reddy College of Engineering,
Mylavaram, India

K. M. Suresh

Department of ECE, Lakireddy Bali Reddy College of Engineering,
Mylavaram, India

N. Sai Kumar

Department of ECE, Lakireddy Bali Reddy College of Engineering,
Mylavaram, India

K. Girija Sravani

Department of ECE, KL University, Green Fields, Guntur-522502, Andhra
Pradesh, India

P. Kiran Kumar

Koneru Lakshmaiah Educational Foundation (Deemed to be University),
Guntur, Andhra Pradesh-522502, India

B. Balaji

Koneru Lakshmaiah Educational Foundation (Deemed to be University),
Guntur, Andhra Pradesh-522502, India

M. Suman

Koneru Lakshmaiah Educational Foundation (Deemed to be University),
Guntur, Andhra Pradesh-522502, India

P. Syam Sundar

Koneru Lakshmaiah Educational Foundation (Deemed to be University),
Guntur, Andhra Pradesh-522502, India

E. Padmaja

Koneru Lakshmaiah Educational Foundation (Deemed to be University),
Guntur, Andhra Pradesh-522502, India

Ritu Yadav

ECE Department, I K Gujral Punjab Technical University, Jalandhar, India

Kiran Ahuja

ECE Department, DAVIET, Jalandhar, India

K. Sasi Bhushan

Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India, 521230

U. Preethi

Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India, 521230

P. Naga Sai Navya

Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India, 521230

R. Abhilash

Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India, 521230

T. Pavan

Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India, 521230

B. Ramesh Reddy

Department of Electronics and Communication Engineering, LBR College of Engineering, Mylavaram, Krishna District, Andhra Pradesh

K. Bhargav Manikanta

Department of Electronics and Communication Engineering, LBR College of Engineering, Mylavaram, Krishna District, Andhra Pradesh

P.V.V.N.S. Jaya Sai

Department of Electronics and Communication Engineering, LBR College of Engineering, Mylavaram, Krishna District, Andhra Pradesh

R. Mohan Chandra

Department of Electronics and Communication Engineering, LBR College of Engineering, Mylavaram, Krishna District, Andhra Pradesh

M. Greeshma Vyas

Department of Electronics and Communication Engineering, LBR College of Engineering, Mylavaram, Krishna District, Andhra Pradesh

B. V. Anil Sai Kumar

School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, India

Suryavamsham Prem Kumar

School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, India

Konduru Jaswanth

School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, India

Kola Vishnu

School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, India

Abhishek Kumar

School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, India

Narendra Babu Alur

Department of Electronics and Communication Engineering, and Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

Kurapati Poorna Durga

Department of Electronics and Communication Engineering, and Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

Boddu Ganesh

Department of Electronics and Communication Engineering, and Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

Manda Devakaruna

Department of Electronics and Communication Engineering, and Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

Lakkimsetti Nandini

Department of Electronics and Communication Engineering, and Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

A. Praneetha

Department of Computer Science Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

T. Satyanarayana

Department of Electronics and Communication Engineering, and Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

K. Rani Rudrama

Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

Mounika Ramala

Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

Poorna sasank Galaparti

Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

Manikanta Chary Darla

Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna District, AP, India

Siva Sai Prasad Loya

Department of Electronics and Communication Engineering, Lakireddy
Bali Reddy College of Engineering (Autonomous), Mylavaram, Krishna
District, AP, India

K. Srinivasa Rao

Department of Electronics and Communication Engineering, KLEF,
Vaddeswaram, Green Fields, 522502, Andhra Pradesh, India

T. Anil Raju

Department of Electronics and Communication Engineering, Lakireddy
Bali Reddy College of Engineering, Mylavaram

K. Srihari Reddy

Department of Electronics and Communication Engineering, Lakireddy
Bali Reddy College of Engineering, Mylavaram

Sk. Arifulla Rabbani

Department of Electronics and Communication Engineering, Lakireddy
Bali Reddy College of Engineering, Mylavaram

G. Suresh

Department of Electronics and Communication Engineering, Lakireddy
Bali Reddy College of Engineering, Mylavaram

K. Saikumar Reddy

Department of Electronics and Communication Engineering, Lakireddy
Bali Reddy College of Engineering, Mylavaram

Rajesh C. Dharmik

Department of Information Technology, Yeshwantrao Chavan College of
Engineering, Nagpur

Bhushan U. Bawankar

Department of Information Technology, Yeshwantrao Chavan College of
Engineering, Nagpur

Preface

Machine Learning (ML) has touched all corners of human life and industry. Databased learning intelligence supports are the scalability of present technology and architecture. The current ML and deep learning (DL) algorithms require huge consumption of data and power. The industry is looking for an efficient VLSI circuit that can meet the demands of the AI-ML-DL universe. ML can pioneer different sectors throughout design methodologies from RTL design, synthesis, and verification. One of the deepest challenges of chip design is the time-consuming iterative process. Thanks to the learning model, time is considerably reduced. VLSI-based solutions and innovation of AI-ML-DL applications are growing in demand. Internet of Things–based solutions address the various challenges in society that require chips. This new book covers the latest AI/ML techniques, VLSI chip design, and systems to address societal challenges.

Applications of VLSI Design in Artificial Intelligence and Machine Learning

Imran Ullah Khan, Nupur Mittal* and Mohd. Amir Ansari

*Dept. of Electronics and Communication Engineering, Integral University,
Lucknow, India*

Abstract

In our advanced times, complementary metal-oxide semiconductor (CMOS) based organizations like semiconductor and gadgets face extreme scheduling of products and other different pressures. For resolving this issue, electronic design automation (EDA) must provide “design-based equivalent scaling” to continue the critical industry trajectory. For solving this problem machine learning techniques should be used both inside and “peripherally” in the design tools and flows. This article reviews machine learning opportunities, and physical implementation of IC will also be discussed. Cloud intelligence-enabled machine learning-based data analytics has surpassed the scalability of current computing technologies and architectures. The current methods based on deep learning are inefficient, require a lot of data and power consumption, and run on a data server with a long delay. With the advent of self-driving cars, unmanned aerial vehicles and robotics, there is a huge need to analyze only the necessary sensory data with low latency and low power consumption on edge devices. In this discussion, we will talk about effective AI calculations, for example, fast least squares, binary and tensor convolutional neural organization techniques, and compare prototype accelerators created in field preprogrammable gate array (FPGA) and CMOS-ASIC chips. Planning on future resistive random access memory (RRAM) gadgets will likewise be briefly depicted.

Keywords: VLSI, AI, ML, CAD & AVM

*Corresponding author: mittal@iul.ac.in