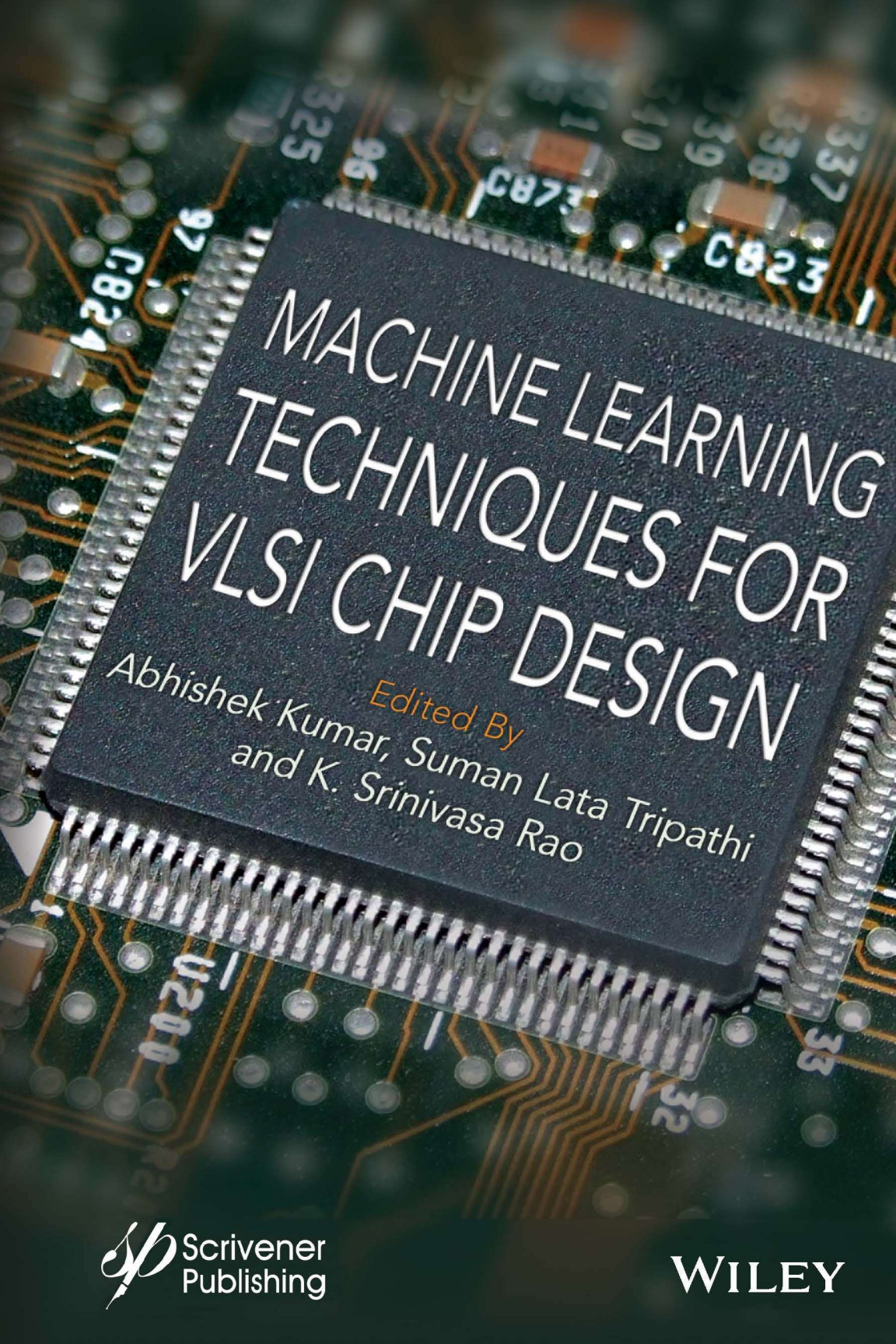
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Preface

Machine Learning (ML) has touched all corners of human life and industry. Databased learning intelligence supports are the scalability of present technology and architecture. The current ML and deep learning (DL) algorithms require huge consumption of data and power. The industry is looking for an efficient VLSI circuit that can meet the demands of the AI-ML-DL universe. ML can pioneer different sectors throughout design methodologies from RTL design, synthesis, and verification. One of the deepest challenges of chip design is the time-consuming iterative process. Thanks to the learning model, time is considerably reduced. VLSI-based solutions and innovation of AI-ML-DL applications are growing in demand. Internet of Things–based solutions address the various challenges in society that require chips. This new book covers the latest AI/ML techniques, VLSI chip design, and systems to address societal challenges.

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Applications of VLSI Design in Artificial Intelligence and Machine Learning

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Abstract

In our advanced times, complementary metal-oxide semiconductor (CMOS) based organizations like semiconductor and gadgets face extreme scheduling of products and other different pressures. For resolving this issue, electronic design automation (EDA) must provide "design-based equivalent scaling" to continue the critical industry trajectory. For solving this problem machine learning techniques should be used both inside and "peripherally" in the design tools and flows. This article reviews machine learning opportunities, and physical implementation of IC will also be discussed. Cloud intelligence-enabled machine learning-based data analytics has surpassed the scalability of current computing technologies and architectures. The current methods based on deep learning are inefficient, require a lot of data and power consumption, and run on a data server with a long delay. With the advent of self-driving cars, unmanned aerial vehicles and robotics, there is a huge need to analyze only the necessary sensory data with low latency and low power consumption on edge devices. In this discussion, we will talk about effective AI calculations, for example, fast least squares, binary and tensor convolutional neural organization techniques, and compare prototype accelerators created in field preogrammable gate array (FPGA) and CMOS-ASIC chips. Planning on future resistive random access memory (RRAM) gadgets will likewise be briefly depicted.

***Keywords*:** VLSI, AI, ML, CAD & AVM

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