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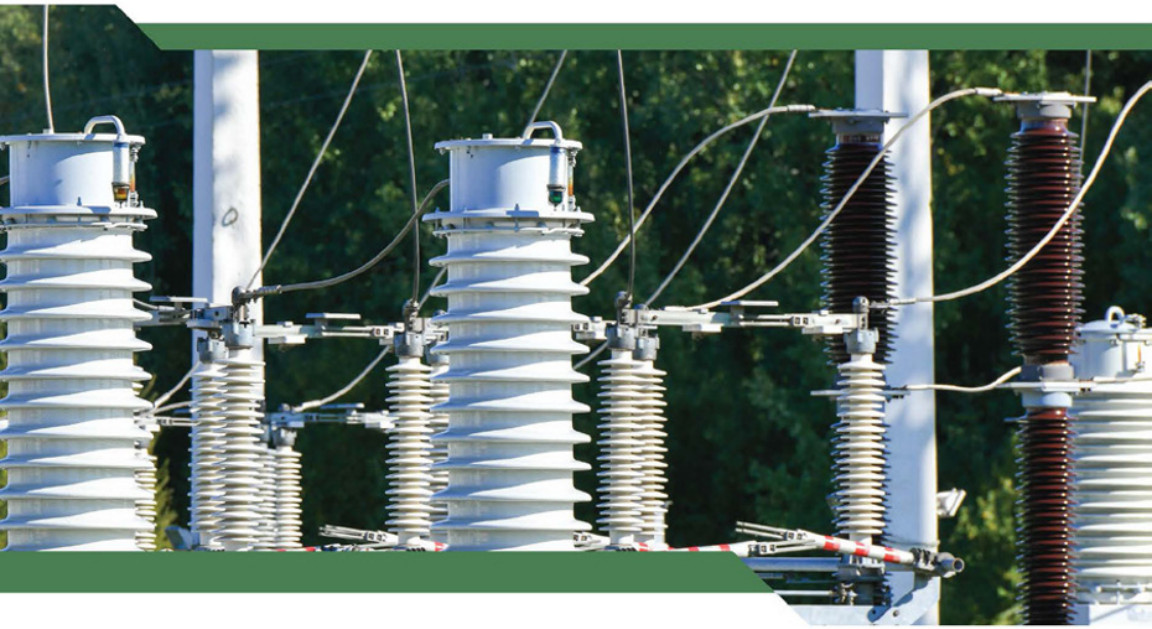
Modular Multilevel Converters

Control, Fault Detection, and Protection

Fujin Deng, Chengkai Liu, Zhe Chen



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Preface

With the rapid development of high-power semiconductor devices, power converters have been widely used in electric power conversion systems, converting electric power with high efficiency and economic benefit. The modular multilevel converter (MMC) is considered as one of the most promising converters for medium-/high-voltage and high-power applications because of its superior advantages, such as excellent output power quality, high efficiency, modularity, and scalability.

As increased MMCs are put into practical application, the concerns in terms of reliability and fault protection emerge to front stage. The semiconductors devices and capacitor are two most fragile components in the submodule of the MMC whose failure brings troubles to reliable operation of the MMC. And the MMC is usually required to have an uninterruptable operation ability in case of submodule malfunction. In addition, the AC-side grid fault and DC-side fault also pose challenges to the MMC system.

First, this book provides a brief review of the MMC basic principle and its control method in Chapters 1 and 2. Then, the insulated gate bipolar transistor fault detection methods and capacitor monitoring methods are respectively covered in Chapters 3 and 4. Chapter 5 offers fault-tolerant operation under submodule faults. Finally, Chapter 6 presents the control of MMCs under AC grid faults, and Chapter 7 explores the protection under DC short-circuit fault of the MMC system.

1

Modular Multilevel Converters

1.1 Introduction

Power converters have been widely used in electric power conversion systems that can convert electric power with high conversion efficiency and economic benefits. In the past few decades, several power converters have been developed and commercialized in the industrial community. They can be classified into current source converters (CSCs) and voltage source converters (VSCs).

The modular multilevel converter (MMC), as a kind of VSC, has been considered one of the most promising converters for medium/high-voltage and high-power applications, with the superiority such as excellent output power quality, high efficiency, modularity, and scalability [1–3]. Compared with traditional two-level and multilevel converters, the MMC has prominent advantages such as high efficiency and low power losses. What is more, high modularity enables the MMC to easily expand capacity. Recently, the MMC has become attractive for high-voltage direct-current (HVDC) transmission [4], renewable energy generation [5], electric railway supplies [6], micro power grid [7], etc.

This chapter deals with the fundamental principles of the MMC. The configuration of the MMC is presented in Section 1.2. Section 1.2 gives an introduction of the converter configuration and the submodule (SM) configuration. The operation principles of the SM and the converter are shown in Section 1.3. Section 1.4 demonstrates the modulation schemes, including phase-disposition (PD) pulse width modulation (PWM), phase-shifted (PS) PWM, and nearest level modulation (NLM). Afterward, mathematical models of the SM, the arm, and the MMC are introduced in Section 1.5. Then, Section 1.6 introduces the parameter design methods of power devices, capacitor, and arm inductor in the MMC. An overview of the MMC faults is given in Section 1.7.

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1.2 MMC Configuration

1.2.1 Converter Configuration

A three-phase MMC topology is shown in Figure 1.1, which consists of three phase-legs, each composed of an upper arm and a lower arm. Each arm contains n identical SMs and an arm inductor L_s. The upper and lower arm currents are i_{ju} and i_{jl}, respectively, in phase j ($j = a, b, c$). The AC side of the MMC is equipped with the filter inductor L_f. The MMC links the DC side and the three-phase AC side. Electric power can flow from the DC side to the AC side or from the AC side to the DC side through changing the operation mode of the MMC. The number of SMs can affect the output voltage level and thus power quality. A multilevel voltage would be synthesized at the AC side of the MMC, and output harmonic contents would be reduced with the cascading of SMs [8].

1.2.2 Submodule Configuration

The SM unit is the fundamental component of the MMC. Figure 1.2 shows the typical half-bridge (HB) SM configuration, which is widely used in power

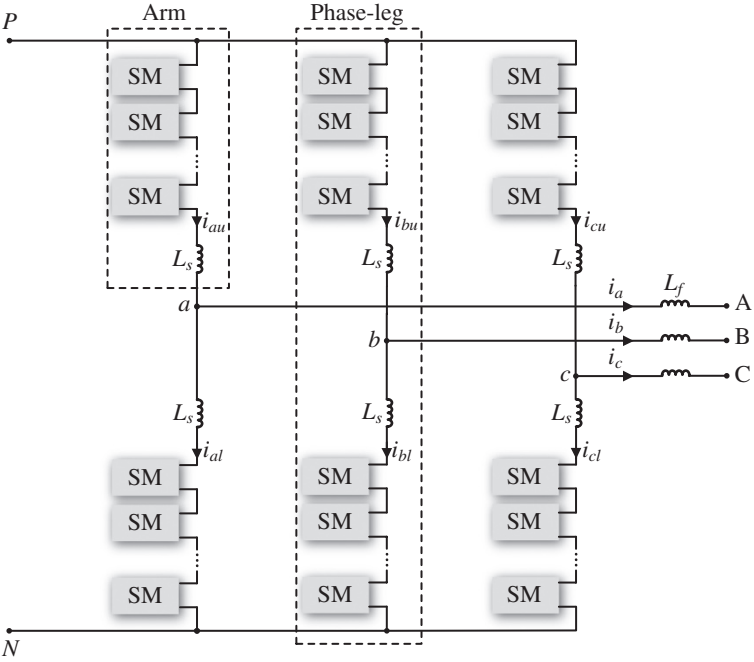
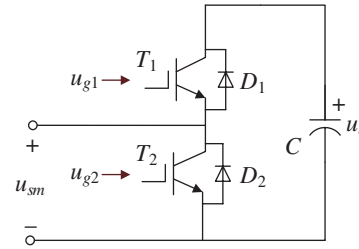


Figure 1.1 Three-phase MMC configuration.

Figure 1.2 Half-bridge SM.



applications. The HB SM consists of two switches/diodes T_1/D_1 and T_2/D_2 and a DC capacitor C. Through the switching of the power switches T_1 and T_2, the HB SM can output two voltage levels, including the capacitor voltage u_c and 0 [8].

1.3 Operation Principles

1.3.1 Submodule Normal Operation

In the normal operation of the MMC, the operation state of the SM is controlled by the switching function S, which is defined as

$$S = \begin{cases} 1, & u_{g1} \text{ is high-level and } u_{g2} \text{ is low-level} \\ 0, & u_{g1} \text{ is low-level and } u_{g2} \text{ is high-level} \end{cases} \tag{1.1}$$

where u_{g1} and u_{g2} are the drive voltages of switches T_1 and T_2, respectively, as shown in Figure 1.2. The switching modes of the HB SM are listed in Table 1.1.

- The T is turned on when the u_g is high-level
- The T is turned off when the u_g is low-level.

The relationship between the SM's output voltage u_{sm} and the SM's capacitor voltage u_c is

$$u_{sm} = S \cdot u_c \tag{1.2}$$

The normal operation of the HB SM has four operation modes, as shown in Table 1.2 and Figure 1.3, which are decided by the switching function S and the direction of the arm current i_{arm}, as follows:

Table 1.1 Switching modes of the HB SM.

S	u_{g1}	u_{g2}	T_1	T_2
1	High-level	Low-level	On	Off
0	Low-level	High-level	Off	On

Table 1.2 Four normal operation modes of the HB SM.

Mode	S	i_{arm}	Circuit state	SM state	T_1	T_2	u_{sm}	C	u_c
1	1	>0	Inserted	On	On	Off	u_c	Charged	Increased
2		<0	Inserted	On	On	Off	u_c	Discharged	Reduced
3	0	>0	Bypassed	Off	Off	On	0	Bypassed	Unchanged
4		<0	Bypassed	Off	Off	On	0	Bypassed	Unchanged

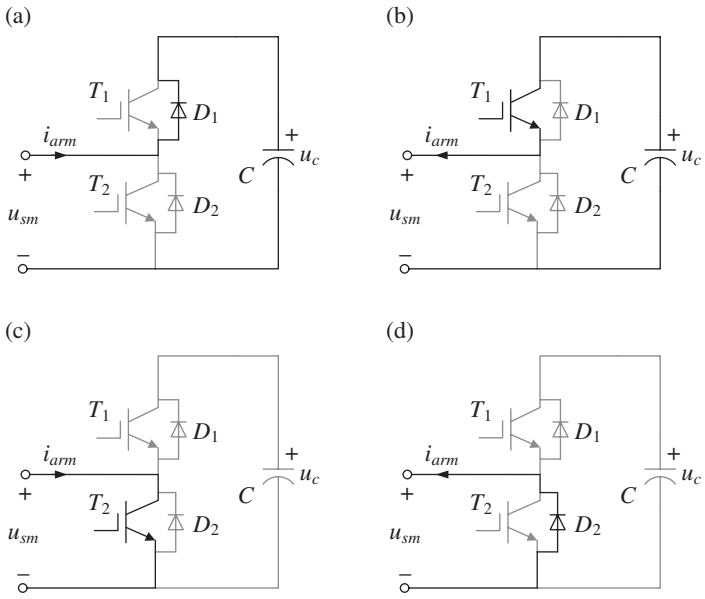


Figure 1.3 Four normal operation modes of the HB SM. (a) Mode 1 (normal operation). (b) Mode 2 (normal operation). (c) Mode 3 (normal operation). (d) Mode 4 (normal operation).

- *Mode 1 (normal operation)*: When $S = 1$ and $i_{arm} > 0$, as shown in Figure 1.3a, the T_1 is turned on, the T_2 is turned off, the SM is inserted into the arm circuit, the SM state is on, and the SM output voltage u_{sm} is equal to the SM capacitor voltage u_c. In this case, the SM capacitor C is charged by i_{arm}, and the capacitor voltage u_c is increased.
- *Mode 2 (normal operation)*: When $S = 1$ and $i_{arm} < 0$, as shown in Figure 1.3b, the T_1 is turned on, the T_2 is turned off, the SM is inserted into the arm circuit, the SM state is on, and the SM output voltage u_{sm} is equal to the SM capacitor

voltage u_c. In this case, the SM capacitor C is discharged by i_{arm}, and the capacitor voltage u_c is reduced.

- *Mode 3 (normal operation)*: When $S = 0$ and $i_{arm} > 0$, as shown in Figure 1.3c, the T_1 is turned off, the T_2 is turned on, the SM is bypassed from the arm circuit, the SM state is off, and the SM output voltage u_{sm} is equal to 0. In this case, the SM capacitor C is bypassed, and the capacitor voltage u_c is unchanged.
- *Mode 4 (normal operation)*: When $S = 0$ and $i_{arm} < 0$, as shown in Figure 1.3d, the T_1 is turned off, the T_2 is turned on, the SM is bypassed from the arm circuit, the SM state is off, and the SM output voltage u_{sm} is equal to 0. In this case, the SM capacitor C is bypassed, and the capacitor voltage u_c is unchanged.

1.3.2 Submodule Blocking Operation

In the blocking operation of the HB SM, the drive voltages u_{g1} and u_{g2} are both low-level and the switches T_1 and T_2 are both turned off, which has two operation modes and is decided by the arm current i_{arm}, as shown in Table 1.3 and Figure 1.4, as follows:

- *Mode 1 (blocking operation)*: When T_1 and T_2 are both turned off and $i_{arm} > 0$, as shown in Figure 1.4a, the SM is inserted into the arm circuit, the SM state is on, and the SM's output voltage u_{sm} is u_c. In this case, the capacitor C is charged by i_{arm}, and the capacitor voltage u_c is increased.

Table 1.3 Two blocking operation modes of the HB SM.

Mode	i_{arm}	Circuit state	SM state	T_1	T_2	u_{sm}	C	u_c
1	>0	Inserted	On	Off	Off	u_c	Charged	Increased
2	<0	Bypassed	Off	Off	Off	0	Bypassed	Unchanged

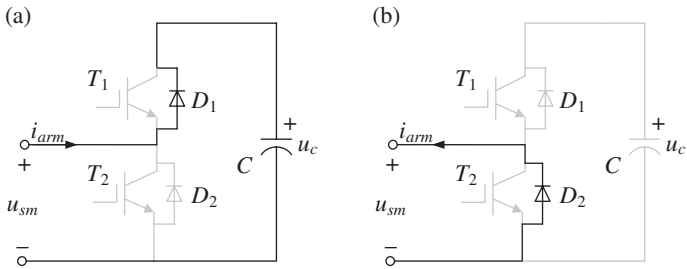


Figure 1.4 Two blocking operation modes of the HB SM. (a) Mode 1 (blocking operation). (b) Mode 2 (blocking operation).

- *Mode 2 (blocking operation)*: When T_1 and T_2 are both turned off and $i_{arm} < 0$, as shown in Figure 1.4b, the SM is bypassed from the arm circuit, the SM state is off, and the SM's output voltage u_{sm} is 0. In this case, the capacitor C is bypassed, and the capacitor voltage u_c is unchanged.

1.3.3 Converter Operation

The MMC generates the multilevel stepped waveform at its AC side by controlling the number of inserted SMs in the arm. To get an intuitive understanding of the operation principle of the MMC, Figure 1.5a shows an example of the upper arm of phase A, where four HB SMs (SM1–SM4) per arm are considered for the MMC. Here, all SMs' capacitor voltages are supposed to be the same as u_c, and the output voltages of the SM1–SM4 are u_{sm_au1}, u_{sm_au2}, u_{sm_au3}, and u_{sm_au4}, respectively. The waveform of the upper arm voltage u_{au} in phase A in one fundamental period is shown in Figure 1.5b, which is the sum of all SMs' output voltages u_{sm_au1}, u_{sm_au2}, u_{sm_au3}, and u_{sm_au4} in the upper arm of phase A. The switching functions of the SM1–SM4 and the corresponding output voltages of the SM1–SM4 are shown in Table 1.4, where the switching functions of

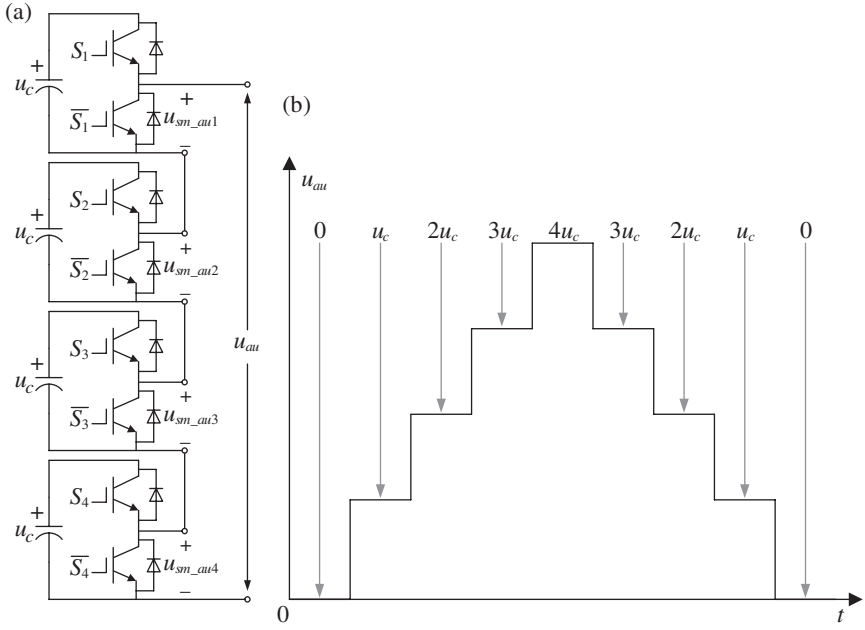


Figure 1.5 Operation principle of the MMC. (a) Upper arm of phase A. (b) Upper arm voltage of phase A.

Table 1.4 Switching functions and output voltages of SMs.

n_{on}	S_{au1}	S_{au2}	S_{au3}	S_{au4}	u_{sm_au1}	u_{sm_au2}	u_{sm_au3}	u_{sm_au4}	u_{au}
0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	u_c	0	0	0	u_c
	0	1	0	0	0	u_c	0	0	
	0	0	1	0	0	0	u_c	0	
	0	0	0	1	0	0	0	u_c	
2	1	1	0	0	u_c	u_c	0	0	$2u_c$
	1	0	1	0	u_c	0	u_c	0	
	1	0	0	1	u_c	0	0	u_c	
	0	1	1	0	0	u_c	u_c	0	
	0	1	0	1	0	u_c	0	u_c	
	0	0	1	1	0	0	u_c	u_c	
3	1	1	1	0	u_c	u_c	u_c	0	$3u_c$
	1	1	0	1	u_c	u_c	0	u_c	
	1	0	1	1	u_c	0	u_c	u_c	
	0	1	1	1	0	u_c	u_c	u_c	
4	1	1	1	1	u_c	u_c	u_c	u_c	$4u_c$

SM1–SM4 are S_{au1}, S_{au2}, S_{au3}, and S_{au4}, respectively. The arm voltage u_{au} has five different levels including 0, u_c, $2u_c$, $3u_c$, and $4u_c$, which is expressed as

$$u_{au} = \sum_{i=1}^{4} u_{sm\_aui} = \sum_{i=1}^{4} \left(S_{aui} \cdot u_c \right) = n_{on} \cdot u_c \tag{1.3}$$

with

$$n_{on} = \sum_{i=1}^{4} S_{aui} \tag{1.4}$$

where n_{on} is the number of inserted SMs in the arm of the MMC. The arm voltage u_{au} depends on different switching combinations corresponding to the SMs in the arm, as shown in Figure 1.5 and Table 1.4.

- *Fifth level ($u_{au} = 4u_c$)*: The highest arm voltage $4u_c$ is generated when all four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 are all switched to 1.

- *Forth level ($u_{au} = 3u_c$)*: The arm voltage $3u_c$ is generated when three out of four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 are switched to 1.
- *Third level ($u_{au} = 2u_c$)*: The arm voltage $2u_c$ is generated when two out of four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 are switched to 1.
- *Second level ($u_{au} = u_c$)*: The arm voltage u_c is generated when one out of four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 is switched to 1.
- *First level ($u_{au} = 0$)*: The lowest arm voltage 0 is generated when all four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 are all switched to 0.

1.4 Modulation Scheme

Modulation is a technique that produces the desired voltage in the arm or at the AC side of the MMC by controlling the drive voltage of switching devices in the MMC. It affects not only the MMC's external performance, such as AC-side voltage harmonics and AC-side current harmonics, but also the internal characteristics, such as capacitor voltage fluctuation, distribution of energy, and power losses distribution among SMs [9]. Currently, there are three modulation schemes commonly used in the MMC, which are PD-PWM, PS-PWM, and NLM, as shown in Table 1.5. Based on the modulation and the reference y for the arm of the MMC, the number n_{on} of SMs to be inserted into the arm of the MMC can be decided, as shown in Figure 1.6.

Table 1.5 Three modulation schemes [9–16].

Modulation scheme	Characteristics
PD-PWM	• High switching frequency modulation • Unevenly distributed pulses • Suitable for MMCs with not so many SMs per arm
PS-PWM	• High switching frequency modulation • Evenly distributed pulses • Suitable for MMCs with not so many SMs per arm
NLM	• Low switching frequency modulation • Easy for implementation • Suitable for MMCs with large number of SMs per arm

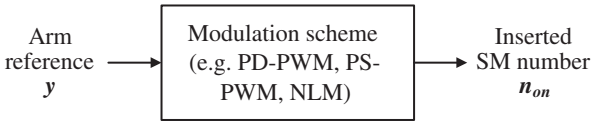


Figure 1.6 Modulation for MMCs.

1.4.1 Phase-Disposition PWM

The PD-PWM is typically suitable for the MMC with not so many SMs per arm [9–11]. For the MMC with n SM per arm, it is realized by applying n number of identical triangular carriers W_1–W_n stacked evenly in the vertical direction between −1 and 1. Through the comparison between the carriers and the reference signal y, the PD-PWM can be produced.

Figure 1.7 illustrates the implementation principle of the PD-PWM ($n = 4$) for the MMC with n SMs per arm. The n carriers W_1–W_n are at the same phase angle. The carrier frequency is f_s. The height Δh of each carrier is equal to $2/n$.

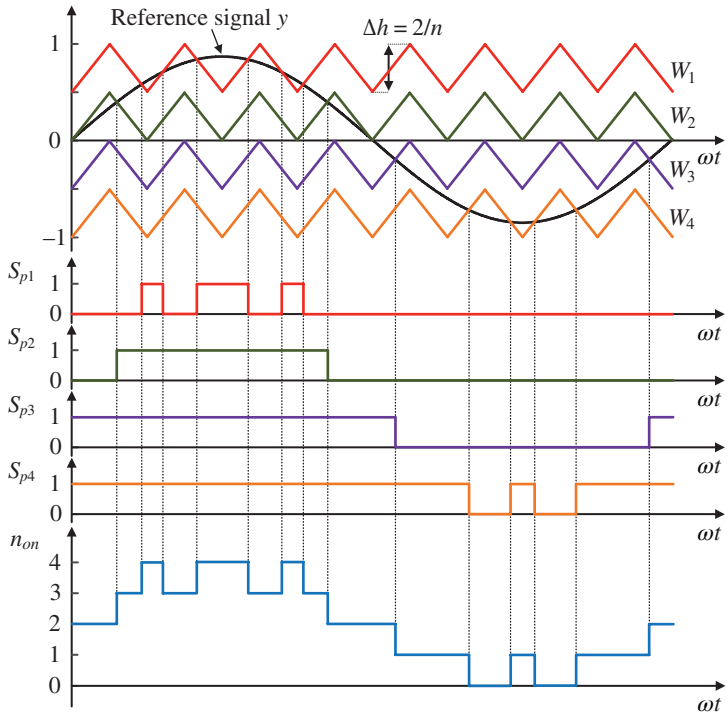


Figure 1.7 Implementation principle of PD-PWM for MMCs.

The reference signal y is compared with the carriers W_1–W_n to generate the pulses S_{p1}–S_{pn}, respectively, as follows:

- The S_{pi} is 1 if the reference y is higher than the carrier W_i ($i = 1, 2, \ldots, n$)
- The S_{pi} is 0 if the reference is lower than the carrier W_i ($i = 1, 2, \ldots, n$)

The total number n_{on} of SMs to be inserted into each arm at each instant can be expressed as the sum of S_{p1}–S_{pn}, as

$$n_{on} = \sum_{i=1}^{n} S_{pi} \tag{1.5}$$

Figure 1.7 shows that the PD-PWM results in an unevenly distributed switching frequency among S_{p1}–S_{pn}. The value of n_{on} varies in the range of 0–n in one fundamental period, which achieves the multilevel synthesized waveform. In addition, it is apparent that the switching actions of S_{p1}–S_{pn} are affected by the amplitude of the reference signal y.

The typical characteristics of the PD-PWM are summarized in Table 1.5.

1.4.2 Phase-Shifted PWM

The PS-PWM is suitable for the MMC with not so many SMs per arm [12, 13]. For the MMC with n SMs per arm, it is realized by applying n number of identical triangular carriers W_1–W_n stacked evenly in horizontal direction. The carrier is between −1 and 1. Through the comparison between the carriers W_1–W_n and the reference signal y, the PS-PWM can be achieved.

Figure 1.8 illustrates the implementation principle of PS-PWM ($n = 4$) for the MMC with n SMs per arm. The carriers W_1–W_n are all with the same carrier frequency f_s. The phase angle between two adjacent carriers of W_1–W_n is denoted as $\Delta\theta$. Generally, the $\Delta\theta$ is

$$\Delta\theta = 2\pi / n \tag{1.6}$$

The reference signal y is compared with the carriers W_1–W_n to generate the pulses S_{p1}–S_{pn}, as follows:

- The S_{pi} is 1 if the reference y is more than the carrier W_i ($i = 1, 2, \ldots, n$)
- The S_{pi} is 0 if the reference is less than the carrier W_i ($i = 1, 2, \ldots, n$)

The total number n_{on} of the SMs to be inserted into each arm at each instant can be expressed as the sum of S_{p1}–S_{pn}, as

$$n_{on} = \sum_{i=1}^{n} S_{pi} \tag{1.7}$$

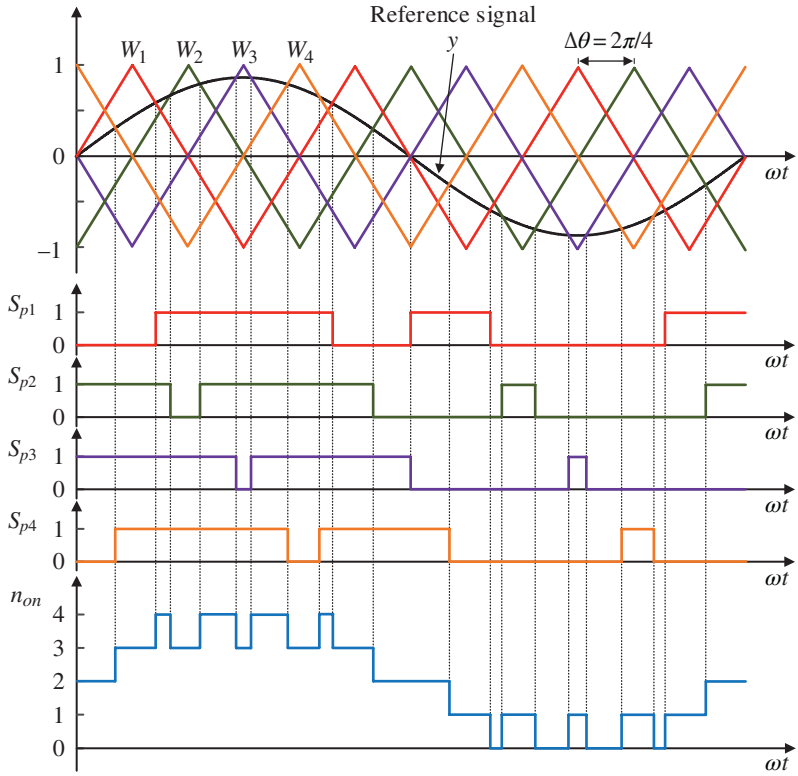


Figure 1.8 Implementation principle of PS-PWM for MMCs.

In Figure 1.8, the reference signal y is always modulated by all carriers W_1–W_n to generate the PWM pulses. The pulses and the switching frequency are distributed evenly among S_{p1}–S_{pn}. The value of n_{on} varies in the range of 0–n in one fundamental period, which achieves the multilevel synthesized waveform. In addition, the switching actions of S_{p1}–S_{pn} remain constant regardless of the modulation index of the reference signal.

The typical characteristics of the PS-PWM are summarized in Table 1.5.

1.4.3 Nearest Level Modulation

The NLM is suitable for the MMC applications with large number of SMs, e.g. high voltage direct current (HVDC) transmission [9, 14–16]. The NLM uses the staircase waveform nearest to the desired reference signal. For the MMC with n SMs per arm, the NLM can be produced with the simple rounding function for the reference y.

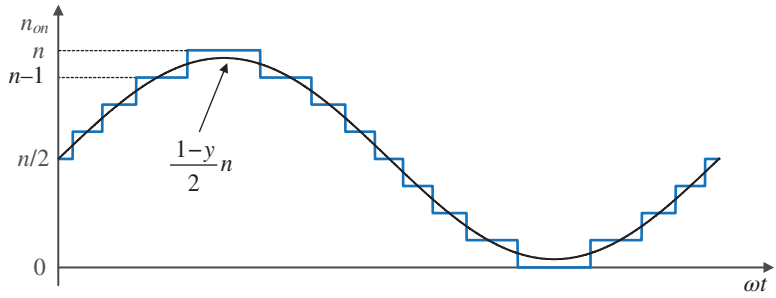


Figure 1.9 Implementation principle of NLM for MMCs.

Figure 1.9 illustrates the implementation principle of the NLM for the upper arm of the MMC ($n = 8$) with n SMs per arm. Based on the reference signal y for the phase unit, the total number n_{on} of SMs to be inserted into the upper arm at each instant can be obtained as

$$n_{on} = \text{round}\left(\frac{1-y}{2}n\right) \tag{1.8}$$

The NLM directly generates the number of inserted SMs in the arm to yield the multilevel waveforms. The waveform of n_{on} is a staircase with step height of 1. The value of n_{on} varies in the range of 0–n. Therefore, the maximum level number of n_{on} is $n+1$. The harmonic spectrum of the NLM is dependent on n. If n is small, the staircase number is small and the harmonics will be a little high. If n is large, the staircase number is large and the multilevel waveforms will be very close to the reference signal and have very little harmonics.

The typical characteristics of the NLM are summarized in Table 1.5.

1.5 Mathematical Model

1.5.1 Submodule Mathematical Model

Figure 1.10 shows the equivalent circuit diagram of the i-th SM in the upper arm of phase A. Figure 1.10a shows the equivalent circuit diagram of the SM when its switching function S_{aui} is 1, and Figure 1.10b shows the equivalent circuit diagram of the SM when its switching function S_{aui} is 0. According to the equivalent circuit diagrams, the switching-function based model and the reference-based model of the HB SM can be derived as discussed in the following sections.