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Preface

In the present day, the integrated circuit (IC) industry has, now more than ever, a massive demand for electronic devices not only for the consumer electronics markets but also in other industries such as medical, automotive, or security. Despite Moore's Law not really being observed anymore, the evolution of the IC industry is still clearly observable every year, with designers building increasingly more complex, power-efficient, and integrated systems. These systems often combine analog and digital sections, where most components are integrated into a single chip originating mixed-signal systems-on-a-chip. While these ICs are implemented mainly using digital circuitry, analog operations are still fundamental and irreplaceable. Additionally, technologies such as the Internet of things or fifth-generation broadband join millions of devices and sensors. All these applications continuously gather an increasing amount of data, posing unprecedented challenges to each element of the networks. Due to this, today's market is highly conditioned by the strong demand for high communication rates, large bandwidths, and ultra-low power consumptions, in which radio-frequency (RF) ICs play a critical role. However, analog design is unlike digital design, where an automated flow is established for most design stages. The absence of effective and established computer-aided design tools for electronic design automation of analog and radio-frequency IC blocks poses a significant contribution to their bulky development cycles, leading to long, iterative, and error-prone designer intervention over their entire design flow.

In the past years, automatic simulation-based sizing approaches became essential in designing analog and radio-frequency IC blocks for modern applications to ensure their robustness. However, optimizations considering process, voltage, and temperature (PVT) corners or layout still pose unprecedented challenges in applying these tools due to the high simulation times and different simulator convergence issues. Therefore, the work presented in this book addresses the automatic sizing of analog ICs assisted by deep learning and artificial neural networks on two fronts. First, it proposes two deep learning models to assist the PVT-inclusive simulation-based sizing process of radio-frequency ICs, specifically, voltage-controlled oscillators (VCOs). Given specific devices' dimensions, the first model classifies the likelihood of the circuit to convergence for nominal and PVT corner cases, bypassing solutions that will hardly produce valuable information for the optimization process. The model also predicts the VCOs' oscillating frequencies for the mentioned conditions. The methodology is tested on a state-of-the-art VCO, reducing 19% of the workload of the circuit simulator, ultimately saving almost 5 days of computational effort and improving the optimization result. Secondly, a PVT regressor is proposed, which inputs the circuit's sizing and the nominal performances to estimate the PVT corner performances via multiple parallel artificial neural networks. Two control phases prevent the optimization process from being misled by inaccurate performance estimates. The proposed controlled PVT estimator is tested on two state-of-the-art VCOs, reducing the workload of the circuit simulator up to 79% while achieving a speed-up factor of 2.92 ×, ultimately saving more than 16 days of computational effort. Both methodologies can be used simultaneously, and ultimately, they offer a unique opportunity to reuse valuable legacy data, often discarded in optimization environments.

Finally, the authors would like to express gratitude for the financial support that made this work possible. The work developed in this book was supported by FCT/MCTES through national funds and when applicable co-funded EU funds under the project UIDB/50008/2020 (including internal research project LAY(RF)^2/X-0002-LX-20) and Research Grant FCT-SFRH/BD/07123/2021.

This book is organized into four chapters.

Chapter 1 presents an introduction to the analog IC design area and discusses how the advances in machine learning can pave the way for new EDA tools.

Chapter 2 presents a study of the available tools for analog design automation. Starting with an overview of existing works where machine learning techniques are applied to analog IC sizing.

Chapter 3 presents two artificial neural network models for analog IC design to be incorporated within simulation-based sizing loops. The first model classifies the convergence of the circuit for nominal and PVT corners, bypassing solutions that will hardly produce valuable information for the evolutionary kernel, and the second predicts the pre-defined simulator values for the previous conditions.

Chapter 4 presents a controlled PVT regressor based on an artificial neural network, also intended to be incorporated within simulation-based synthesis. This regressor estimates the complete set of PVT corner performances via multiple parallel networks.

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Contents

Chapter 1
Introduction

1.1 Analog/RF Integrated Circuit Design Automation

In the present day, the IC industry has, now more than ever, a huge demand for electronic devices not only in the consumer electronics markets but also in other industries such as medical, automotive, or security. Despite Moore's law not really being observed anymore, the evolution of the IC industry is still clearly observable every year, with designers building increasingly more complex, power-efficient and integrated systems. These systems often combine analog and digital sections, where most components are integrated into a single chip originating mixed-signal systems-on-a-chip (SoCs). While most functionalities are implemented using digital or digital signal processing circuitry, analog circuits are the bridge between digital circuitry and physical devices with a steady increase in connectivity needs. Even though analog circuits only occupy a small fraction of the SoCs, their design effort is disproportionally large, as illustrated by Fig. 1.1 [1]. According to [2], the global IC market was worth $412.3 billion in 2019 and is expected to grow to $502.94 billion by 2023, with analog components being present in more than 50% of the total IC shipments yearly. Besides, the strict time-to-market constraints and development costs make electronic systems' design challenging, being, therefore, fundamental to accelerate their development process as much as possible.

Plenty of EDA tools and design methodologies have been made available to cope with new capabilities offered by the integration technologies. However, there is still a considerable discrepancy between the analog and digital IC design tools. The gap between the number of existing EDA tools for digital and analog circuits is usually explained by the fact that the digital market is much larger, absorbing the available resources. It is also easier to express a digital system, which can be represented naturally in terms of Boolean expressions, whereas, on the analog side, their design is less systematic, more knowledge-based, and more heuristic [3]. Even though analog circuits only occupy a small fraction of these SoCs, they are responsible for most design errors and expensive redesigns/reruns. Therefore, economic pressure

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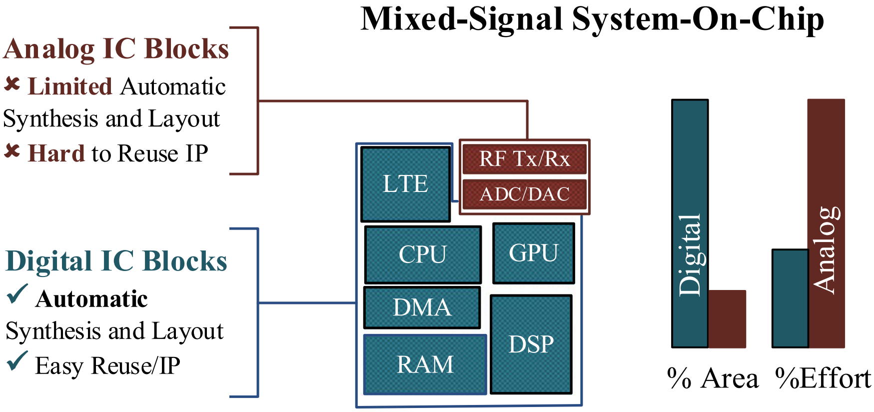

Fig. 1.1 Contrast between analog and digital blocks' design effort [1]

has motivated the quest for better methodologies to accelerate analog design. The automation level for analog IC has improved in the last few years, a field of profound academic and industrial research activity producing significant advances. However, it is still far from the push-button stage, leading designers to keep exploring the solution space almost manually, as there are no standard plug-and-play EDA tools and methodologies to automate the analog IC design flow.

While most of this is true for analog base-band, on top of that, with predictions that more than half of new businesses will run on the internet-of-things (IoT) and advanced telecommunication broadbands, such as the 5th generation (5G), there will be an immense demand for devices and sensors, opening doors to advances in many areas. This has already led to an increase in the amount of data that is being continuously generated, resulting in new challenges within every part of the network. Consequently, there is high pressure in today's market for larger communication rates, extensive bandwidths, and ultralow-power consumptions. This is where RF ICs come in hand, playing a crucial role. However, RF IC design in deep nanometric integration technologies for both IoT and 5G is extraordinarily difficult, due to their high complexity and demanding performances. Some of the design difficulties lie in the wide range of frequencies and dynamic ranges involved, but also on:

- Their dependence on non-reliable models of passive devices;
- At gigahertz frequencies, there is a huge impact of layout parasitics;
- Their integration in deep nanometer technologies causes variability issues and non-idealities which have never been experienced in older technology nodes.

Avoiding costly redesign cycles and reducing post-fabrication tuning and compensation work on first-pass fabrication success became primary RF IC design objectives. Established computer-aided design (CAD) companies provide environments that allow circuit designers to carry this flow manually. Despite this, the classical trial