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Multi-Gigahertz Nyquist Analog-to-Digital Converters

Architecture and Circuit Innovations in Deep-Scaled CMOS and FinFET Technologies

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To Theodhor and Linda

Preface

The analog-to-digital converter (ADC) is considered the cornerstone of modern electronics due to its fundamental role in virtually any application requiring the transfer of information between the physical (analog) world and the processing (digital) world. This task comes with myriad challenges due to the complex multi-functional ADC nature, further exacerbated when the relevant applications demand stringent performance requirements. Furthermore, bridging the analog and digital worlds fundamentally implies that ADCs must deal with the non-idealities of the former while keeping up with the advancements of the latter.

The rapidly accelerating trend for broader-band signals and software-defined systems has spurred the need for ADCs operating in the multi-GHz sample rate and bandwidth regime. Such converters are highly demanded by applications in the realm of next generation high-speed wireless and wireline communications, automotive radar, and high-end instrumentation, and have attracted a growing attention from both industry and academia. The ever-increasing desire of these systems is to maximize speed, while progressively improving the accuracy and the power efficiency, pushing the performance dimensions to new benchmarks. Meeting these requirements at the multi-GHz regime comes with numerous challenges at the circuit, architecture, and system levels. On top, the constant technology downscaling, dictated by the demand for higher functionality at a reduced power and cost, and the improvement in digital performance, exacerbates these challenges for traditional analog-intensive solutions.

This book follows a holistic approach, from analysis to implementation, to propose innovative circuit, architecture, and system solutions in deep-scaled CMOS and maximize the $accuracy \cdot speed \div power$ of multi-GHz sample rate and bandwidth ADCs. The approach starts by identifying the major error sources of any practical converter's circuits and quantitatively analyzing their significance on the overall performance, establishing the fundamental accuracy-speed-power limits imposed by circuits, and building an understanding as to what may be achievable from a converter's elementary building blocks. The analysis extends to the architecture level, by introducing a mathematical framework to estimate and compare the accuracy-speed-power limits of high-performance architectures, such as flash, SAR, pipeline,

and pipelined-SAR. To gain insight on the system level and peripheral blocks, a framework is introduced to quantitatively compare interleaver architectures, in terms of achievable bandwidth and sampling accuracy. The strength of the newly introduced frameworks is further enhanced by adding technology effects from four deep-scaled CMOS processes: 65 nm, 40 nm, 28 nm, and 16 nm, building insight into both architecture as well as process choices for optimum performance at given specifications.

The validity of the above holistic approach and the feasibility of the proposed solutions are demonstrated by four prototype ICs, realized in 28 nm bulk CMOS and 16 nm FinFET CMOS:

1. An ultrahigh-speed three-stage triple-latch feed-forward dynamic comparator improves the gain and reduces the delay of dynamic comparators across the entire input range. [28 nm CMOS, presented at *ESSCIRC 2019*, and published in *SSC-L 2019* and *TCAS-I 2022*]
2. A high-speed wide-bandwidth medium resolution single-channel SAR ADC maximizes the $accuracy \cdot speed \div power$ ratio with a semi-asynchronous timing, an improved bootstrapped input switch, a triple-tail dynamic comparator, and a Unit-Switch-Plus-Cap DAC. [28 nm CMOS, presented at *ESSCIRC 2017*, and published in *JSSC 2018*]
3. A high-resolution wide-bandwidth 8×-interleaved hybrid RF ADC with a bufferless input front end, a 3-stage pipelined-SAR sub-ADC, a low excess jitter clock chain, and co-designed analog–digital calibrations significantly improves the state of the art in RF ADCs. [28 nm CMOS, presented at *ISSCC 2019*, and published in *JSSC 2020*]
4. An ultra-wideband highly linear analog front end with a multi-segment distributed attenuation filter and a hybrid amplifier-buffer extends the bandwidth of next-generation direct RF ADC-based receivers to several tens of GHz, enabling direct RF sampling up to mm-wave frequencies. [16 nm FinFET CMOS, presented at *VLSI 2022*, and two US patents]

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Chapter 1
Introduction

Real-world phenomena comprise to their vast majority analog quantities; that is continuous-time and continuous-amplitude signals able to take any value at any particular instant. However, manipulation and storage of data are mainly performed in the digital domain due to several benefits of digital signal processing, such as reduced sensitivity to noise and distortion, increased flexibility and reconfigurability, and continuous performance improvement with technology scaling. As a result, Analog-to-Digital (A/D) conversion performed by an Analog-to-Digital Converter (ADC) and Digital-to-Analog (D/A) conversion performed by a Digital-to-Analog Converter (DAC) are indispensable operations in almost all electronic systems.

This introductory chapter starts by briefly outlining the need and applicability of data converters in a digital era, in Sect. 1.1. Key high-performance ADC applications are briefly discussed. Section 1.2 introduces challenges in simultaneously improving the three main ADC performance parameters. These come on a circuit level, an architectural level, a system level, and a technology level, with the last one being particularly important as it affects the other three. The main scope of the research described in this book and its objectives are listed and briefly discussed in Sect. 1.3. Finally, Sect. 1.4 concludes this chapter with the structural organization of this book.

1.1 Data Converters in a Digital Era: Need and High-Performance Applications

Electronic devices undeniably play a crucial role in tremendously improving every aspect of our modern life: from massive communication and transportation infrastructure to personalized entertainment systems and healthcare. To a great extent, this level of accessibility to electronic devices and services owes to the expansion of Digital Signal Processing (DSP), leading to a progressively digital electronic world. The fundamental reason for the DSP advances finds its root

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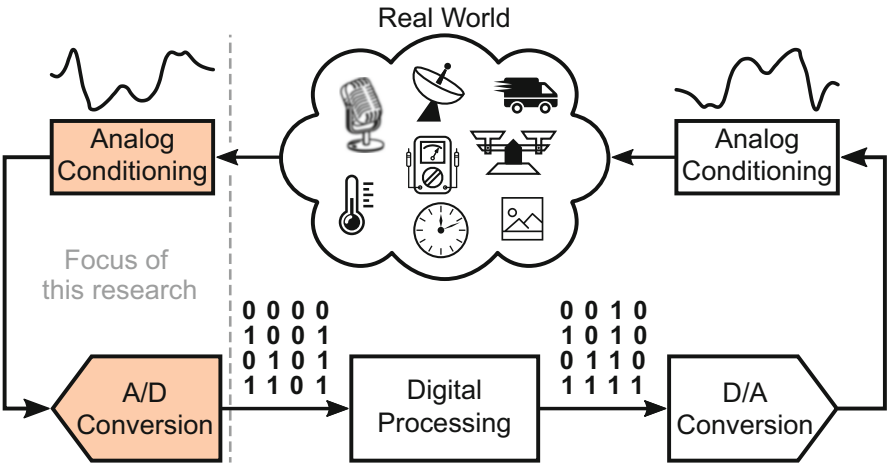

Fig. 1.1 Illustration of the data conversion as an indispensable bridging function between the real analog world and the digital signal processing world

in the down-scaling and integration advantages of Very Large Scale Integration (VLSI) technologies, offering a higher functionality per unit area for a reduced power and cost. Following Gordon E. Moore's law proposed in 1965 [1], the number of devices per chip doubles every roughly 2 years, with an even higher rate recently [2]. Further, digital circuits offer several advantages with respect to their analog equivalents, such as reduced susceptibility to distortion and noise, less dependency on process-voltage-temperature variations, increased flexibility and reconfigurability, and an unprecedented ability to perform complex computations on-demand, making Systems-on-a-Chip (SoC)s the norm.

Yet, real-world phenomena comprise analog quantities, such as velocity, volume, weight, temperature, voltage, current, etc. Therefore, A/D conversion is a vital function in most electronic devices, to provide the translation interface between the physical and electronic worlds, as illustrated in Fig. 1.1. Similarly, D/A conversion enables the interaction of the device with the environment and the humans, who perceive and process data in the form of analog quantities. Even without the human in the loop, the information exchange between two devices still requires conversion of the data from the digital domain to the analog domain and back. At the transmit side, the digital data is converted into the analog domain to travel through a certain medium. Equivalently, at the receive side, the signal comes either in an analog form or in a degraded by the medium digital form; therefore, it is processed as analog information before it is converted into the digital domain. This role of data converters as interfaces between the analog and digital domains puts them in a unique position in the signal processing chain but also poses considerable design challenges since they must deliver an equivalent or better performance than the corresponding digital systems. For the ADC in particular, which is the focus of this work, to maximally leverage the favorable properties of DSP, its function should be

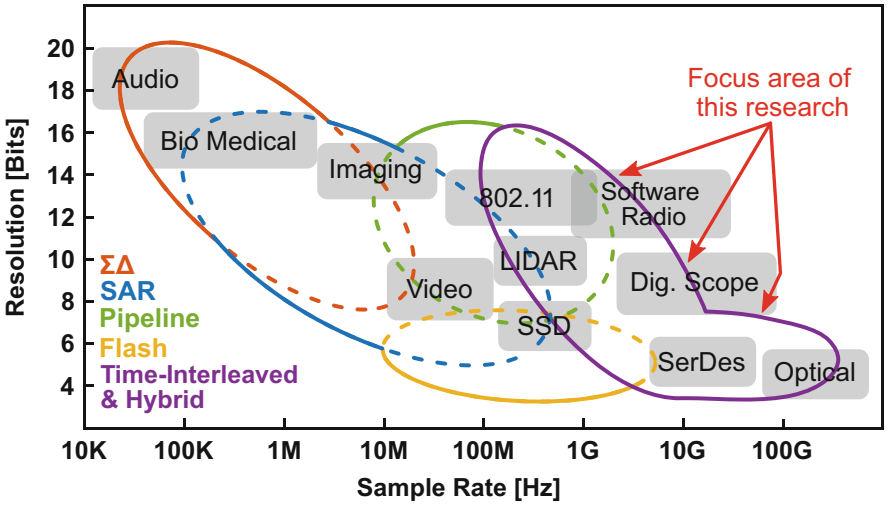

Fig. 1.2 Popular ADC applications and architectures covering them

performed as early as possible in the chain. However, to account for additional and unpredictable signal corruption by the medium, one or more analog conditioning blocks usually precede the converter, whose design is added on the existing set of challenges.

ADCs are employed in a vast and constantly growing number of applications incorporating DSP, either standalone or integrated on the same die or substrate with other blocks composing a larger complex system. More often than not, the performance of the ADC determines the overall performance of the system it is included in. The various applications span a wide range of needs and specifications, including healthcare (diagnostic imaging), consumer electronics (mobile phones, audio, video), automotive (RADAR, LIDAR), next-generation communications (wireline, wireless, optical), and high-end measurement/instrumentation (digital storage oscilloscopes). Some noteworthy applications with established as well as under development specifications are illustrated in Fig. 1.2. To try and meet the demands of such applications, different ADC architectures have been developed. The most widely used up to date are flash, pipeline, Successive Approximation Register (SAR), and sigma-delta ($\Sigma\Delta$). These topologies all have their merits and drawbacks in terms of different specifications, such as sample rate (speed), bandwidth, aggregate resolution, effective resolution (actual), noise, linearity, power consumption, complexity, scalability, etc., making them better tailored for some applications than others. However, as depicted in the conceptual illustration of Fig. 1.2, overlapping target areas exist, such that more than one application can be satisfied by several architectures. To extend the sample rate beyond that of a single converter, time-interleaving has been extensively applied to the above architectures. More recently, hybrid converters have emerged, combining the merits of different

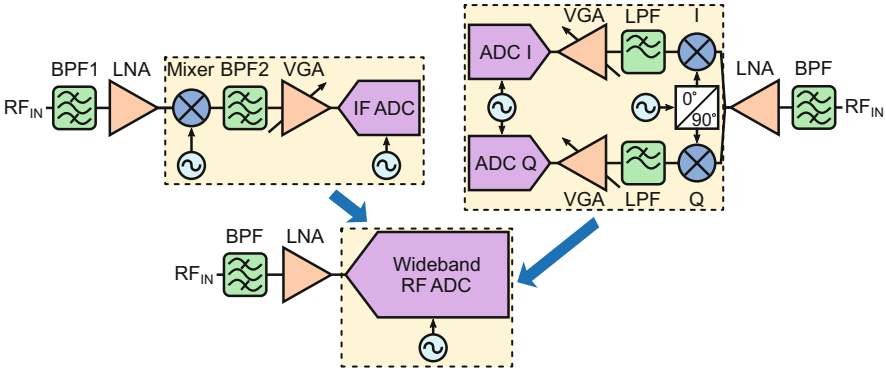

Fig. 1.3 Wideband ADC-based heterodyne (top left) and zero-IF (top right) vs. direct RF sampling receiver (bottom)

architectures,[1] to extend the range of achievable performance and keep up with the rapidly advancing number/demands of future applications.

Undeniably, the field that has established data converters as a hot research topic in both industry and academia for several decades now is that of communications [3]. The constantly increasing demand for higher bandwidth and accuracy in wireline and wireless communication systems is majorly driving the advances in research and development of ADCs, as being key blocks in every receiver. The multi-band requirements of fifth-generation (5G) and future sixth-generation (6G) cellular mobile networks [4] and data over cable networks [5] call for ADCs with high resolution (10–12 bits), multi-GS/s sample rates (5 GS/s or higher), and several GHz of signal bandwidth (half the sample rate or more) while ensuring high linearity (60–70 dB) and low power (preferably below 500 mW). Realizing such ADCs and integrating them with the digital processor in deep-scaled Complementary Metal-Oxide-Semiconductor (CMOS) empower the direct RF sampling receiver topology [6], depicted in Fig. 1.3. This is the closest hardware equivalent to the ideal Software-Defined Radio (SDR) [7]. By leveraging the advanced DSP capabilities in finer CMOS processes, this topology simplifies the analog signal chain and captures multiple bands with a reduced receiver count, lowering area and cost, with improved flexibility and efficiency.

On another high-speed communications front, the rapid emergence of cloud computing and the Internet-of-Things (IoT) has dramatically increased the demand for a higher bandwidth in data center infrastructures. Consequently, the data rates of the transceivers in these systems have reached numbers as high as 112 Gb/s, with future plans to extend to 224 Gb/s and beyond. With Pulse-Amplitude Modulation (PAM-4) currently the prevailing signaling method, for an ADC-based receiver,

[1] One of the proposed prototypes Integrated Circuit (IC)s in this book is a hybrid converter of such kind.

this translates to sample rate requirements of 56 GS/s (112 Gb/s) and a theoretical[2] 112 GS/s (224 Gb/s) with 6–8-bit resolution. To keep up with these sample rates, suitable ADCs are typically realized with a massive amount of time-interleaving ($\geq$64, rarely $\geq$36) [8, 9]. However, this significantly increases the power and area, on top of deteriorating the signal bandwidth due the large input loading. Further, time-interleaving results in offset, gain, timing, and bandwidth mismatches between the different sub-ADCs, which deteriorate accuracy and require complex calibration schemes, further increasing power and complexity. It is of great interest to develop speed-boosting techniques to increase the sub-ADC sample rate (beyond 1 GS/s), such that the aforementioned interleaving-associated drawbacks are reduced while ensuring negligible accuracy degradation as well as minimizing the power and complexity. Again, to maximally exploit the DSP benefits in advanced CMOS nodes, it is favorable to place the ADC on the same chip; therefore, scalable-friendly solutions are highly desirable.

The above applications require very-high-performance multi-GHz ADCs on multiple specifications and are key drivers for future performance advancements. It is important to note that these specifications are highly desirable to enable next-generation communications, but not entirely achievable.[3] As such, they were used to motivate this work in extending the limits beyond what is realizable.

1.2 Challenges in Pushing Performance Boundaries

The previous section briefly discussed some common ADC specifications and requirements for key multi-GHz-range applications. Generally, many different metrics exist, with different importance depending on the target application. However, in a generalized manner, three main parameters encompass the overall ADC performance in a nutshell; these are accuracy, speed, and power. Under accuracy, we include metrics such as aggregate/effective resolution, dynamic range, noise, and linearity. With speed, we denote both sample rate and bandwidth, in the sense that if one increases, the other one must follow. These three main parameters, as illustrated in Fig. 1.4, are bound to each other and influenced by several factors on different levels, such as on a circuit level, an architectural level, a system level, and a technological/process level. These factors present considerable challenges in all the levels, making it non-trivial (even impossible) to simultaneously push all three parameters toward the desired directions, especially at multi-GHz sample rate and bandwidth.

[2] This is one of the potential future options under consideration with several others being investigated, such as PAM-6 or a different signaling method altogether.

[3] At the time of this writing, these applications are undergoing research and prototyping phases to determine viability and long-term reliability.