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Rui Paulo da Silva Martins
Pui-In Mak *Editors*

Analog and Mixed-Signal Circuits in Nanoscale CMOS

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Analog Circuits and Signal Processing

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To all our Families.

Foreword

The world is changing rapidly, and the speed of change depends on modern electronic technologies and their fast advancements. Electronics, or microelectronics products, now govern all modern devices and apparatuses. After the microprocessor's invention, the continuous reduction in size of transistors until almost the physical limit mainly favored digital electronics. Subordinately, there was a development of disciplines that refer to analog electronics. Analog developments have had to adapt to limitations imposed by technological advancements but have also exploited the advantages offered by new technologies.

If we consider the engineering design aspect, we see that there is a substantial difference between digital and analog design. While digital design, which allows a high level of automation, requires innovation at the architectural level, analog design requires mental processing and inventiveness at a much lower complexity, reaching the transistor and layout levels. Indeed, different applications require the use of specific design techniques and strategies. Moreover, since analog functions of a very different nature must operate on the same chip, as happens for the so-called system on chip (SoC), the designers must have a broad spectrum of knowledge while possessing a specific familiarity with their sector of activity.

Market demands have brought requests for various analog engineering skills. They must know how to convert analog to digital, make circuits that arrive at microwave frequencies, and obtain amplification with extremely low noise or handling power at very high or ultra-low levels.

For the above, research laboratories with increasing capability and specific competencies have been born. These laboratories of excellence produce state-of-the-art results, also presented at primary conferences, and published in prestigious scientific journals. More important, their activity indicates the path of innovation in industries. The State Key Lab of Analog and Mixed Signal VLSI of Macau is an example of a scientific reality born and grown to a top level in a few years.

Transferring knowledge from the research and development laboratories to the productive world is a fundamental step of innovation. Unfortunately, advanced knowledge is not available on the shelf and is often tacit (i.e., owned by the

researcher and not codified), hence the vital necessity for methods that facilitate the process. In the digital field, the need is less felt for two reasons. Few industrial players dominate the market and have robust R&D activity internally. The architectural studies for realizing with billions of transistor digital processing functions can be codified and studied using a hierarchical approach. Design automation supports the project phases at a lower level.

Conversely, the transfer of analogical knowledge is problematic. Textbooks provide essential knowledge, and scientific articles summarize advanced knowledge. The status suggests that the activity of an analog designer is like a craftsman (or an artist) that uses their own experience (or inventiveness). There is a gap between basic and advanced knowledge; overcoming this isn't easy.

The knowledge gained from studying textbooks does not go into detail and does not teach the "tricks" that are fundamental to the success of an advanced design. Scientific articles often miss relevant features, and the used wording is for an already experienced audience. Also, they use procedures and research methodologies that only the specialized community often understands. Furthermore, the mathematical foundations are frequently believed to be known and referred to other publications, indicated as bibliographic references.

All this constitutes a barrier to an effective transfer of analog knowledge. How to fill the gap? The procedure is complex because it requires harmonizing the role and needs of two interacting realities, to increase the visibility of research centers, and to identify stimulating research topics. It also needs to collaborate on medium- and long-term issues and educate future engineers and researchers capable of conveying the tacit knowledge accumulated during the study and research periods.

The first essential element for the complex process indicated above is the present book which, as well illustrated in the introduction, describes in suitable detail the knowledge developed in various fields of microelectronics by many scientists of a top research center. The book, other than the desire to “fill the gap,” favors the cooperation between research and production.

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Acknowledgment

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We would like to thank Kass Chow for her precious work in the formatting and editing of the text.

Introduction

General purpose integrated circuits (ICs) emerged in the early 1960s, and the application-specific integrated circuits (ASICs) gained traction in the IC market during the 1980s, highly influencing until now the world of ICs. ASICs are customized ICs for a particular application or end use responsible for expanding the semiconductor industry, changing the respective business model, and significantly increasing IC designs and the working opportunities especially for analog design engineers. ASICs also influenced the whole ecosystem of semiconductor system design, fabrication, and manufacturing, testing, and packaging, as well as the CAD tools. They are completely different from other standard ICs like microprocessors or memories specifically designed for a wide range of applications. On the other hand, analog and mixed-signal ASICs contain both analog and digital circuits, as well as a key building block that is the data converter, in the same chip. Their design allows engineers to explore a great potential to reduce complex multiple IC chips, minimize costs, protect intellectual property, improve reliability and performance, as well as increase miniaturization, bringing down the power consumption. Real-life applications include smart mobile phones, sensor systems with on-chip standard digital interfaces, voice-related signal processing, charge controllers for lithium-ion batteries, unmanned aerial vehicles (or drones), automotive and other electrical vehicles, aerospace electronics, and the fast-developing Internet of Everything (IoE). All this, in a global network that involves communications among the users and the whole universe of around 50 billion electronic gadgets worldwide. Essential in such electronics infrastructure are the brain (CPU), the memory, and the senses (analog/digital interface with audio, vision, and sensors) because a brain does not work without a sensing system. This ubiquitous network operates with data acquired from analog sources, thus connecting two different realities, the analog (physical/real) and the digital (metaverse/virtual) worlds. Since the interface between the two realms plays with analog signals, the most critical building blocks are high-performance radios, power-efficient RF and mm-wave circuits, ultra-low-voltage clock references, low-power and high-performance data converters, integrated energy harvesting interfaces, fully integrated power converters, and low-dropout regulators.

All these circuits need to exhibit high-quality performance with low power consumption, high energy efficiency, and high speed, thus enabling a reliable and consistent development of the IoE while enlarging its frontiers. Since the total market value of the A/D interface is in excess of 20 Billion USD per year, this imposes a huge pressure in the design area with a high demand for analog design engineers. Nevertheless, although this opens a vast field of opportunities for those engineers, it also constitutes a huge challenge for them because it implies a continuous knowledge update to accompany the fast pace of IC technology development down to the nanometer scale in CMOS. Mixed-signal ASIC design offers engineers the possibility of putting their creativity into practice to come about with innovative solutions. Then, the main objective of this book is to present state-of-the-art designs, all based in material from the two top publishing electronics outlets, the *IEEE International Solid-State Circuits Conference (ISSCC)* and the *IEEE Journal of Solid-State Circuits (JSSC)*, adequate for the applications referred above and that are appropriate to stimulate and well equip the mind of future skillful analog design engineers. The authors list of this book also reveals a high quality of international collaboration. This book includes eight chapters organized as follows. Chapter "High-Performance SAW-Less TDD/FDD RF Front-Ends" presents high-performance radio frequency (RF) transceiver (TXR) front-ends, describing first a SAW-less TXR for multiband TDD communications and next a fully integrated multiband FDD SAW-less transmitter (TX) for 5G New Radio (5G-NR). Chapter "Power-Efficient RF and mm-Wave VCOs/PLL" addresses power-efficient RF and mm-wave VCOs, presenting different techniques that enhance the performance of the oscillator, as well as introducing reference-spur-reduction techniques for the subsampling PLL. Chapter "Ultra-Low-Voltage Clock References" puts forward designs and measurement results of two ultra-low-voltage clock references in deep-submicron silicon processes, introducing a regulation-free sub-0.5 V crystal oscillator for energy-harvesting Bluetooth Low Energy (BLE), and also demonstrating a fully integrated 0.35-V temperature-resilient relaxation oscillator using an asymmetric swing-boosted RC network. Chapters "Low-Power Nyquist ADCs" and "High-Performance Oversampling ADCs" give out two types of analog-to-digital converters, namely low power Nyquist and high-performance oversampling, respectively. Chapter "Low-Power Nyquist ADCs", in particular, starts by describing two high-performance pipelined ADCs, a 12-bit SAR-assisted three-stage pipelined ADC with an open-loop Gm-R-based residue amplifier running at 1GS/s, and a 3.3-GS/s 6-bit fully dynamic pipelined ADC using a linearized dynamic amplifier. Besides, it also presents two time-domain ADCs different from conventional voltage-domain ADCs: the first is a 13-bit hybrid ADC which combines a SAR ADC with a time-to-digital converter (TDC), and the second is an 8-bit 10-GS/s time-domain ADC that aggregates four time-interleaved channels. Chapter "High-Performance Oversampling ADCs" initially describes a sturdy multi-stage noise-shaping (MASH) continuous time (CT)–delta sigma modulator (DSM), followed by the analysis of the preliminary sample and quantization technique and finalizing with two different noise-shaping pipeline-SAR ADCs. Chapter "Integrated Energy Harvesting Interfaces" introduces different switched-

capacitor (SC) power converters for several AC-type and DC-type energy-harvesting interfaces that allow full integration, target high system efficiency, and small size for the highly miniaturized Internet of Things (IoT). Chapter "Fully Integrated Switched-Capacitor Power Converters" hands out fully integrated switched-capacitor power converters discussing the topology, analyzing the power conversion losses, introducing techniques to reduce gate-drive switching and parasitic losses, and comparing centralized and distributive clock generation methods for multiphase SC converters. It also presents practical design examples of a SC converter-ring and a multi-output SC converter. Finally, chapter "Hybrid Architectures and Controllers for Low-Dropout Regulators" reports hybrid architectures and controllers for low-dropout regulators, introducing classic LDO control methods and power stage selection, it also details examples of analog-assisted and hybrid control digital LDOs, as well as ampere-level switching LDO for high-performance multi-core processors.

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Part I
Radio Front-Ends and Clock References

High-Performance SAW-Less TDD/FDD RF Front-Ends

Gengzhen Qi, Pui-In Mak, and Rui P. Martins

1 Introduction

In this chapter, we introduce two high-performance radio frequency (RF) transceiver (TXR) front-ends. The first is an SAW-less TXR for multiband TDD communications that employs a novel N-path switched capacitor (SC) gain loop; another is a fully integrated multiband FDD SAW-less transmitter (TX) for 5G new radio (5G-NR).

To achieve an area-efficient SAW-less wireless TXR for multiband TDD communications, we propose an N-path SC gain loop. Unlike the direct-conversion transmitter (TX: BB filter → I/Q modulation → PA driver) and receiver (RX: LNA → I/Q demodulation → BB filter) with such functions arranged in an open-loop style, here we unify the signal amplification, bandpass filtering, and I/Q

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(de)modulation in a closed-loop formation, being reconfigurable as a TX or RX with an LO-defined center frequency. The key advantages are the multiband operation capability in the TX mode and high resilience to OB blockers in the RX mode. Fabricated in 65-nm CMOS, the TXR prototype consumes up to 38.4 mW (20 mW) in the TX (RX) mode at the 1.88-GHz LTE band2. The LO-defined center frequency covers >80% of the TDD-LTE bands with neither on-chip inductors nor external input matching components. By properly injecting (extracting) the signals into (from) the N-path SC gain loop, the TX mode reaches an −1-dBm output power, a −40-dBc $ACLR_{EUTRA1}$, and a 2.0% EVM at 1.88 GHz, while showing a −154.5-dBc/Hz OB noise at 80-MHz offset. In the RX mode, we measured a 3.2-dB NF and a + 8-dBm OB-IIP_3. The active area (0.038 mm^2) of the TXR is 24 times smaller than the state-of-the-art LTE solutions.

Besides that, we also report a fully integrated multiband FDD SAW-less TX for 5G-NR. It features the following: (1) a bandwidth-extended N-path filter modulator (BW-Ext FIL-MOD) to enable high-Q bandpass filtering at a flexible RF, with its bandpass characteristic enhanced through the synthesis of a complex pole pair via merging positive and negative feedback networks (PFN/NFN), thus surmounting the trade-off between the passband flatness and out-of-band (OB) rejection; (2) an isolated baseband (BB) input network to avoid the mutual loading effect between the BW-Ext FIL-MOD and itself; and (3) a transimpedance amplifier (TIA)-based power amplifier driver (PAD) to absorb both the bias and signal currents of the BW-Ext FIL-MOD for better linearity and power efficiency. Fabricated in 28-nm CMOS, the TX manifests a 20-MHz passband BW and a consistently low OB noise (≤ −157.5 dBc/Hz) for different 5G-NR bands between 1.4 and 2.7 GHz. The circuit exhibits sufficient output power (3 dBm) and high TX efficiency (2.8–3.6%) concurrently with high linearity ($ACLR_1$ <44 dBc and EVM <2%). The active area is 0.31 mm^2.

The organization of this chapter is the following:

Section 2 introduces an N-Path SC gain loop as a SAW-less TXR for multiband TDD communications. Section 2.1 introduces the properties of the SC gain loop that holds a number of promises of being a reconfigurable TXR. Section 2.2 describes how it is possible to embed the gain-boosted N-path technique into the SC gain loop to build the SAW-less TX mode. In Sect. 2.3, we report the SAW-less RX mode utilizing a switched BB extraction technique to improve further the NF. Section 2.4 describes the LO (local oscillator) generator (LOGEN) with the TX−/RX-mode control logics, followed by the measurement results in Sect. 2.5. Finally, Sect. 2.6 draws the conclusions.

Section 3 introduces the SAW-less multiband transceiver using an N-path SC gain loop. Section 3.1 introduces the BW-Ext FIL-MOD and compares it with the original FIL-MOD. Section 3.2 details the TX design and analyzes it using both the functional view approach and LTI-based transfer function. Other details are for the isolated BB input network, wideband TIA-based PAD, and low-power LOGEN. Section 3.3 summarizes the measurement results and Sect. 3.4 presents the conclusions.

2 SAW-Less Multiband Transceiver Using an N-Path SC Gain Loop

In order to develop multiband cellular radios at low cost, on-chip N-path switched capacitor (SC) filters [1] rekindled as a promising replacement of the off-chip SAW filters. The improved speed and parasitic effects of ultra-scaled CMOS technologies enable the N-path SC filters to provide tunable high-Q filtering over a wide range of frequencies [2, 3]. Beyond filtering, N-path mixing also facilitates wideband receivers (RXs) to achieve input matching and harmonic rejection [4–6]. The mixer-first wideband RX [4] shows a high out-of-band (OB)-IIP_3 (+25 dBm) while covering a wide RF range (0.1–2.4 GHz), but the NF (5 dB) becomes a hard trade-off with the power consumption (70 mW) due to the absence of RF gain. The noise-canceling RX [5] balances better between the OB-IIP3 (+13.5 dBm) and NF (1.9 dB), but its dual-path topology involves extra mixing and baseband (BB) circuitries, consuming more area (1.2 mm^2) and power (78 mW). Recently reported, a gain-boosted N-path technique led to a single-mixing blocker-tolerant RX [6] with competitive OB-IIP3 (+13 dBm) and NF (1.5–2.9 dB) at smaller area (0.028 mm^2) and power (11 mW). Regrettably, it demands a high gain-boosting factor (200 mS), which strongly restricts the signal bandwidth (BW = 2.6 MHz) and RF coverage (<1.5 GHz); both are inadequate for modern cellular standards such as the LTE.

SAW-less transmitters (TXs) confront a different challenge as the effort is on lowering the OB noise and spectral leakage, especially at the nearby RX bands (<100-MHz offset). The SAW-less TX in [7] exploits direct quadrature voltage modulation to lower the OB noise (−159 dBc/Hz at 40-MHz offset) and raise the power efficiency (5.7%). Its power amplifier driver (PAD) is the only gain stage, rendering the OB noise primarily dominated by the thermal noise of the passive mixers and phase noise of the LO generator. Nevertheless, its PAD relies on a passive LC load to deliver the required output power (P_{out}) and suppress the OB harmonics, being inflexible to support multiband communications. In fact, recent SAW-less multiband TXs still rely on dedicated baluns to extend the RF coverage. An example is the current-mode SAW-less TX in [8] that exhibits a −158-dBc/Hz OB noise at the RX band (30-MHz offset), but demanding large die area (1.06 mm^2), and power (96 mW) for its mixer and voltage-to-current converter that have to be linear and low noise.

We present an N-path SC gain loop as a SAW-less TXR for multiband TDD communications, entailing no on-chip inductors or external passives for input matching. Unlike the typical TXRs with the building blocks cascaded in an open-loop style to build up the RF-to-BB (or BB-to-RF) signal-processing chain, here the N-path SC gain loop operates in a closed-loop style to unify the TX and RX functions, allowing a very compact multiband TXR (0.038 mm^2). Measured at the LTE-band2 (1.88 GHz) and band5 (0.836 GHz), the TX mode exhibited an $ACLR_{EUTRA1}$ <−40 dBc, an EVM ≤2.1%, and a low output noise of <−154 dBc/Hz at 80-MHz offset. The RX mode drew 20-mW power and exhibited a 3.2-dB NF and a + 8-dBm OB-IIP_3 at 1.88 GHz.

2.1 *Principle of the SC Gain Loop as a TXR*

Comparatively, a SAW-less RX should be able to amplify a weak in-band (IB) signal in the presence of large OB blockers, whereas a SAW-less TX ought to be able to deliver a large IB signal with low OB noise and spectral leakages. Such discrepancy inspires the exploration of a RX-TX-compatible N-path technique to implement a reconfigurable TXR suitable for TDD-LTE (even FDD-LTE, by duplicating the TXR as separated TX and RX modes). To build this concept, Fig. 1a presents an SC gain loop. We create the primary functions of TX and RX with a gain stage rounded by a SC network that consists of a capacitor C_F and two switches. Empirically, we can recognize "upmix + gain" as a TX function (Fig. 1b), with the BB signal injected between the left-hand switch and C_F and the RF signal extracted from the gain stage's output. Based on the Miller effect, the extra downmix path helps reusing the gain stage to boost the effective C_F and reduce the effective on-resistance of the two switches. Besides, with the right-hand switch, the gain stage's output sees a large RF impedance, avoiding any unwanted gain drop. By transforming the SC network into an N-path SC network, we can embed the gain-boosted N-path technique [9] into such a gain loop, unifying the key TX functions in a closed-

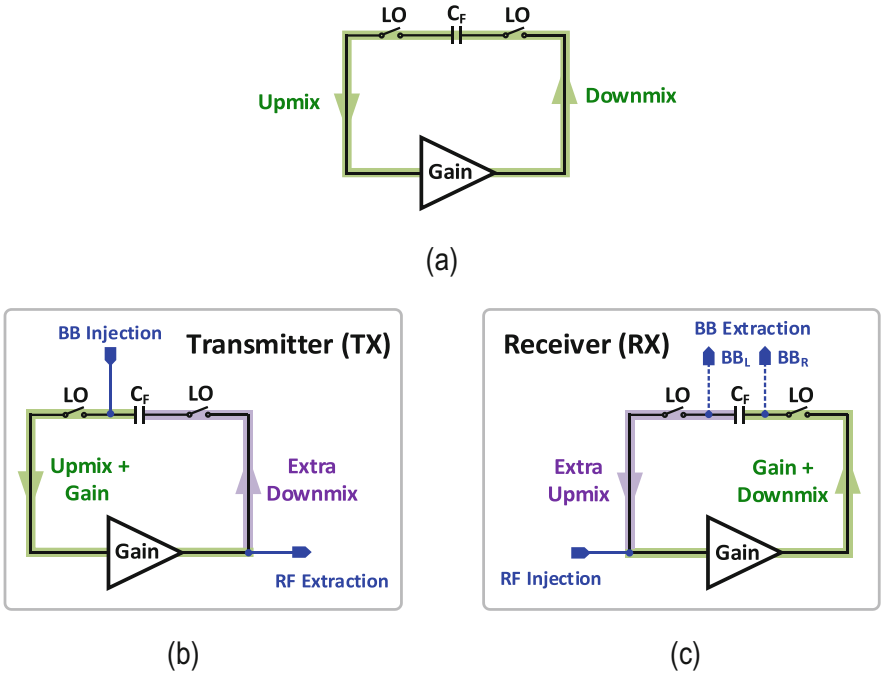

Fig. 1 (**a**) An SC gain loop performs gain, downmix and upmix in a self-feed manner. It can operate as a (**b**) TX under BB injection and RF extraction or (**c**) RX under RF injection BB extraction. The extra downmix and upmix paths allow gain-boosted N-path filtering. For RX, there are two BB extraction solutions, BBL (without right-hand switch) and BBR

loop style: (1) signal amplification, (2) high-Q bandpass filtering, and (3) I/Q modulation.

Figure 1c shows that the SC gain loop is reconfigurable as a RX by using the "gain + downmix" function. Specifically, with the RF signal injected at the gain stage's input, we can extract the BB signal around C_F. Similar to the TX mode, the extra upmix path allows it to be compatible with the gain-boosted N-path technique. The resultant RX essentially offers the key functions: (1) signal amplification, (2) high-Q bandpass filtering, (3) I/Q demodulation, and (4) input impedance matching.

2.2 N-Path SC Gain Loop as a TX

TX-Mode Architecture

From Fig. 2, with $N = 4$, the N-path SC gain loop becomes a practical TX by adding four passive RC filters $R_{BT}C_{BT}$ to receive the general four-phase BB signals $V_{BB,\ TX1\ -\ 4}$ (i.e., differential and I/Q). Switches SW_L and SW_R perform the upmix and downmix functions, respectively, around the gain stage (G_{mRF}). G_{mRF} is an inverting amplifier that ensures the gain loop is under negative feedback. Outside the gain loop, the utilization of a wideband PAD boosts the gain, provides isolation, and drives the off-chip 50-Ω load.

With SW_L and SW_R activated periodically by a four-phase nonoverlap LO, the capacitor C_F charges with an in-phase BB voltage at one side, while charging an amplified out-phased BB voltage on the other side. As such, the loop gain due to the Miller effect boosts the effective capacitance of C_F at the input. This mechanism not only reduces the chip area for C_F but also its parasitic effects, allowing the TX mode to operate at a higher RF. Another key aspect is that we embed high-Q bandpass filtering at both $V_{i,\ TX}$ and $V_{o,\ TX}$ sharing one N-path SC network. Further, we sum the IB RF voltage in-phase over a switching period, while the OB RF voltage cancels out at both $V_{i,\ TX}$ and $V_{o,\ TX}$. Unlike the typical passive N-path filter with the OB rejection limited by the on-resistance of the switches, here the loop gain offered by G_{mRF} alleviates such a limit due to the on-resistance division by the open loop gain (i.e., high OB rejection without consuming large LO power).

Functional View of the TX Mode

Figure 3a presents, for intuitive understanding, a functional view of the TX mode. It is not an equivalent circuit, since the "I/Q modulation" and "high-Q bandpass filtering" appear unmerged as two cascaded functions to illustratively make a comparison with [7]. The I/Q modulation is alike a typical TX, synthesizing an RF signal at $V_{i,\ TX}$ from a four-phase BB signal at $V_{BB,\ TX1\ -\ 4}$. $V_{i,\ TX}$ virtually passes through a high-Q bandpass filter that can reject the OB noise first at $V_{i,\ TX}$ and second

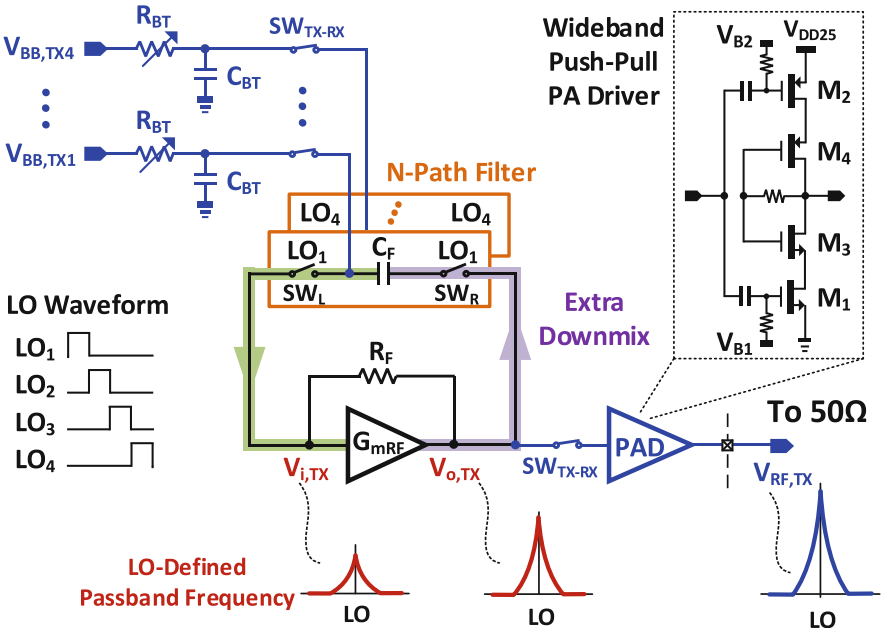

Fig. 2 Four-path SC gain loop as a TX. Injection of the four-phase BB ($V_{\mathrm{BB,\ TX1\ -\ 4}}$) via R_{BT}. The PAD extracts $V_{\mathrm{o,\ TX}}$ and drives the 50 Ω. Gain-boosting the N-path filter by G_{mRF} realizes high-Q bandpass responses at $V_{\mathrm{i,\ TX}}$ and $V_{\mathrm{o,\ TX}}$

at $V_{\mathrm{o,\ TX}}$. We can model the N-path SC network as a linear-time-invariant (LTI) RLC resonator around the passband [2], where the tunable inductor represents a tunable center frequency. Interestingly, when we omit the extra downmix path in Fig. 2, the closed-loop TX returns to an open-loop style similar to [7] that aims at low OB noise emission by direct quadrature voltage modulation (Fig. 3b). The narrowband PAD in [7] exploits a passive LC resonator for unwanted harmonic attenuation (<-40 dBc), and hence the output response has a low Q and fixed center frequency. Unlike [7], here we reuse the gain created by G_{mRF} to boost the Q of the bandpass responses at $V_{\mathrm{i,\ TX}}$ and $V_{\mathrm{o,\ TX}}$, resulting in much stronger OB noise suppression. To exemplify it, Fig. 4 plots the simulated gain responses at $V_{\mathrm{i,\ TX}}$ and $V_{\mathrm{o,\ TX}}$ at 2 GHz. Without the extra downmix path, $V_{\mathrm{i,\ TX}}$ offers only 11-dB OB rejection with no further improvement added at $V_{\mathrm{o,\ TX}}$. For the proposed TX, the rejection at $V_{\mathrm{i,\ TX}}$ improves to 22.5 dB, with an extra rejection of 7.8 dB added at $V_{\mathrm{o,\ TX}}$. There is a 1.6-dB gain drop at $V_{\mathrm{o,\ TX}}$ in the TX, due to the finite frequency-translated impedance of the extra downmix path. Also, the gain response in Fig. 4 refers the four-phase BB to the single-phase RF. If considering the single-phase BB to the single-phase RF, the gain value is 9 dB higher. This fact applies to all plotted gain responses of the TX mode (presented later).

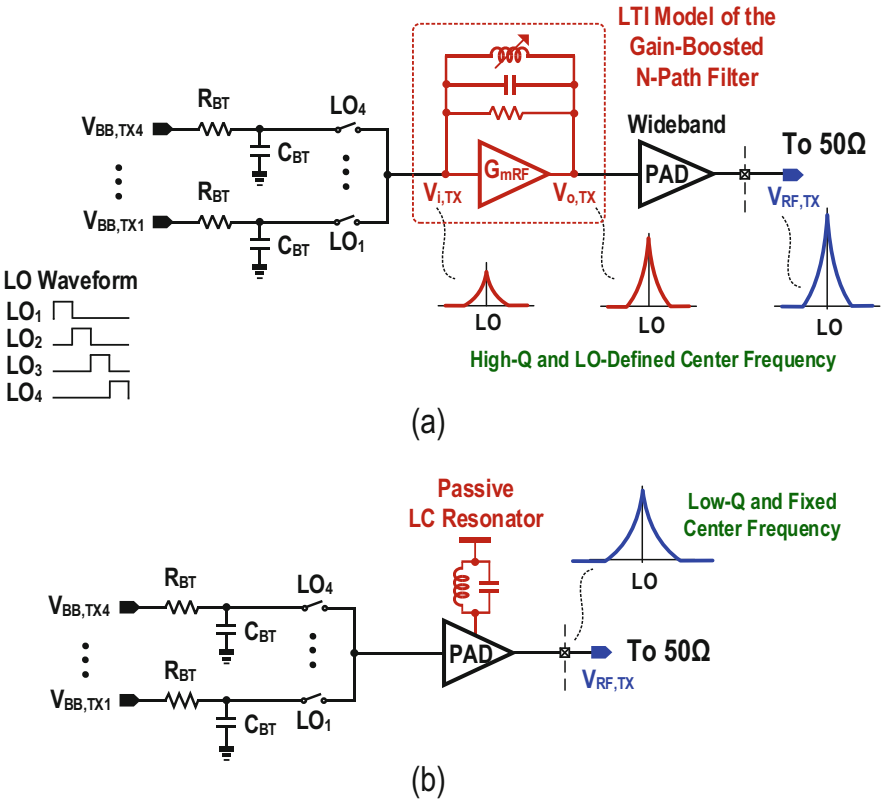

Fig. 3 (**a**) Functional view of the TX, we can compare it with [7] (**b**) that uses a passive LC resonator for its narrowband PAD. This work features a gain-boosted N-path filter and a wideband PAD to allow high-Q filtering and LO-defined center frequency, being more flexible for multiband operation

TX-Mode Open-Loop Equivalent Model

To simplify the quantitative study, we develop an open-loop equivalent model of the TX mode illustrated in Fig. 5. Inspired by the principle of Miller decomposition, the N-path SC network has a subdivision into two parts referring to the gain stage's output and input. The former is alike a typical passive N-path filter [9] hanged on $V_{o,TX}$, while the latter becomes four separated SC networks (i.e., single path, single phase) placed between the BB passive filter $R_{BT}C_{BT}$ and voltage mixer SW_L. We can model the input-referred on-resistance of SW_R ($R_{SWR,i}$) and the input-referred Miller capacitance of C_F ($C_{F,i}$) at BB as

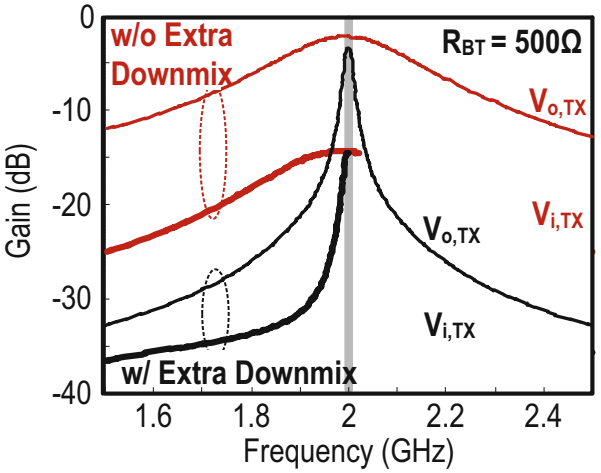

Fig. 4 Simulated TX-mode gain responses at $V_{i,\,TX}$ and $V_{o,\,TX}$ with and without the extra downmix path at 2 GHz

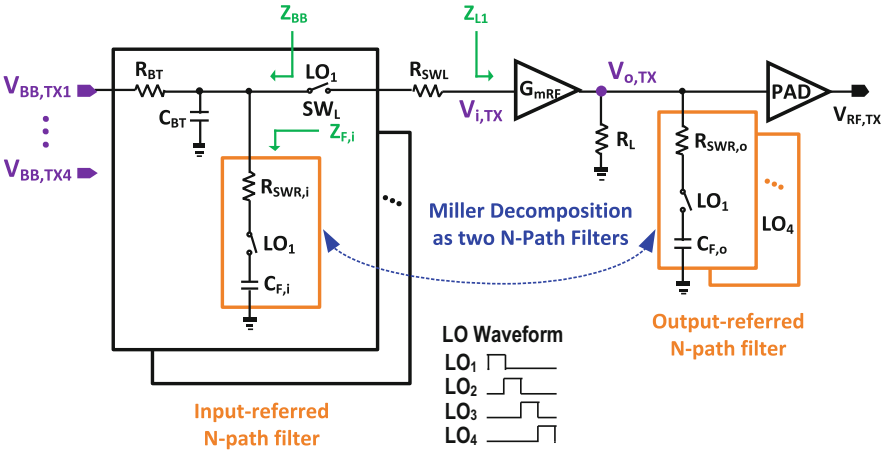

Fig. 5 Proposed open-loop TX model, with the gain-boosted N-path filter decomposed into two N-path filters using the principle of Miller decomposition [9]. R_F (9.3 kΩ) is large enough and omitted

$$\begin{cases} R_{\mathrm{SWR,i}} = \dfrac{R_{\mathrm{SWR}}//R_{\mathrm{F}} + R_{\mathrm{L}}}{1 + G_{\mathrm{mRF}}R_{\mathrm{L}}} \\ R_{\mathrm{SWR,o}} = \dfrac{R_{\mathrm{SWR}}//R_{\mathrm{F}} + R_{\mathrm{SWR}}}{1 + G_{\mathrm{mRF}}R_{\mathrm{SWR}}} \\ C_{\mathrm{F,i}} = \left|C_{\mathrm{F}} \cdot \dfrac{(1 - G_{\mathrm{mRF}}R_{\mathrm{F}})R_{\mathrm{L}}}{R_{\mathrm{F}} + R_{\mathrm{L}}}\right| \\ C_{\mathrm{F,o}} = C_{\mathrm{F}} \end{cases} \tag{1}$$

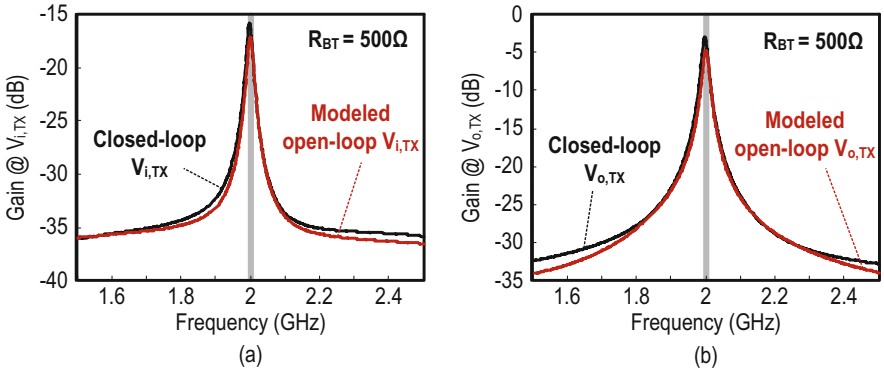

Fig. 6 Comparison of modeled and simulated gain responses: (**a**) open-loop $V_{i,\,TX}$ in Fig. 5 versus the closed-loop $V_{i,\,TX}$ in Fig. 2 and (**b**) open-loop $V_{o,\,TX}$ in Fig. 5 versus the closed-loop $V_{o,\,TX}$ in Fig. 2

where $R_{SWR,\,o}$ is the output-referred switch's on-resistance, $C_{F,\,o}$ is the Miller capacitance at $V_{o,\,TX}$, and R_L is the load impedance of G_{mRF}. The modeled $C_{F,\,i}$ in Eq. (1) is equal to C_F multiplied by the open-loop gain of G_{mRF}. The enlarged $C_{F,\,i}$ implies less physical capacitors to realize a specific BW. For instance, with $G_{mRF} = 130$ mS, $R_F = 9.3$ kΩ, $R_L = 38.4$ Ω, and $C_F = 8$ pF, the computed $C_{F,\,i}$ is 39.7 pF which is ~5× more area efficient than the general passive N-path filter [2]. Also, the circuit suppresses the effective resistance $R_{SWR,\,i}$ (10 Ω) and $R_{SWR,\,o}$ (11.3 Ω) through G_{mRF}, improving the OB rejection.

To verify the accuracy of the model, Fig. 6a plots the gain responses at $V_{i,\,TX}$ simulated with $R_{BT} = 500$ Ω, where the modeled open-loop response fits well with the closed-loop, except that there is a 1.2-dB gain drop due to the input parasitic capacitance of G_{mRF}. The modeled gain response of the open-loop $V_{o,\,TX}$ is accurate (Fig. 6b), which has a better OB rejection (~2 dB) as the far-out blockers see a smaller impedance at the open-loop $V_{o,\,TX}$.

Gain Response

Based on the open-loop equivalent model above, we can study the gain response from BB to $V_{RF,\,TX}$ in two steps. Recalling Fig. 5, the gain stage G_{mRF} essentially isolates its preceding and following stages, allowing first the computation of the transfer function from BB to $V_{i,\,TX}$, followed by that from $V_{i,\,TX}$ to $V_{RF,\,TX}$. For the former, we employed a simplified equivalent circuit (Fig. 7a). Since the input impedance seen from G_{mRF} is mainly capacitive (C_1), we can denote the load impedance as $Z_{L1}(\omega) = 1/j\omega C_1$. Here, the angular frequency ω is close to ω_{LO}. In view of the BB, the input voltage $V_{BB,\,TX1\,-\,4}$ is in series with the BB impedance which becomes.

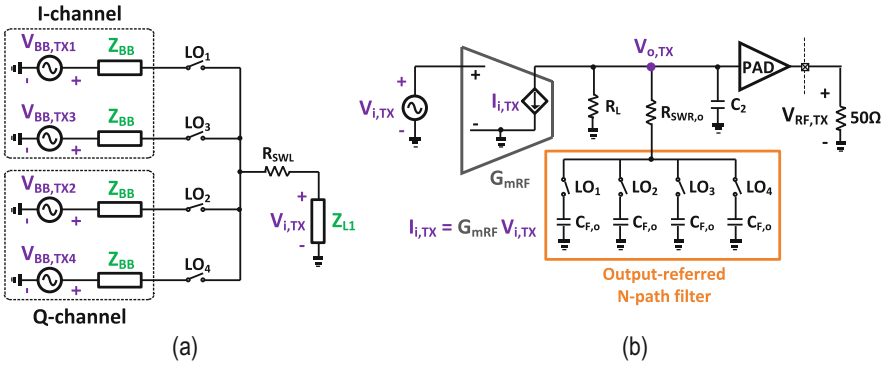

Fig. 7 Simplified circuit for calculating the responses: (**a**) from BB to $V_{\mathrm{i,\ TX}}$ of the open-loop TX and (**b**) from current source $I_{\mathrm{i,\ TX}}$ to $V_{\mathrm{RF,\ TX}}$. $I_{\mathrm{i,\ TX}}$ is equal to the transconductance G_{mRF} multiplied by $V_{\mathrm{i,\ TX}}$

$$Z_{\mathrm{BB}}(\omega-\omega_{\mathrm{LO}})=R_{\mathrm{BT}}//\frac{1}{j(\omega-\omega_{\mathrm{LO}})C_{\mathrm{BT}}}//Z_{\mathrm{F,i}}(\omega-\omega_{\mathrm{LO}}) \tag{2}$$

where $Z_{\mathrm{F,\ i}}(\omega-\omega_{\mathrm{LO}})$ (Fig. 5) is the impedance of a single path decomposed from the extra downmix path. Since the SC circuit operates as a BB-to-BB gain response, we can ignore the high-order frequency components and represent $Z_{\mathrm{F,\ i}}(\omega-\omega_{\mathrm{LO}})$ as.

$$Z_{\mathrm{F,i}}(\omega-\omega_{\mathrm{LO}})\approx 4R_{\mathrm{SWR,i}}+\frac{1}{j(\omega-\omega_{\mathrm{LO}})C_{\mathrm{F,i}}} \tag{3}$$

which enhances the BB rejection due to the boosted capacitance of $C_{\mathrm{F,\ i}}$. Putting Eq. (3) into Eq. (2), $Z_{\mathrm{BB}}(\omega-\omega_{\mathrm{LO}})$ expands to.

$$Z_{\mathrm{BB}}(\omega-\omega_{\mathrm{LO}})=\frac{1}{1/R_{\mathrm{BT}}+j(\omega-\omega_{\mathrm{LO}})C_{\mathrm{BT}}+\frac{j(\omega-\omega_{\mathrm{LO}})C_{\mathrm{F,i}}}{1+4R_{\mathrm{SWR,i}}\cdot j(\omega-\omega_{\mathrm{LO}})C_{\mathrm{F,i}}}} \tag{4}$$

At center frequency with $\omega=\omega_{\mathrm{LO}}$, the impedance is R_{BT} in Eq. (4), and when ω moves away from ω_{LO}, the impedance starts to roll off. The −3-dB BW approaches $1/R_{\mathrm{BT}}(C_{\mathrm{BT}}+C_{\mathrm{F,\ i}})$ if $R_{\mathrm{SWR,\ i}}$ is close to zero. In this case, $C_{\mathrm{F,\ i}}$ dominates the BB BW and the ultimate rejection is infinite. If enlarging $R_{\mathrm{SWR,\ i}}$, the −3-dB BW widens and finally converges to $1/R_{\mathrm{BT}}C_{\mathrm{BT}}$.

According to the LTI expression of the up-converted RF voltage in [10], we can obtain the RF voltage $V_{\mathrm{i,\ TX}}$ transferred from $V_{\mathrm{BB,\ TX1\ -\ 4}}$ in Fig. 7a as.

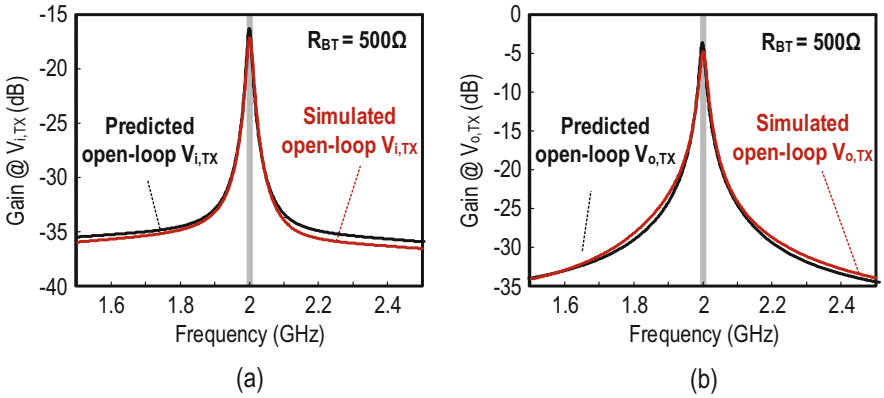

Fig. 8 Comparison of gain responses: (**a**) simulated open-loop $V_{\mathrm{i,\ TX}}$ versus the approximation of Eq. (5) and (**b**) simulated open-loop $V_{\mathrm{o,\ TX}}$ versus the approximation of Eq. (8)

$$V_{\mathrm{i,TX}}(\omega) = \frac{\sqrt{2}}{\pi} \frac{Z_{\mathrm{L1}}(\omega) \cdot Z_{\mathrm{BB}}(\omega - \omega_{\mathrm{LO}})/R_{\mathrm{BT}}}{Z_{\mathrm{L1}}(\omega) + R_{\mathrm{SWL}}} \times \frac{e^{j\pi/4} \cdot V_{\mathrm{BB,TX1}}(\omega - \omega_{\mathrm{LO}}) + e^{-j\pi/4} \cdot V_{\mathrm{BB,TX2}}(\omega - \omega_{\mathrm{LO}})}{1 + \frac{2}{\pi^2} Z_{\mathrm{BB}}(\omega - \omega_{\mathrm{LO}}) \sum_{m=-\infty}^{+\infty} \frac{1}{(4m+1)^2 (Z_{\mathrm{L1}}(4m\omega_{\mathrm{LO}} + \omega) + R_{\mathrm{SWL}})}} \tag{5}$$

where m is an integer. Figure 8a plots Eq. (5) for 2 GHz which matches well with the simulated curve spanning from 1.5 to 2.5 GHz. The term of infinite summation in Eq. (5) comprises the fundamental and higher odd-order harmonics. Since the fundamental term is dominant, we can simplify Eq. (5) as.

$$V_{\mathrm{i,TX}}(\omega) \approx \frac{\sqrt{2}}{\pi} \frac{Z_{\mathrm{L1}}(\omega) \cdot Z_{\mathrm{BB}}(\omega - \omega_{\mathrm{LO}})/R_{\mathrm{BT}}}{Z_{\mathrm{L1}}(\omega) + R_{\mathrm{SWL}} + \frac{2}{\pi^2} Z_{\mathrm{BB}}(\omega - \omega_{\mathrm{LO}})} \times \left(e^{j\pi/4} \cdot V_{\mathrm{BB,TX1}}(\omega - \omega_{\mathrm{LO}}) + e^{-j\pi/4} \cdot V_{\mathrm{BB,TX2}}(\omega - \omega_{\mathrm{LO}}) \right) \tag{6}$$

where $V_{\mathrm{i,\ TX}}(\omega)$ provides an intuitive view of the low-pass response of $Z_{\mathrm{BB}}(\omega - \omega_{\mathrm{LO}})$ up-converted to $V_{\mathrm{i,\ TX}}$ as a high-Q bandpass response, with a −3-dB BW around twice of that from Eq. (4).

Similarly, to analyze the response from $V_{\mathrm{i,\ TX}}$ to $V_{\mathrm{RF,\ TX}}$ of the open-loop TX model, we developed a simplified circuit (Fig. 7b), with G_{mRF} modeled as a transconductor converting the input $V_{\mathrm{i,\ TX}}$ to an output current $I_{\mathrm{i,\ TX}}$, expressed as $I_{\mathrm{i,\ TX}} = G_{\mathrm{mRF}} V_{\mathrm{i,\ TX}}$. C_2 is the input parasitic capacitance of the PAD. $I_{\mathrm{i,\ TX}}$ draws current from R_{L}, C_2, and the output-referred N-path filter to create the RF voltage $V_{\mathrm{o,\ TX}}$. As the PAD involves no frequency translation and its passband gain should be flat, our focus is on the response from $V_{\mathrm{i,\ TX}}$ to $V_{\mathrm{o,\ TX}}$. Referring to Eq. (13), the impedance $Z_{\mathrm{o,\ TX}}(\omega)$ seen by $V_{\mathrm{o,\ TX}}$ is as follows:

$$Z_{\mathrm{o,TX}}(\omega)=\frac{R_{\mathrm{SWR,o}}\cdot Z_{\mathrm{L2}}(\omega)}{R_{\mathrm{SWR,o}}+Z_{\mathrm{L2}}(\omega)} + \frac{\left(\frac{Z_{\mathrm{L2}}(\omega)}{R_{\mathrm{SWR,o}}+Z_{\mathrm{L2}}(\omega)}\right)^2\cdot\frac{2}{\pi^2}Z_{\mathrm{F,o}}(\omega-\omega_{\mathrm{LO}})}{1+\frac{2}{\pi^2}Z_{\mathrm{F,o}}(\omega-\omega_{\mathrm{LO}})\sum_{m=-\infty}^{+\infty}\frac{1}{(4m+1)^2(Z_{\mathrm{L2}}(4m\omega_{\mathrm{LO}}+\omega)+R_{\mathrm{SWR,o}})}} \tag{7}$$

where $Z_{\mathrm{L2}}(\omega)=R_{\mathrm{L}}//\frac{1}{j\omega C_2}$ and $Z_{\mathrm{F,o}}(\omega-\omega_{\mathrm{LO}})=\frac{1}{j(\omega-\omega_{\mathrm{LO}})C_{\mathrm{F,o}}}$. Thus, $V_{\mathrm{o,TX}}$ will be.

$$V_{\mathrm{o,TX}}(\omega)=G_{\mathrm{mRF}}Z_{\mathrm{o,TX}}(\omega)\cdot V_{\mathrm{i,TX}}(\omega) \tag{8}$$

From Fig. 8b, the prediction of Eq. (8) fits well with the simulations covering a 1-GHz span at LO = 2 GHz. By ignoring higher harmonics, we can simplify Eq. (7) just to a high-Q bandpass impedance as below:

$$Z_{\mathrm{o,TX}}(\omega)=\frac{Z_{\mathrm{L2}}(\omega)}{Z_{\mathrm{L2}}(\omega)+R_{\mathrm{SWR,0}}}\cdot\left(R_{\mathrm{SWR,o}}+\frac{Z_{\mathrm{L2}}(\omega)}{1+j\frac{\pi^2}{2}C_{\mathrm{F,0}}(R_{\mathrm{L}}+R_{\mathrm{SWR,o}})(\omega-\omega_{\mathrm{LO}})}\right). \tag{9}$$

At the center frequency, Eq. (9) is equal to $Z_{\mathrm{L2}}(\omega)$, and then, it is interesting that the output-referred N-path load does not bring any gain drop if the harmonics are out of concern [11]. However, the parasitic capacitance C_2 induces a $1/(1+j\omega R_{\mathrm{L}}C_2)$ gain drop (e.g., −0.6 dB at 2 GHz). Also, the −3-dB BW of the high-Q bandpass filtering is equal to $4/\pi^2 C_{\mathrm{F,\ o}}(R_{\mathrm{L}}+R_{\mathrm{SWR,\ o}})$ when $Z_{\mathrm{L2}}(\omega)$ is resistive.

Noise Analysis

Most OB noise of the TX mode results from the thermal noises of the R_{BT}, the gain stage G_{mRF}, and the on-resistance R_{SWL}. As modeled in Fig. 9a, the thermal noise voltage $V_{\mathrm{n,\ RBT}}$ is in series with the BB impedance and experiences the same transfer function of the BB signals. As such, the power spectral density (PSD) at $V_{\mathrm{n,\ oTX}}$ due to R_{BT} is.

$$\overline{V^2_{\mathrm{n,R_{BT,oTX}}}}=|H_{\mathrm{i,TX}}(\omega)|^2\cdot|H_{\mathrm{o,TX}}(\omega)|^2\cdot\overline{V^2_{\mathrm{n,R_{BT}}}} \tag{10}$$

where we introduce $|H_{\mathrm{i,\ TX}}(\omega)|$ and $|H_{\mathrm{o,\ TX}}(\omega)|$ as the transfer functions from BB to $V_{\mathrm{i,\ TX}}$ and $V_{\mathrm{i,\ TX}}$ to $V_{\mathrm{o,\ TX}}$, respectively, to represent Eqs. (5) and (8). The thermal noise power of R_{BT} is $\overline{V^2_{\mathrm{n,R_{BT}}}}=4kTR_{\mathrm{BT}}$. The high-Q bandpass filtering in the N-path SC gain loop greatly suppresses the OB noise contribution from R_{BT}. Similarly, the output noise PSD due to R_{SWL} is.

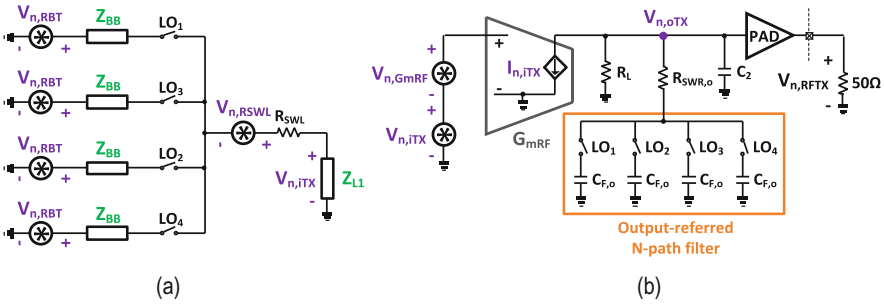

Fig. 9 Simplified equivalent circuit for noise analysis of (**a**) R_{BT} and SW_L and (**b**) G_{mRF}

$$\overline{V^2_{n,R_{SWL},oTX}} = \left(\frac{R_{BT}}{Z_{BB}(\omega-\omega_{LO})}\right)^2 \cdot |H_{i,TX}(\omega)|^2 \cdot |H_{o,TX}(\omega)|^2 \cdot \overline{V^2_{n,R_{SWL}}} \tag{11}$$

where $\overline{V^2_{n,R_{SWL}}} = 4kTR_{SWL}$. In Fig. 9b, we modeled the thermal voltage source of the G_{mRF} stage as an input-referred $V_{n,\ GmRF}$, and the corresponding noise power is $\overline{V^2_{n,GmRF}} = 4kT/G_{mRF}$. $V_{n,\ GmRF}$ experiences the same transfer function as $V_{n,\ iTx}$; thus the output noise PSD due to G_{mRF} is.

$$\overline{V^2_{n,GmRF,oTX}} = |H_{o,TX}(\omega)|^2 \cdot \overline{V^2_{n,GmRF}}. \tag{12}$$

Figure 10a, b exhibit the simulated output noises at $V_{o,\ TX}$ due to R_{BT} and G_{mRF}, as well as due to SW_L and SW_R, respectively. When the offset frequency is beyond 70 MHz, G_{mRF} generates more noise than that of R_{BT} as it experiences less OB rejection within the N-path SC gain loop. When comparing it with SW_L, SW_R contributes with less noise due to the lack of amplification in the extra downmix path (Fig. 2). Furthermore, the output noises shown in Fig. 10 are almost flat, with the offset frequency referred over 80 MHz. Upsizing the switches $SW_{L,\ R}$ can lead to a lower output noise floor, at the expense of more LO power.

Figure 11 displays the simulated harmonic folding effect at $V_{o,\ TX}$. For $N = 4$, the nearest and strongest component that folds back to the desired band (around LO) is 3xLO and after is 5xLO [10]. Even though the TX is single-ended, the even harmonic folding is insignificant (simulated <-70 dB). Due to the high-Q bandpass filtering of the gain-boosted N-path technique around 3xLO and 5xLO, the far-out noise induced by the folding terms is much smaller than the IB that experiences no frequency translation. Thus, the harmonic folding effect is generally less important in the TX design.

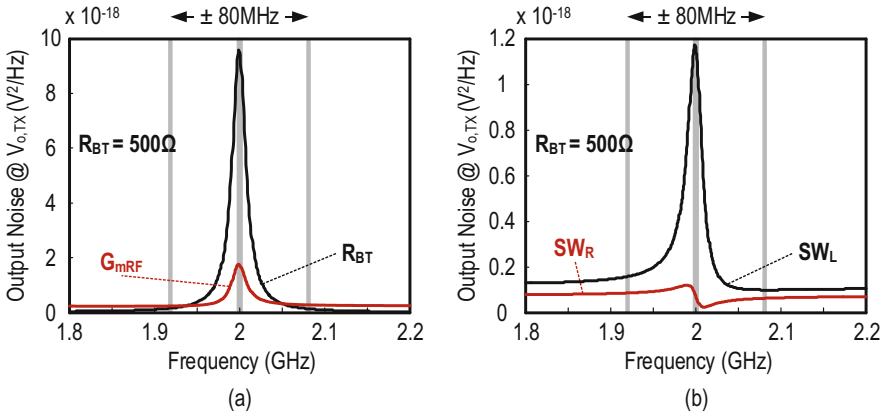

Fig. 10 Simulated output noise power at $V_{o,\,TX}$ with contribution from (**a**) R_{BT} and G_{mRF} and (**b**) SW_L and SW_R

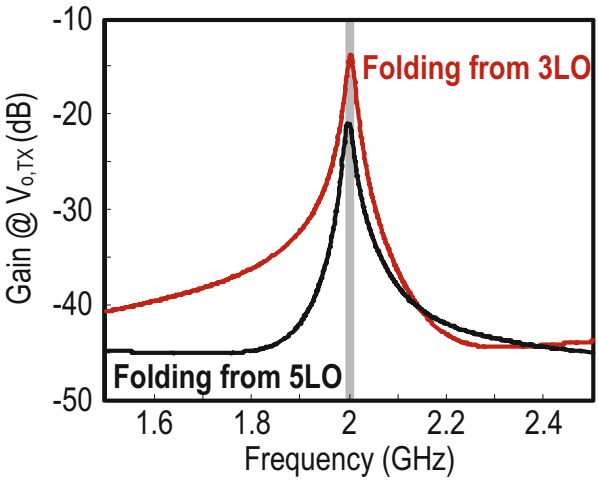

Fig. 11 Simulated unwanted folding terms from 3LO and 5LO at $V_{o,\,TX}$

OB Noise, Passband Roll-off, and Harmonic Emission

The BB resistor R_{BT} plays a key role in balancing the performances in terms of signal BW, voltage gain, OB linearity, and OB noise. Intuitively, any resistors coupled with the N-path SC gain loop will degrade the Q of the passband responses at $V_{i,\,TX}$ and $V_{o,\,TX}$. As plotted in Fig. 12a, a large R_{BT} improves the OB rejection but at the expense of a gain drop in the passband due to the finite input impedance at $V_{i,\,TX}$. Simulated at 2 GHz, with R_{BT} ranging from 100 to 800 Ω, the OB rejection increases but induces a 4-dB gain drop, whereas the −1-dB BW decreases from 24 to 8 MHz. The output noise at $V_{o,\,TX}$ drops from 1.04 to 0.33 aV^2/Hz at 80-MHz offset owing to the increased rejection from 7.3 to 19.3 dB (Fig. 12b). In fact, as R_{BT} generates noise

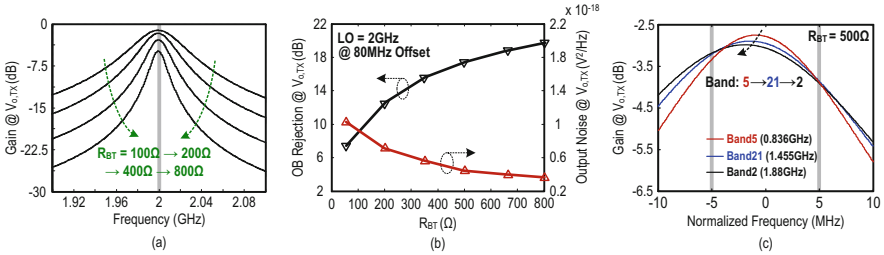

Fig. 12 (**a**) R_{BT} should balance the signal BW, OB rejection, and noise. (**b**) The output OB noise reduces with increased OB rejection but it will saturate as a large R_{BT} induces noise itself. (**c**) When RF frequency increases from 0.836 to 1.88 GHz, passband frequency shifting increases from 0.9 to 1.9 MHz while the gain droop decreases from 1.1 to 0.8 dB

itself, the rejection of OB noise will saturate eventually if raising only R_{BT}. Here, the TX mode chooses a 500-Ω R_{BT} to reach 17.1-dB OB rejection and 0.42-aV^2/Hz output noise at $V_{o,\,TX}$. From SpectreRF simulations (pss + pnoise), the OB noise at $V_{RF,\,TX}$ is −157.7 dBm/Hz at 80-MHz offset, where the main contributors are R_{BT} (24%), G_{mRF} (20%), $SW_{L,\,R}$ + LO divide-by-4 circuitry (20%), and PAD (10%). The rest arises from the off-chip 50-Ω load and switches $SW_{TX\,-\,RX}$ for the TX-RX-mode control.

Mainly due to the input capacitor of G_{mRF}, the simulated passband frequency shifting is within 0.9–1.9 MHz when the RF frequency covers the range between 0.836 GHz (band5) and 1.88 GHz (band2) (Fig. 12c), with 1.1-dB passband roll-off at band5 and 0.8 dB at Band2 for LTE10. The impact of such roll-off characteristics on the EVM performance should be insignificant, since the EVM of an LTE signal is the RMS value of each resource block (RB)'s EVM and the BW (180 kHz) of each RB is much smaller than the signal BW (9 MHz for LTE10) [12]. To address this roll-off issue, we can apply a preemphasis digital equalizer to compensate the passband roll-off for the TX mode, similar to the post-emphasis equalizer used in the RX path [13]. In the digital baseband, the compensation of different passband roll-offs (0.3 dB range) according to the RF frequency is feasible at the cost of small area and power. In addition, the preemphasis digital equalizer can be an option to compensate the sharp roll-off region of the analog filter for [8], although without passband frequency shifting.

For the spectral purity, $V_{o,\,TX}$ contains typical LO harmonic emission with a third-order harmonic rejection ratio (HRR_3) of 9.5 dB for $N = 4$. Nevertheless, with the limited BW of the PAD and output bonding wire, the HRR_3 at the TX output $V_{RF,\,TX}$ improves (Fig. 13), going up with frequency (e.g., 23 dB at 2 GHz). In addition, the single-ended PAD operating in class AB mode dominates the second-order harmonic distortion (HD_2) at $V_{RF,\,TX}$. In fact, by properly matching the PAD's push-pull transistors, HD_2 can be <-37 dBc at a 0-dBm P_{out} from simulations (Fig. 13). Harmonic rejection N-path filtering [14] can be an option to further improve the harmonic emission. In practice, an off-chip PA loads the output of the PAD. For LTE applications, the commercial high-power PA (e.g., [15]) is narrowband and will

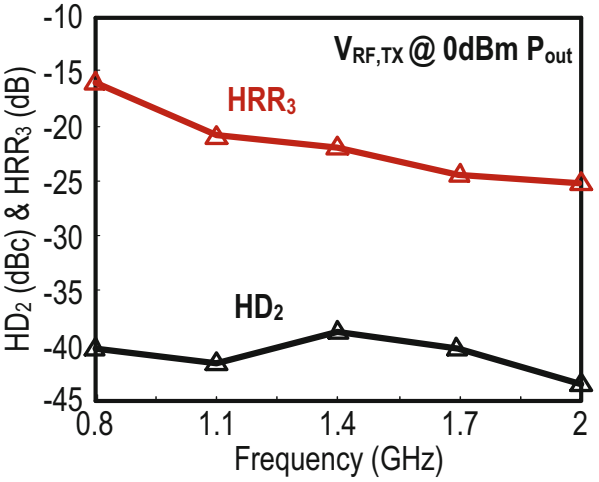

Fig. 13 Simulated OB harmonics (HD2 and HRR3) at $V_{RF,\ TX}$ versus operating frequency

suppress all OB harmonics from its TX. Thus, the PA harmonic distortion still dominates the spectrum clearance at the final output. Finally, we use a single-pole multi-throw switch for the multiband TX to interface with different PAs.

Other Implementation Details

To enhance the power efficiency and avoid any internal gain nodes, we choose G_{mRF} as an inverter-based amplifier self-biased by a feedback resistor R_F. The nonoverlap LO_1 - LO_4 (25% duty cycle) prevents the I/Q cross talk from degrading the linearity. The capacitor C_{BT} essentially operates as a charge buffer at the BB side to relieve the gain drop at the RF side, due to the input capacitance of G_{mRF}. By switching $SW_{L,\ R}$, the circuit will up-sample the filtered BB voltages to $V_{i,\ TX}$ in sequence, thus seeing a high input impedance of G_{mRF} and allowing good linearity. In order to decouple the signal-handing ability of G_{mRF} to the overall TX output power, we further amplify the RF signal at $V_{o,\ TX}$ by the wideband single-ended PAD before outputting $V_{RF,\ TX}$. The PAD, based on a push-pull cascode structure ($M_{1\ -\ 2}$), contains the cascode transistors ($M_{3\ -\ 4}$) self-biased by a feedback resistor (Fig. 2). From the simulations, the class AB PAD achieves a −1-dB output BW of ~2.1 GHz, which is adequate to cover >80% of the LTE-TDD/FDD bands from 0.7 to 2 GHz. With the PAD single-ended, a 2.5-V supply allows better HD_3 (−43.4 dBc) and voltage gain (9.3 dB) while showing a 12.2% drain efficiency at a 0-dBm single-tone Pout. Both HD_3 (−37 dBc) and voltage gain (5.7 dB) will degrade with a 1.2-V supply applied and the cascode transistors removed.

As a reconfigurable TXR, the TX-RX-mode switches $SW_{TX\ -\ RX}$ (Fig. 2) are critical and require careful sizing to minimize the parasitic effects, especially for the PAD that has an input capacitance of ~500 fF. With the PAD powered-down, we set