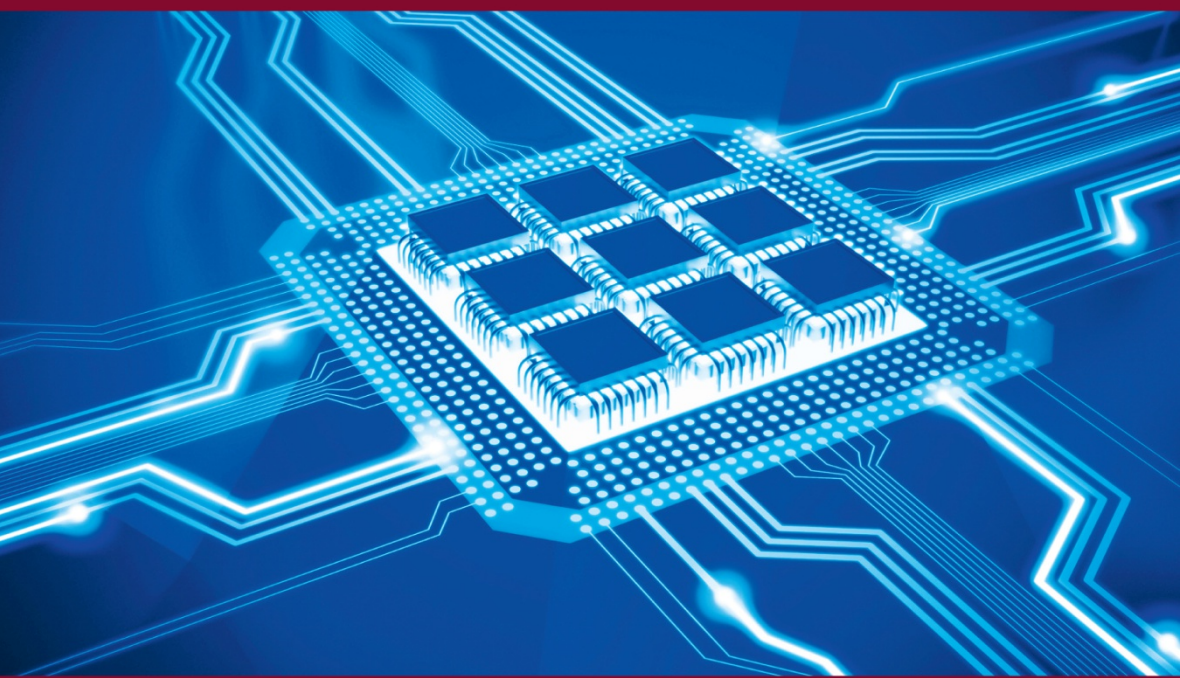
ENERGY SERIES

Smart Power Integration

Mohamed Abouelatta
Ahmed Shaker
Christian Gontrand



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Contents

Preface ix

Chapter 1. Overview of Smart Power Integration 1

1.1. Introduction. 1
1.2. Smart PIC applications 2
1.2.1. Flat panel displays 4
1.2.2. Computer power supplies and disk drivers 4
1.2.3. Variable speed motor drives 4
1.2.4. Factory automation 4
1.2.5. Telecommunications 5
1.2.6. Appliance controls 5
1.2.7. Consumer electronics 5
1.2.8. Lighting controls 5
1.2.9. Smart homes 6
1.2.10. Aircraft electronics (Avionics) 6
1.2.11. Automotive electronics. 6
1.3. Historical view of the MOS power devices 6
1.4. Smart PIC fabrication processes 9
1.4.1. Dedicated processes 9
1.4.2. Compatible processes 10
1.5. Insulation techniques 10
1.5.1. Self-insulation 10
1.5.2. Dielectric insulation 11
1.5.3. Junction insulation 11
1.5.4. Advanced junction insulation techniques 12
1.6. Motivation of the book 13

Chapter 2. Modular or Hybrid Integration 17

2.1. Introduction 17
2.2. IGBT technology evolution 18
2.2.1. IGBT presentation 18
2.2.2. Epitaxial structure with buffer layer and reduction of carrier lifetime 30
2.2.3. Homogeneous structure with control of load injection 36
2.2.4. Silicon direct bonding-IGBT 38
2.2.5. IGBT trench 39
2.2.6. Lateral IGBT 39
2.3. Assembly technology 40
2.4. Thermal aspect 41
2.4.1. Thermal impedance. 43
2.5. Applications fields. 45
2.5.1. IGBT power modules for electric traction applications 45
2.5.2. IPM for low- and medium-power applications. 48

Chapter 3. Monolithic Integration 51

3.1. Functional integration and smart power 51
3.2. Transition from low-voltage technology (CMOS) to high voltage . . . 52
3.2.1. Introduction 52
3.2.2. A typical CMOS technology 62
3.2.3. Breakdown voltage of a microelectronics structure 63
3.2.4. Improved junctions breakdown by guard techniques 68
3.2.5. Improvement using electrical insulation techniques 73
3.2.6. Review of the main MOS devices for high-voltage integrated circuits 75
3.3. Combining analog and digital (mixed) 82
3.3.1. Analog: basic functional blocks in CMOS technology and basic analog structures. 82
3.3.2. Reminder on the general structure of the operational amplifier . . . 88
3.3.3. Digital 96
3.3.4. The notion of codesign. 96
3.3.5. Assessment 99

Chapter 4. Technology for Simulating Power Integrated Systems . . 101

4.1. Introduction. 101
4.2. Hardware and software design of engine control. 102
4.2.1. Functional specification 105

4.2.2. Exploring the space of solutions: the partitioned specification model . . . 106
4.2.3. Mixed synthesis, hardware and software code . . . 107
4.2.4. Model functional testing . . . 110
4.2.5. Synthesis of the approach and related tools of the functional model . . . 111
4.3. Proposed design stream: related tools . . . 112
4.3.1. Accuracy . . . 113
4.3.2. Resources and system architecture . . . 113
4.3.3. Realization . . . 120
4.4. Conclusion . . . 123

Chapter 5. 3D Electrothermal Integration . . . 125

5.1. Introduction . . . 125
5.2. Electrothermal modeling of substrate . . . 126
5.2.1. Brief introduction to mathematical tools . . . 127
5.2.2. Simulation results by using Green/TLM . . . 132
5.2.3. Thermal management in a 3D-integrated figure . . . 146
5.2.4. Thermo-mechanical design . . . 156
5.2.5. Thermal modeling of the connectors . . . 157
5.3. Heat analysis for 3D ICs . . . 157
5.3.1. 3D IC heat transfer compact model without TSVs . . . 157
5.3.2. IC model for analyzing the temperature of the chip of the top layer taking into account the TSVs . . . 159
5.3.3. 3D IC thermal modeling result . . . 161
5.3.4. Electrothermal (ET) modeling of very large scale circuits . . . 166
5.3.5. Electrical modeling of very large scale . . . 167
5.3.6. Thermal modeling of very large scale circuits . . . 170
5.3.7. Electrothermal modeling of very large scale circuits . . . 171
5.4. Conclusion . . . 184
5.5. Heat pipe . . . 185
5.6. Conclusion . . . 203

Chapter 6. Substrate Coupling in Smart Power Integration . . . 205

6.1. Introduction . . . 205
6.2. Part I: smart power integration using the DTI technique . . . 205
6.2.1 DTI technology . . . 205
6.2.2 DTI structure . . . 206
6.2.3. LDMOSFET performance with DTI . . . 207

6.2.4. Parasitic suppression in 2D smart power ICs with deep trench . . . 211
6.2.5. HV dynamic signal impact on CMOS devices 215
6.2.6. Mixed-mode CMOS-substrate coupling simulation 227
6.3. Part II: smart power integration using stacked 3D technology 232
6.3.1. From 2D planar integration to 3D integration 232
6.3.2. 3D smart power integration 234
6.3.3. TSV-CMOS mixed-mode coupling 253
6.3.4. Electromagnetic impact of TSV in RF range 264

Conclusion 271

Appendix: Semiconductor Physical Models 275

References 299

Index 301

Preface

Smart integration is a process in which an existing system infrastructure is upgraded through the integration of multiple technologies, for example, automated sensors, advanced automated controls and forecasting systems. A smart grid allows for interaction between the consumers and enables optimal use of energy and communication systems based on price preferences and system technical stresses, without forgetting the environmental aspect.

The continuous reduction in dimensions and the need for increasingly high power density have highlighted the need for ever more efficient structures. Smart power technology has been developed to meet this demand. This technology makes specific use of (L)DMOS devices, offering new solutions because of its unique high voltage and high current characteristics. The operation of these devices is accompanied by a number of phenomena. Good modeling makes it possible to account for these phenomena and predict the physical behavior of the transistor prior to production. To this, we add an axis that has become unavoidable: the entanglement between devices, circuits, connections and substrates.

(Micro)grid designs have evolved significantly in recent years with the incorporation of information and communication technology (ICT) solutions, such as artificial intelligence (AI) and machine learning (ML). A smart microgrid, equipped with sensors and automation controls, can efficiently perform load profiling and forecasting, generation management, load prioritization, etc. A go-to example is the vehicles that are quickly becoming a center of communication, navigation and connectivity. Automotive solutions will integrate with smart city infrastructures, personal devices and in-vehicle services to become part of a connected whole.

This book introduces different domains and tools and allows the reader to develop their understanding of smart power systems through real studies. Knowledge of high school mathematics is sufficient to progress through these studies.

Mohamed Abdelhamid Abouelatta
Ahmed Shaker Ahmed Zaki Ghazala
Christian Gontrand
January 2021

1

Overview of Smart Power Integration

1.1. Introduction

Since 1965, integrated circuit (IC) technology has followed Moore's law which states that the number of integrated devices doubles every 18 months. This growth is partly due to an increase in the size of ICs that can be produced. However, the dominant effect is due to the reduction in feature size of component devices that are integrated. The reduction of feature size tends to bring advantages of increased speed and the possibility to operate at lower voltages, allowing reduced power consumption. These advantages make technology shrinkage very attractive for technical performance reasons, as well as cost.

However, there are many applications where voltage cannot be reduced for external reasons. There are three areas where this is the case: power electronics, automotive applications and wide dynamic range circuits. In such applications, system integration of high voltage, analog and digital circuitry on a single IC is attractive in order to gain advantage in terms of miniaturization, reliability, efficiency and cost. However, in order to make these gains, the conflict of reducing voltage due to technology feature size has to be resolved with the requirements for operation at continued relatively high voltage.

The different operation and interface requirements of high voltage, analog and digital require a technology development optimized for these system requirements. Different technologies have been developed to address these applications, such as smart power and various bipolar-CMOS-DMOS (BCD) processes.

Smart power integrated circuits (PICs) that monolithically integrate low-loss power devices and control circuitry have attracted much attention across a wide range of applications. These ICs improve system reliability, reduce volume and weight and increase overall efficiency. Considerable effort has been put into the development of

Smart Power Integration,
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smart power devices for automotive electronics, peripheral computer appliances and portable equipment, such as cell phones, video cameras, and so on.

Commonly used smart power devices are the lateral double diffused MOS Field Effect Transistor (LDMOSFETs) and lateral insulated gate bipolar transistors (LIGBTs) implemented in bulk silicon or silicon on insulator (SOI). The main challenges in the development of these devices are obtaining the best trade-off between specific ON-resistance $R_{ON,SP}$ (R_{ON} × area) and breakdown voltage (BV), and shrinking feature size without degrading device characteristics.

1.2. Smart PIC applications

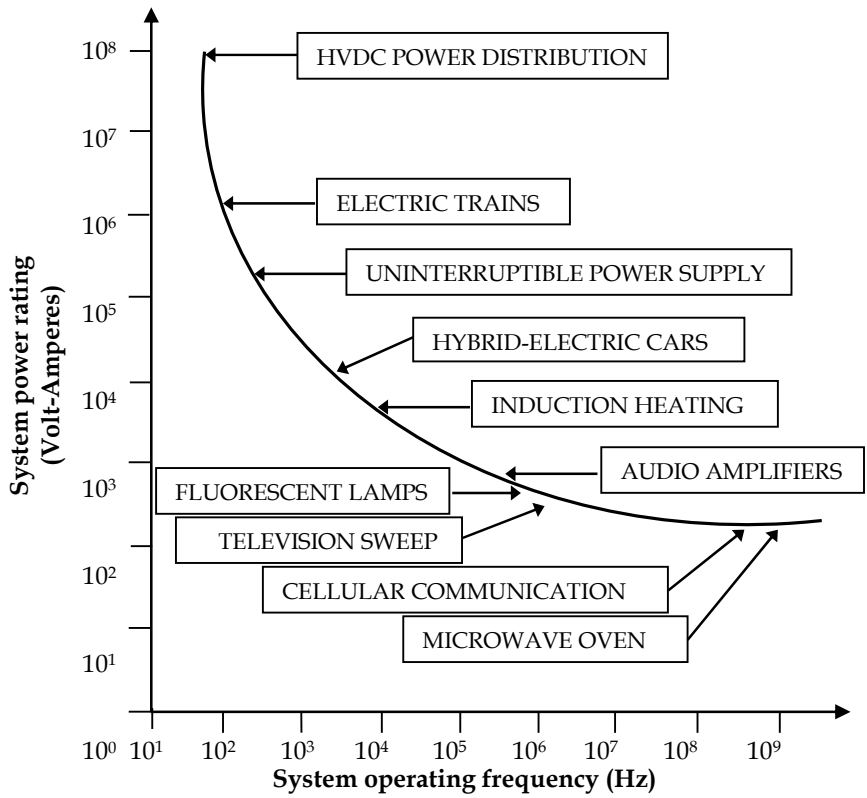

Figure 1.1. *Applications of power devices*

Smart PIC technology is expected to have an impact in all areas in which discrete power semiconductor devices are currently being used. It is anticipated that this technology will open up new applications based upon the added features of smart controls. In Figure 1.1, applications of power devices are shown as a function of operating frequency. Another classification approach of these applications involves current and voltage handling requirements, as shown in Figure 1.2. Some of these applications are listed in the following subsections.

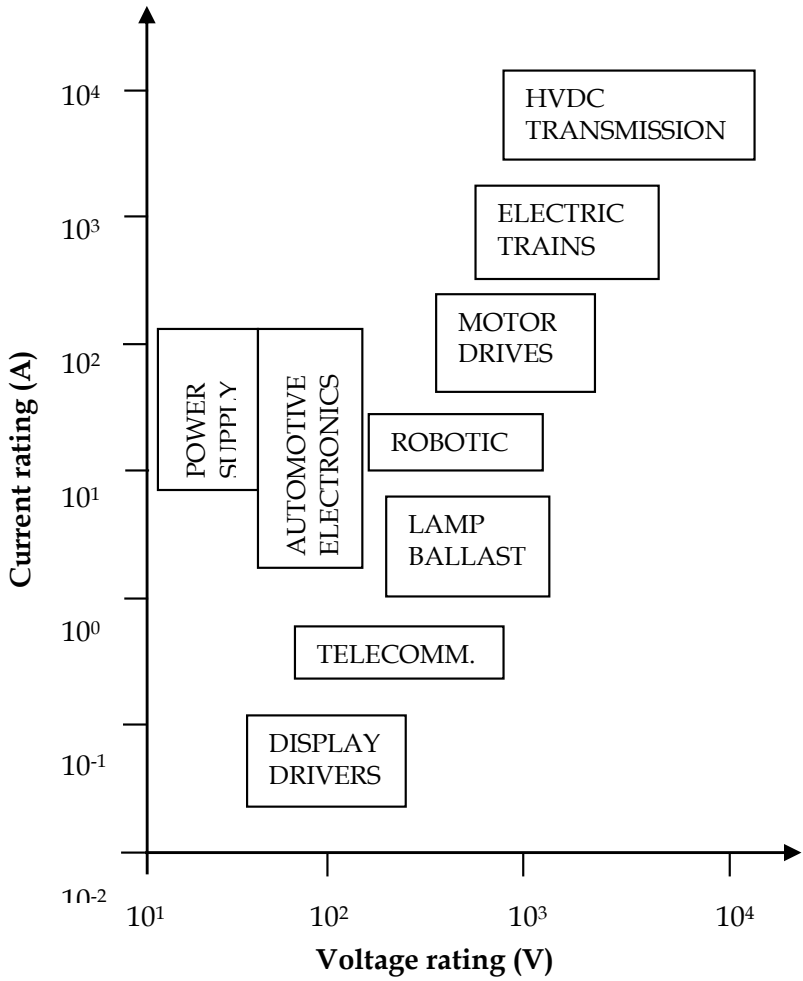

Figure 1.2. *System ratings of power devices*

1.2.1. *Flat panel displays*

The popularity of portable electronic products such as cell phones and notebook computers has generated significant demand for flat panel displays. These displays are usually liquid crystal displays (LCD) or electro-luminescence (EL) panels arranged in a matrix with large number of column and row drivers (e.g. 640 × 480 for VGA resolution). Although the required voltage may be high, the current level is low (usually in the mA range). Smart PICs with as many as 80 output channels have been fabricated on a monolithic chip.

1.2.2. *Computer power supplies and disk drivers*

Computer systems are developing continuously in terms of speed and processing capabilities. This is made possible by using higher density Very Large-Scale Integration (VLSI) technology. However, the increased power requirement has resulted in an increase in the physical size of the power supply. In 1976, the CPU board and power supply each represented one-third of the total physical volume of a computer system. By the 1990s, the power supply had grown to 50% of the physical volume while the CPU board had shrunk to about 20%. To reverse this trend, it is necessary to develop smart PIC technology to improve the density and hence the volume of the power supplies.

1.2.3. *Variable speed motor drives*

Variable-speed motor drives are being developed to reduce power loss in all applications. The improvement in performance requires smart power technology that can operate at relatively high frequencies with low power losses. This translates to a low ON-state voltage drop at high current levels, fast switching speed and rugged operation. For smart PIC implementation, additional consideration, such as level shifting to and from high voltages, over-temperature, over-current, over-voltage and short-circuit protection are more critical.

1.2.4. *Factory automation*

Advanced numerical control and robotic systems require efficient smart PIC technology to create a distributed power control network under the management of a central computer. The smart PICs for this application must be capable of providing AC or DC power to various loads, such as motors, solenoids, arc welders, and so on. They are also required to perform diagnostic, protection and feedback functions.

1.2.5. *Telecommunications*

One of the high-volume markets for smart power technology is in telecommunications. The technology required for these applications must be capable of integrating multiple high-voltage, high-current devices on a single chip. At present, this has been achieved using MOS devices fabricated using dielectric insulation. Improvements are required to reduce the cost of the dielectric insulation fabrication process. Ongoing development on direct wafer bonding has been promising in terms of providing a cost-effective process.

1.2.6. *Appliance controls*

The main benefit of using smart PICs in appliance control is to provide improvements in performance and efficiency. Onboard sensors can also provide more precise controls (e.g. temperature settings). Simple domestic appliances, such as toasters, washing machines and irons, are appearing with smart PICs for this reason.

1.2.7. *Consumer electronics*

Smart PICs are required for a large variety of entertainment systems such as CD players, tape recorders, VCRs, etc. For example, a monolithic motor control IC that regulates the speed of the motor, while minimizing power losses, is essential to all battery-operated consumer entertainment systems. Development of improved lateral power devices with greater power density is necessary to increase the efficiency of this technology.

1.2.8. *Lighting controls*

Traditional fluorescent lights use a mechanical ballast (transformer) for start-up. The electrical characteristics of fluorescent lights vary drastically from start-up to normal operation. In order to improve the efficiency and overall lifetime of a lighting system, more precise control is needed. The cost of electronic fluorescent light ballasts implemented using smart PICs can easily be justified by the resulting savings in energy and maintenance. In addition, incorporating smart PIC technology enables lighting to be controlled by a central computer, further enhancing energy savings in commercial buildings.

1.2.9. *Smart homes*

The concept of smart homes is attracting increased attention as a result of advances in smart power technology that are driving down the cost of the control module. A smart home system requires the development of a multiplexed network with smart power modules to control loads such as ovens, furnaces, air conditioners, lights and small appliances.

1.2.10. *Aircraft electronics (Avionics)*

The concept of fly-by-wire, where the hydraulic actuators in an aircraft are replaced by electromechanical actuators, is gaining acceptance among manufacturers. Success in development will depend on the availability of smart PIC technology to perform the control that is small in both size and weight. The power switches must be extremely reliable and capable of operating at high voltage and current levels with low ON-state voltage drop. In this regard, MOS-gated devices are essential for compact PICs.

1.2.11. *Automotive electronics*

One of the biggest anticipated markets for smart PICs is automotive electronics. Between the 1960s and 1970s, there was a slow uptake of discrete devices and analog ICs for automotive applications. In the 1980s, digital ICs and microprocessors were incorporated. In the 1990s, smart PICs were already being used to create a multiplexed control network in cars to reduce the size and weight of the wiring harness. The smart PIC modules control loads such as lights and motors, while providing protection functions. This has greatly enhanced fault management and diagnostic capability.

1.3. Historical view of the MOS power devices

The basic operation of the MOSFET involves the formation of a conductive channel at the surface of the semiconductor, below an insulator, by the application of a voltage to a gate electrode. The first MOSFET structure reported in 1960 was not designed to support high voltages or handle high-current levels and, furthermore, thin metal electrodes were used that had poor current-handling capability.

In the 1970s, it was recognized that the vertical architecture is required to handle high voltages and currents to produce a power device. The vertical structure enables the use of thick source and drain electrodes. The first power MOSFET structure was fabricated using a V-groove process, as shown in Figure 1.3.

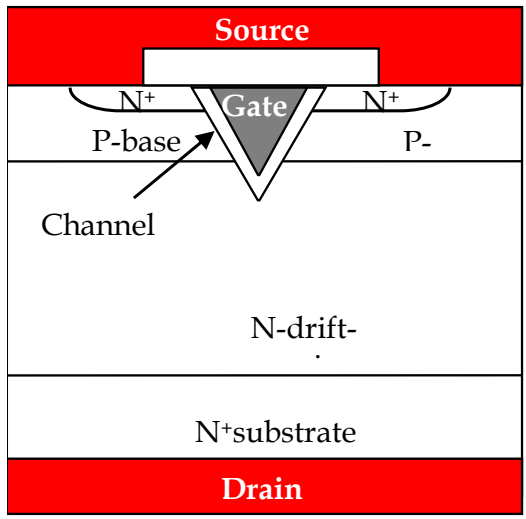

Figure 1.3. *V-groove MOSFET structure. For a color version of this figure, see www.iste.co.uk/abouelatta/smartpower.zip*

The V-MOSFET structure fell out of favor because of manufacturing difficulties. In addition, the sharp corner at the bottom of the V-groove was found to degrade the breakdown voltage.

The first commercial power MOSFET was the vertical diffused (VD) MOSFET of the mid 1970s, which is illustrated in Figure 1.4.

The non-uniform current distribution enhances its resistance (JFET region), making the internal resistance of the VD-MOSFET structure larger than the ideal specific ON-resistance of the drift region. The large internal resistance of the VD-MOSFET structure provided motivation for the development of the trench-gate power structure in the 1990s.

Moreover, the U-MOSFET is shown in Figure 1.5. There is no JFET region in the structure, enabling a reduction in internal resistance when compared to the VD-MOSFET structure.

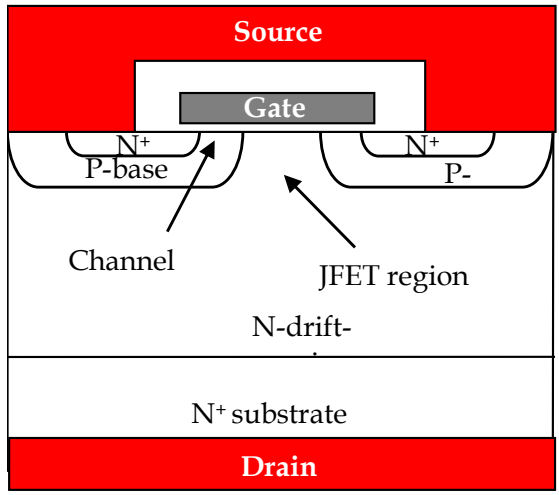

Figure 1.4. *VD-MOSFET structure. For a color version of this figure, see www.iste.co.uk/abouelatta/smartpower.zip*

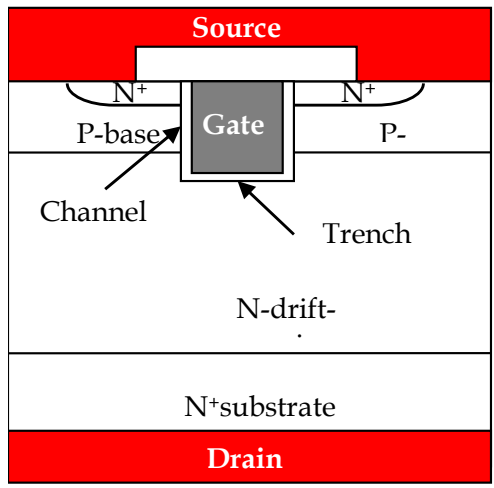

Figure 1.5. *U-MOSFET structure. For a color version of this figure, see www.iste.co.uk/abouelatta/smartpower.zip*

One significant drawback of the vertical devices is the fact that it is difficult to include multiple power devices on the same monolithic chip. The lateral structure allows all terminals to be accessed from the top surface of the chip. The current

flows laterally from the drain along the surface through the MOS channel and up into the source, hence the name LDMOSFET, as shown in Figure 1.6.

LDMOSFET generally suffers from a higher specific ON-resistance due to the longer current path. Furthermore, the blocking voltage of the LDMOSFET depends critically on the curvature of the P-body to the N-drift region junction. In order to obtain high blocking voltage, it is necessary to use a low doping concentration in the N-drift region. However, this directly contradicts the low specific ON-resistance requirement. Therefore, it must be optimized to achieve high breakdown voltage with low $R_{ON,SP.}$

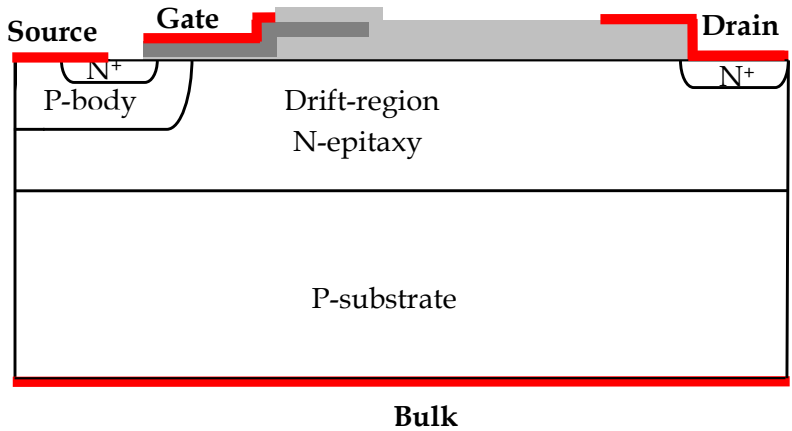

Figure 1.6. *LDMOSFET structure. For a color version of this figure, see www.iste.co.uk/abouelatta/smartpower.zip*

1.4. Smart PIC fabrication processes

Smart PIC fabrication processes are classified into two categories: dedicated processes and compatible processes.

1.4.1. *Dedicated processes*

A dedicated smart PIC technology refers to a fabrication process with the optimization of the power devices as the highest priority. The performance of the low-voltage CMOS devices is usually compromised. S.G.S. Thomson is a long time advocate of such a trend with their family of BCD processes.

1.4.2. *Compatible processes*

The compatible approach is to integrate the power devices into an existing process. While this would invariably lead to a greater degree of compromise in the performance of the power devices, it is a significantly more cost-effective approach. The goal would be to minimize the number of additional steps that have to be introduced to the original process. This will ensure low production costs since most existing processes are already fine-tuned and are running at high volume.

The blocking voltage and specific ON-resistance ratings can be optimized by selecting the appropriate doping profiles. The compatible approach is currently being adopted by many manufacturers for their existing CMOS processes, especially for out-dated processes. Since most of the production volume is being migrated to more advanced processes (e.g. BiCMOS processes), in order to maintain the existing process lines, new applications have to be found. Smart PIC technology is the ideal way to inject new life into these soon to be obsolete processes.

1.5. Insulation techniques

In PIC technology, power transistors are controlled by low-voltage BiCMOS circuitry. Insulation between these two types of components – i.e. high power devices and control/logic circuitry – is necessary in order to avoid crosstalk and ensure systems operate as they should.

Under certain conditions, a negative bias can be applied on the drain contact with respect to the substrate of laterally diffused MOS (LDMOS), as a result of the switching of an inductive load. If the technology employs junction insulation, this may lead to an unwanted injection of minority charge carriers into the substrate. The resulting currents may cause the entire PIC device to malfunction. Minority carriers injected into the substrate can cause signal disturbances in the low power circuitry or latch-up in the CMOS structures.

Several insulation techniques have been employed in order to protect the low-voltage CMOS circuitry from substrate currents that originate from power transistors.

1.5.1. *Self-insulation*

Self-insulation is characterized by a very simple process flow; it is based on the CMOS process but includes a few additional steps. However, as all devices in the same chip have to share the positive supply voltage, additional parasites are introduced. Siemens smart SIPMOS technology is an example of this.

1.5.2. *Dielectric insulation*

SOI insulation, where active devices are completely surrounded by a non-conducting dielectric layer, is shown in Figure 1.7. This technology provides excellent insulation; however, since the dielectric is a poor thermal conductor, this may lead to serious thermal problems for the power devices. Additionally, the cost of producing SOI wafers is significantly higher than it is for conventional silicon wafers.

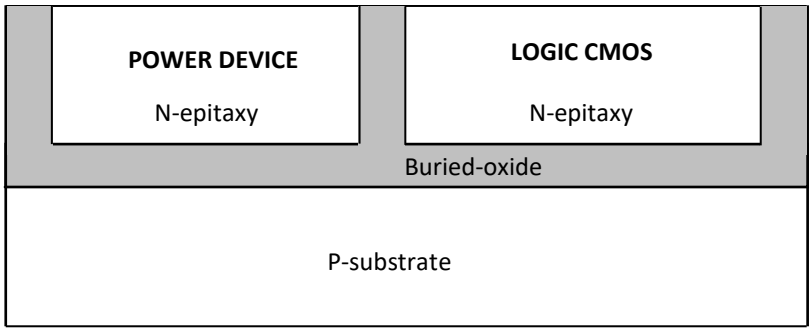

Figure 1.7. *Dielectric insulation*

1.5.3. *Junction insulation*

Junction insulation (JI) does not suffer from such serious self-heating problems, but the electrical insulation is much poorer. Standard junction insulation structures consist of a reversed biased P-N junction, as shown in Figure 1.8.

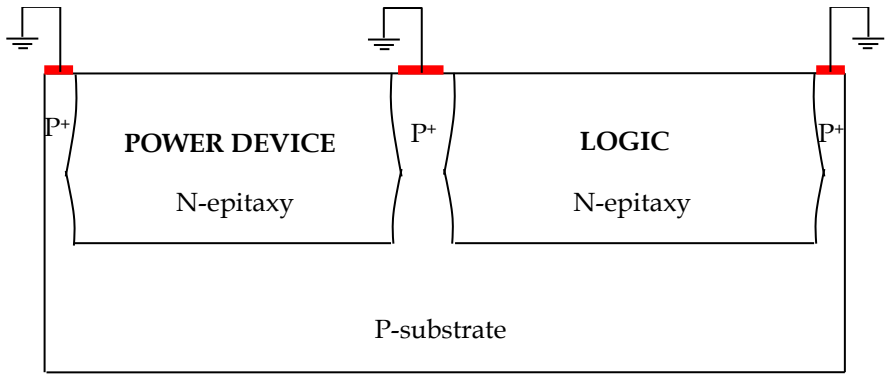

Figure 1.8. *Standard junction insulation*

1.5.4. *Advanced junction insulation techniques*

To enhance the performance of junction insulation structures, advanced techniques are used.

1.5.4.1. *Passive JI*

In order to make the insulation more effective, an extra N-region is added and enclosed by two deep P-diffusions. The N-region is permanently tied to the highest potential of the circuit, as shown in Figure 1.9. Its purpose is to remove the minority carriers as close to their point of injection as possible.

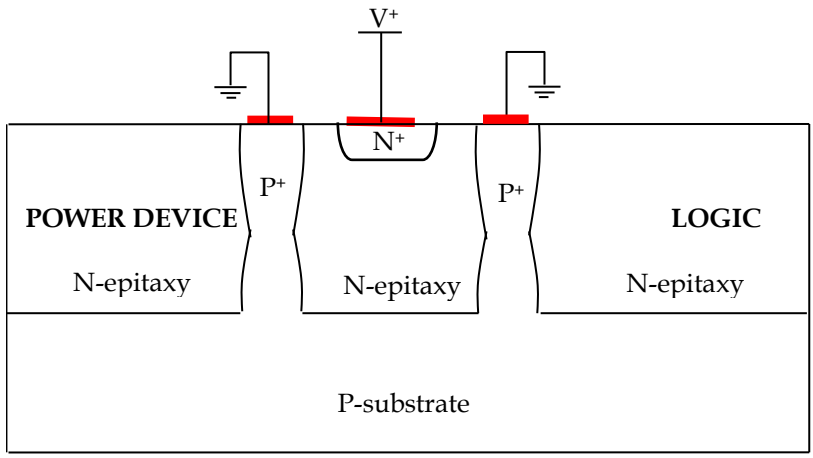

Figure 1.9. *Passive junction insulation*

1.5.4.2. *Active JI*

A significant step forward has been made by introducing the multi-ring active analogic protection (MAAP) JI, as shown in Figure 1.10. This self-triggered JI technique is able to reduce the current that reaches the low power circuitry by up to several orders of magnitude compared with the passive JI.

In the MAAP device, ND and P2 are shorted and left floating, as shown in Figure 1.10. This time, the on-chip metallization is implemented on the chip instead of on external wiring to reduce the interconnect resistance R_{via}.

Once injected from the drain side, electrons flow through the substrate and some are collected by ND, reducing the ND's potential. This negative potential is now transferred through the metallization to P2, which adds to its built-in potential. P2 is

now on lower potential than P1 and the resulting electric field will reject the substrate minority carriers injected from the drain of the power device.

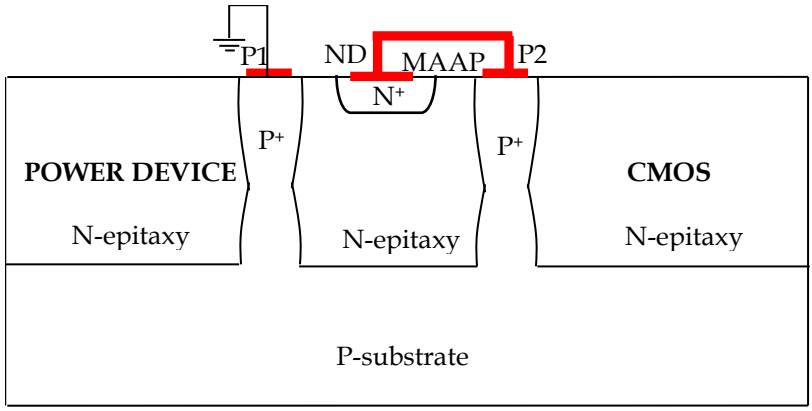

Figure 1.10. *Active junction insulation*

1.5.4.3. *Active pull-down protection*

Active pull-down protection combines junction insulation with a bipolar transistor that biases a P-substrate contact according to the injected current level. This insulation structure is highly effective, but its complexity and number of variables may lead to a significant increase in the number of iterations at the design stage.

1.5.4.4. *Multiple structures*

In an attempt to further improve the blocking capabilities of junction insulation, the use of multiple or combined structures has been investigated, keeping the surface area of the insulation device as small as it is for the single structures. This means that the width of the P and N diffusion zones is decreased in order to retain the same total area.

1.6. Motivation of the book

Smart PICs that monolithically integrate low-loss power devices and control circuitry have attracted much attention across a wide range of applications. These ICs improve system reliability, reduce volume and weight and increase efficiency. Considerable effort has been put into the development of smart power devices for automotive electronics, peripheral computer appliances and portable equipment, etc.

Commonly used smart power devices are the lateral double diffused MOS transistors (LDMOSFETs). The main challenges in the development of these devices are obtaining the best trade-off between specific ON-resistance $R_{ON,SP}$ and breakdown voltage BV, and shrinking the feature size without degrading device characteristics. A lot of work has been done on both characterization and modeling of LDMOSFETs in the literature starting from the late 1970s. Still, there is some confusion concerning the origin of special phenomena such as, quasi-saturation and explanation of the capacitive behavior of the HV device as a function of the biasing conditions. Unfortunately, this matter was not treated in a thorough manner, as most of the time only a few characteristics that do not cover the entire voltage domain were presented.

Device simulation with technology computer-aided design (TCAD) tools has been proven to play an important role for design engineers and researchers in analyzing, characterizing and developing new devices. It saves time and lowers the cost of design when compared to the experimental approach. In addition, it allows physical effects to be seen clearly in the semiconductor devices of new device concepts. Therefore, a clear understanding of TCAD tools in the analysis of power semiconductors is essential in order to obtain accurate and reliable simulation results.

This book deals with novel power semiconductor concepts for smart power applications. New device structures are suggested and studied to improve the device characteristics related to traditional power devices. Two- and three-dimensional device simulations are performed to study new device concepts. These new structures are implemented in 0.35 µm BiCMOS technology.

An important motivation point is the planar integration of HV LDMOSFETs with low-voltage CMOS devices. A new electrical insulation scheme between the power devices, as well as between the power devices and low-voltage CMOS devices is suggested, using a deep trench to reduce the insulation distance among the high-voltage devices considerably, and hence to reduce the total chip area drastically compared to technologies with a standard junction insulation scheme.

In recent years, an emerging technology was the three-dimensional (3D) integration. This technology uses through-silicon vias (TSVs) and re-distribution layers (RDLs) to interconnect multiple active circuit layers. 3D integration offers significant improvements over two-dimensional (2D) ICs on performance, functionality and integration density, and promises a solution to the so-called “wiring crisis” problem. Furthermore, 3D integration also provides new architectures for sophisticated ICs and facilitates the integration of heterogeneous materials and devices. The important motivation question is: can this 3D technology be used for the implementation of smart PICs?

In this work, ISE and SENTAURUS-TCAD tools, general purpose device simulators, are used for the simulation of established and newly proposed power semiconductor devices and integration schemes.

From a modeling point of view, two model types are presented in the literature. Several attempts were made to build compact models for the HV devices. Some authors focus on the construction of the intrinsic MOS model and treat the drift part as a trivial extension. Others focus on the modeling of the drift part only. To fulfill this target, very simple expressions are needed for both the drift and intrinsic MOS parts. Most of the time, this results in poor accuracy when compared with real device characteristics. In the second category are the macro-models that are built by merging several spice elementary devices in a subcircuit and using the result as a black box for the transistor model. The proposed LDMOS devices are used to construct an interface circuit to convert the low-level logic voltage to high-level voltage.

The upheavals of the electronics of power will come from the capacity of the component makers to propose silicon devices (in the future, other materials that can withstand the high temperature, such as silicon carbide and gallium arsenide, will be added), integrating a system and a function. The integration of power was born from the desire to increase the reliability of the systems, and simplify their assembly and maintenance, while also reducing the cost. The progress of the electronics in the coming years will be focused primarily on the projections of the integration of power. According to the power to be commutated, today, the integration of power can be classified in two dies: monolithic integration and hybrid integration.

In practice, we want the readers to be aware of the various fields and bricks of the integration of power, which is essentially multi-field and whose main concept is the approach system.

2

Modular or Hybrid Integration

2.1. Introduction

In this chapter, we develop projections of the power modules (switch of high power) containing insulated gate bipolar transistors (IGBTs) of intelligent power modules (IPMs) and application-specific intelligent power modules (ASIPMs), as well as fully customized hybrid solutions.

Over the last few years, the range of power modules has expanded. Of note are the advanced IGBT modules that compete with the gate turn-off thyristors (GTOs), invented by General Electric. Unlike conventional thyristors, GTOs are fully controllable switches that can be turned on and off by their third lead: the gate electrode. The development of non-punch through (NPT) technology, IGBTs and the massive parallelization of chips (up to more than 20) makes it possible to lay out modules in the range of 5 KV and 5 kA. These ranges of power make it possible to consider applications for electric traction.

Unfortunately, traditional solutions (with bonding) do not support thermal fatigue induced in such applications. Research is directed toward cases pressed for the best held with thermal fatigue, a better dissipation of the heat and an increased facility of assembly. Work on the cases has led to economic solutions that have a profit in facility of assembly and reliability. In parallel, manufacturers are endeavoring to improve hybrid modules by reducing internal inductances, thermal resistance, volume and weight. This will require materials with better properties (dielectric insulation, thermal conductivity, etc.). Some examples include replacing the traditional aluminum base plate with a metal matrix composite (MMC) such as Al/SiC, replacing the alumina Al_2O_3 substrate with aluminum nitride (AlN) or diamond and integrating the radiator (which becomes the base plate) or microphone-coolers. A recently suggested solution is based on the suppression of the dielectric substrate and the placement of a massive dielectric exchanger of AlN,

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on which the copper collector is thermo-compressed. The disadvantage of this encapsulation lies in the high cost of machining the AlN.

IPM modules contain the power stage, the drivers and protect the devices. They can be compared with monolithic smart power solutions, but those relate to a much higher power range (I < 30 A, U < 1200 V). The IPM provides complete solutions for applications such as the inverter. IPM modules are, however, relatively expensive or inflexible devices and depend on the manufacturer (not second source manufacturers). The hybrid circuits give a profit in clutter, maintenance, confidentiality, etc. One considers several technologies according to the range of power: PCB (Printed Circuit Board – printed circuit board with components assembled on the surface CMS) (750 W), SMI (Metal Isolated Substrate) (4 kW), DCB (Direct Contact Bonding, largely used in IGBT modules) (> 10 kW). The research tasks in this field join those of the modules.

	MOSFET transistor	**Bipolar transistor**
Conduction types	– Majority carriers	– Bipolar (two types of carriers in play)
Advantages	– Speed – Simple control circuit (and for low consumption) – Robustness	– Low-voltage drop for ON-state
Drawbacks	– High-voltage drop in static (low current density for high voltage MOSFETs)	– Control circuit rather complex (and with significant consumption) – Slow in destocking (although fast in switching)
Quality available on the market in discrete device (single chip)	– From 1 to 70 A – From 30 to 1000 V – High current with high voltage	– From 1 to 100 A – From 20 to 1500 V

Table 2.1. *Advantages and disadvantages of the MOSFET and bipolar transistor*

2.2. IGBT technology evolution

2.2.1. *IGBT presentation*

The IGBT was developed as a result to associate, on the same silicon crystal, the speed of the unipolar Metal Oxide Semiconductor Field Effect Transistor