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Enhanced Virtual Prototyping for Heterogeneous Systems

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To Khushboo and Maryam,
Marie,
and
Anna.

Preface

The successful co-design and verification of secure multi-disciplinary heterogeneous *systems-on-chips* (SOCs) with tight interactions between *hardware/software* (HW/SW) systems and their analog physical environment is an increasingly daunting task. In this regard, the emergence of *virtual prototypes* (VPs) at the abstraction of *electronic system level* (ESL) has modernized the design and verification of heterogeneous SOCs. A VP is essentially an executable abstract model of the entire HW platform and pre-dominantly created in C++-based system modeling language SystemC together with *transaction level modeling* (TLM) techniques and its mixed-signal extension SystemC AMS. The much earlier availability as well as the significantly faster simulation speed in comparison to the *register transfer level* (RTL) models and SPICE-level models are among the main benefits of VPs. Thus, virtual prototyping enables HW/SW co-design and verification very early in the design flow. Serving as reference for (early) embedded SW development and HW verification, the functional correctness and security validation of VPs are very important. Hence, a VP is subjected to rigorous functional verification. However, the modern VP-based verification flow still has weaknesses, in particular due to lack of methodologies to capture the complex interactions between digital and analog designs as well as unavailability of security validation techniques. This book proposes several novel approaches that cover varying verification aspects to strongly enhance the modern VP-based verification flow. The chapters of the book are essentially divided into four parts: The first part introduces a new verification perspective for VPs by using *metamorphic testing* (MT) as no reference models/value are needed for verification, unlike in modern VP-based verification flow. The second part enhances the code coverage closure methodologies in modern VP-based verification flow by considering *mutation analysis* and stronger coverage metrics like *data flow* coverage. The third part covers a set of novel, systematic, and lightweight functional coverage-driven verification methodologies to improve the coverage closure. The fourth and final part of the book showcases novel approaches to enable early security validation of VPs. All approaches are presented in detail and

are extensively evaluated with several experiments that clearly demonstrate their effectiveness in strongly enhancing the modern VP-based verification flow.

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Chapter 1
Introduction

Internet-of-Things (IOT) and *5G* (fifth generation technology standard for broadband cellular networks) have enabled a plethora of possibilities which were once unimaginable. While *5G* provides the high-speed connectivity and ubiquitous coverage, it is the smart IOT devices that gather and transport the data that fuel the promise and potential of IOT. These smart devices are a prime example of heterogeneous *System-On-Chips* (SOCs), which comprise two parts: (1) Mixed-Signal *Hardware* (HW) where analog world meets the digital world, (2) and *Software* (SW), the invisible layer that connects us to the physical reality. Heterogeneous SOCs are among the fastest growing market segments in the electronics and semiconductor industry. Driven by growth opportunities in various application domains, many semiconductor vendors are adapting and shifting their focus from separate *Integrated Circuits* (ICs) performing one functionality, toward a more integrated solution of *Radio Frequency* (RF) and high-performance *Analog/Mixed-Signal* (AMS) designs. Due to this industry shift, most SOCs today are heterogeneous containing analog sensors, mixed-signal converters, digital processors running SW on top, and RF transceivers, tightly integrated on a single die. While this shift has resulted in high-performance, efficient, and low-area devices, e.g., Apple M1 SOC [6], it has significantly increased the efforts required to develop and verify these highly complex devices and achieving the required *Time-To-Market* (TTM) simultaneously.

The first challenge in this regard is the HW and SW dependency. Conventionally, HW and SW were developed in isolation and only met each other at the late integration and testing stages. As a consequence, a sequential dependency between HW and SW development phases always existed as shown in Fig. 1.1a. Hence, SW could only be tested properly once the first silicon prototypes of the SOC were available. In particular, HW dependent SW such as device drivers and low-level kernel code could only be written after the silicon design had been completed. One solution to lessen the TTM widely adopted by industry is to move away from complete in-house HW development and instead use larger amounts of pre-

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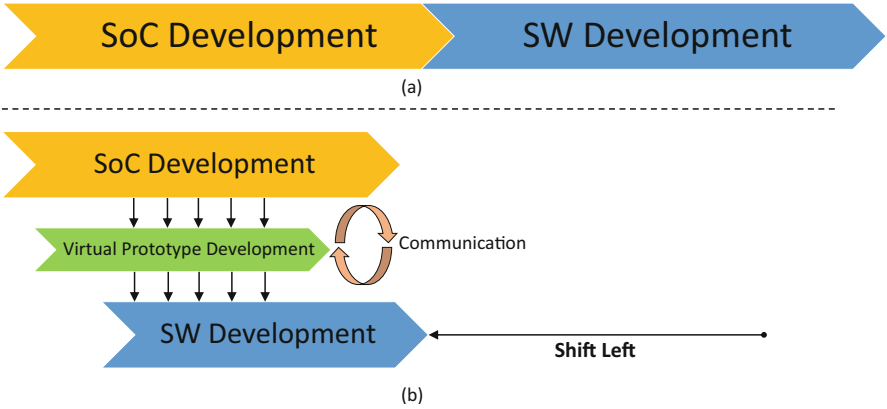

Fig. 1.1 Early SW development leveraging shift left concept

verified third-party *Intellectual Property* (IP). It allows them to focus more on the *Unique Selling Point* (USP) of their HW and SW. With the increased SW feature-rich functionality and complex interactions between different HW components, the design complexity has increased manyfold making the design verification of heterogeneous SOCs an increasingly daunting task.

The second challenge in verification of heterogeneous SOCs is the slow joint simulation speed of *Register Transfer Level* (RTL) and SPICE (Simulation Program with Integrated Circuit Emphasis) models for the digital and analog/RF part of the SOC [9]. Traditionally, analog/RF verification methodology was ad hoc by nature and these IPs were always verified by separate teams. It was driven by directed tests run over sweeps, corners, and Monte Carlo analysis. Unfortunately, it has not changed much until now and creates a bottleneck in the design and verification process. On the other hand, digital IPs had formalized verification methodologies used by separate teams. This included executable verification plans, constrained-random stimulus generation [119], testbench automation, assertions, and coverage metrics. These pre-verified analog, RF, and digital IPs were later on integrated together in a mostly digital SOC design and SW was executed on top to test if everything works as expected. However, due to multi-functional nature of the heterogeneous SOCs, the analog and RF IPs in particular have become very complex with significant digital control logic. Furthermore, the interaction of analog/RF and digital IPs has increased significantly, in particular when SW running on top is considered as well [77]. Hence, the traditional verification approaches are no longer adequate. The joint simulation, while slow, is still considered a golden standard because of high accuracy and cannot be ignored. However, it is too slow for chip-level simulations, unless it is used extremely selectively.

Third, design space and architectural exploration is restricted. Given the system requirements, finding the optimal system configuration is a tiring task. Each