WIDE BANDGAP NANOWIRES

SYNTHESIS, PROPERTIES, AND APPLICATIONS

TUAN ANH PHAM • TOAN DINH
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Synthesis, Properties, and Applications

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Preface

The last two decades have witnessed a remarkable progress in the field of semiconducting nanowires, which provide unique features such as high electron mobility, tunable mechanical properties, and high surface to volume areas. Starting with the bottom-up synthesis of silicon nanowires and nanorods in the early of 2000s, over one hundred types of nanoscale materials are today widely deployed in numerous nanoelectromechanical systems (NEMS) applications. Among these, wide bandgap nanowires such as III-nitride, silicon carbide, diamond, and oxide semiconductors have attracted a great deal of attention from the research community and the electronic industrial sector, due to their superior physical and chemical properties. The large breakdown voltage, electrical stability at elevated temperatures, and corrosive tolerance in this group of semiconductor nanowires enable a new class of NEMS sensing devices that function in extreme environments, where silicon-based counterparts fail to deliver a reliable operation.

This book systematically summarizes the state-of-the-art works on wide band gap semiconductor nanowires from material synthesis, to device development, to practical applications. The book starts with an introductory level and then develops further into deeper technical contents. This structure is highly suitable for a broad range of readership including undergraduate/postgraduate students as well as engineers and researchers working on the field of NEMS. The book aims to provide a fundamental guideline for NEMS designers, covering key parameters such as choice of materials, nanoarchitectures, fabrication and integration approaches, and functional mechanisms for particular electronics and sensing applications.

With the completion of this book, we would like to thank the generous supports from research funding agencies such as the Australian Research Council (ARC), the Innovative Manufacturing Cooperative Research Centre, Australia (IMCRC), as well as our industrial partners such as SPTS Technologies, Rio Tinto, and QuestSemi who have been greatly supporting our research on silicon carbide and gallium nitride (two representative materials of the wide band gap semiconductor group) over the last decade. We also acknowledge our long-standing collaborators including Prof. Dzung Viet Dao and Prof. Sima Dimitrijev at Griffith University, Prof. Takahiro Namazu at Kyoto University of Advanced Science, Prof. Toshihiro Itoh at The University of Tokyo, Prof. Debbie G. Senesky at Stanford University, Prof. Mina Rais-Zadeh at NASA, JPL, and Prof. John A. Rogers at Northwestern University for their dedication and effort in pushing the frontiers of this fast-growing research area.

Although we have edited and proofread this book carefully, mistake and typos are unavoidable. We welcome any feedbacks and suggestions from the readers.

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10 December 2021

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Bottom-Up Growth Methods

1.1 Introduction

Wide bandgap semiconductor nanowires have recently attracted increasing attention from researchers and engineers due to their superior chemical inertness and mechanical properties together with interesting electronics and electrical behaviors [1–6]. In particular, the chemical inertness of wide bandgap semiconductors offers the reliable and long-term operation, while their large energy gap allows for high-temperature operation and unique functionalities that cannot be achieved with the conventional Si nanowires. Importantly, nanowires exhibit numerous advantages compared with their bulk counterparts at the nanoscale level, including tunable properties, large surface-to-volume ratios, excellent sensitivity, low power consumption, and the ability to integrate different functional elements into a single chip [7–10]. For example, piezoresistance of top-down and bottom-up fabricated Si nanowires was found to be much more significant compared with that of bulk Si [11, 12]. Moreover, the quantum confinement of nanowires may result in exotic properties in sensing and optoelectronic devices such as tunable band gap and fast operation speed [13–15]. Another vital benefit of nanowires is that, unlike conventional thin-film structures, lattice mismatch strain in nanowires can be relieved at the free surfaces by elastic deformation without dislocation defects [16–20]. These huge advantages of nanowires offer exciting opportunities for their integrations on diverse substrates for the fabrication of high-performance electronic and photonic devices, such as light-emitting diodes, sensors, photodetectors, and solar cells. In this context, it is realized that the resulting performance of such electronic devices strongly depends on the morphological quality and uniformity and the ability to control the doping types and concentration of synthesized wide bandgap semiconductor nanowires. However, these key parameters determining the electronic device performance are strongly associated with the choice of the synthesis and fabrication methods. Therefore, an in-depth understanding of the synthesis and fabrication methods of wide bandgap semiconductor nanowires is highly necessary to achieve the desired nanowires bearing a high degree of structural perfection with tunable electronic properties.

To date, various approaches have been employed to synthesize and fabricate a wide range of wide bandgap semiconductor nanowires. Among them, the bottom-up approach has been currently considered as one of the most effective methods for the nanowire's fabrications. The bottom-up method is usually defined as an additive process, in which atoms and molecules are the basic building for the construction of various sophisticated nanostructures. This method exhibits a huge flexibility to synthesize high-quality wide bandgap

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semiconductor nanowires bearing controllable and programmable properties. On the other hand, the most significant drawbacks of the bottom-up approach are the limitation of large-scale uniformity and integration of different elements into functional devices. Considering advantages and disadvantages of this approach, an in-depth understanding on the bottom-up growth of wide bandgap nanowires is highly necessary for researchers and engineers who are currently working toward the fabrication of semiconductor nanowires-based electronic devices. This chapter, therefore, will review the basic concepts as well as the recent progress on the bottom-up synthesis and fabrication of several widely used wide bandgap semiconductor nanowires. The chapter consists of three sections and its exposition is the following. After a brief introduction in Section 1.1, Section 1.2 contains an introduction to various growth mechanisms for the synthesis of wide bandgap nanowires using bottom-up approaches with an emphasis on advantages and limitations of each mechanism. Finally, Section 1.3 discusses the possibility to use different bottom-up synthesis techniques to effectively control over the atomic structures, crystalline orientation, chemical composition, defect densities, and doping concentration of wide bandgap semiconductor nanowires.

1.2 Bottom-Up Growth Mechanisms

1.2.1 Vapor–Liquid–Solid Growth Mechanism

The vapor–liquid–solid (VLS) mechanism has been the most widely exploited process among various effective processes developed for the bottom-up synthesis of semiconductor nanowires. This process was firstly introduced by Wagner and Ellis for large whisker growth in 1960s, where they employed Au particles as catalysts to grow crystalline silicon microwires from $SiCl_4$ and SiH_4 [21–25]. Over the past decades, considerable efforts have been devoted to uncovering many fundamental aspects of VLS growth mechanism, which could open-up new pathways to synthesize various wide bandgap semiconductor nanowires with an enhanced quality and uniformity [23, 26–28].

Because the growth process is extremely rapid under conventional growth conditions, probing the VLS growth of nanowires at different stages in real-time represents a huge technical barrier for researchers. In this regard, Wu et al. reported the first real-time observation of semiconductor Ge nanowire growth in an *in situ* high-temperature transmission electron microscope (TEM) [28]. Their results undoubtedly provided an insight into the VLS growth mechanism at nanometer scale. Figure 1.1 shows a series of *in situ* TEM images recorded during the growth process of Ge nanowires, providing direct evidence for the events at different VLS growth stages of Ge nanowires. In another pioneering work, Ross and coworkers systematically investigated the VLS growth of Au–Si system using a combination of ultra-high vacuum TEM and a capillary precursor delivery system. Their results provided much significant information on the growth kinetic of the VLS process, in which the growth proceeds in a layer-by-layer fashion [29]. In particular, the VLS mechanism relies on a three stage-process, including metal alloying, crystal nucleation, and axial growth stage as shown in Figure 1.2. In the alloying stage, a catalytic liquid alloy phase is formed on the substrate upon annealing. Subsequently, this alloy phase can rapidly absorb a vapor of precursors to its supersaturation level in the nucleation stage. Finally, nanowire growth can proceed from nucleated seeds at the solid/liquid interface in the growth stage.

Due to its great flexibility, the VLS process has been successfully employed to produce a wide range of wide bandgap semiconductor nanowires, such as silicon carbide (SiC), gallium

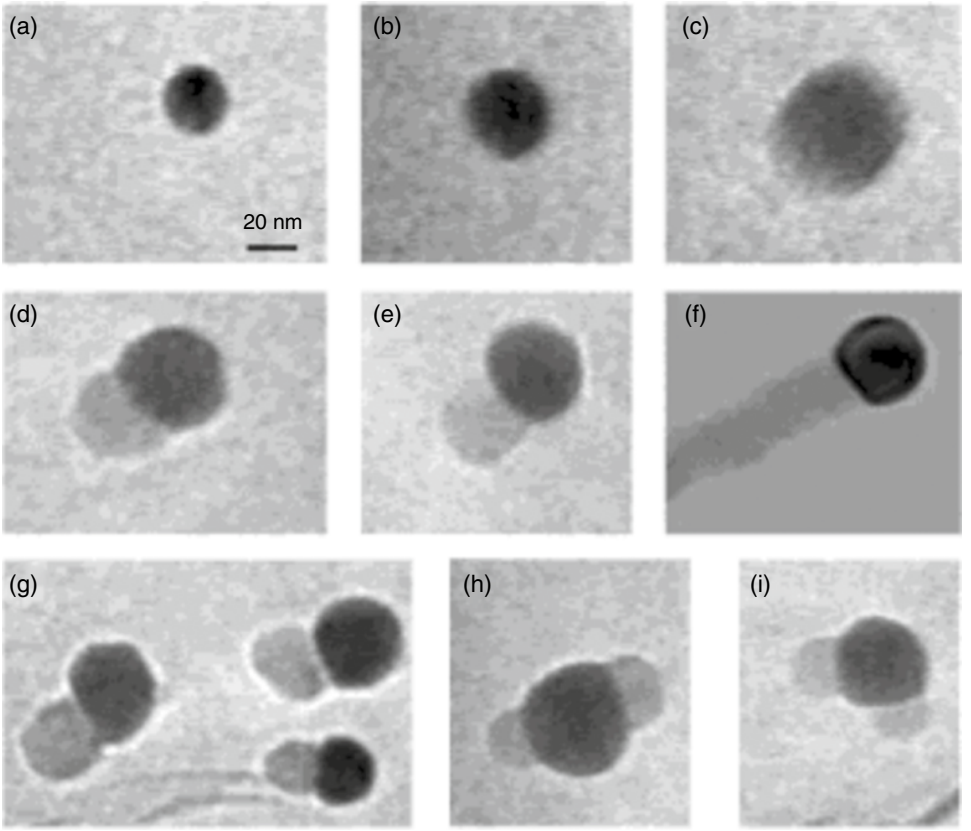

Figure 1.1 A series of *in situ* TEM images recorded during the process of Ge nanowire growth. (a) Au nanoclusters in solid state at 500 °C; (b) alloying initiates at 800 °C, at this stage Au exists in mostly solid state; (c) liquid Au/Ge alloy forms; (d) the nucleation of Ge nanocrystal on the alloy surface; (e) Ge nanocrystal elongates with further Ge condensation; (f) eventually a wire form; (g) several other examples of Ge nanowire nucleation. (h, i) TEM images show two nucleation events on single alloy droplet. *Source:* Reprinted from Wu and Yang [28].

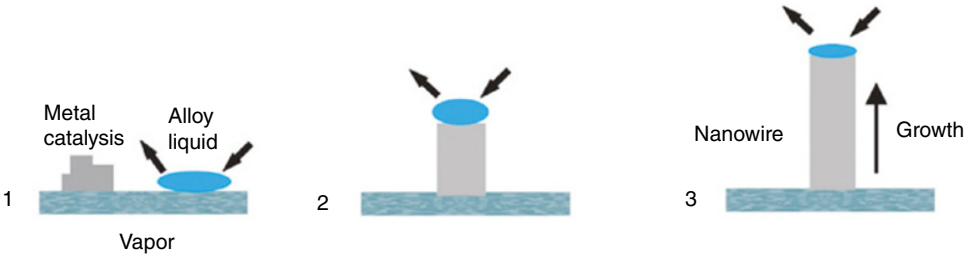

Figure 1.2 Schematic illustration of vapor–liquid–solid nanowire growth mechanism including three stages: (1) alloying, (2) nucleation, and (3) axial growth.

nitride (GaN), diamond nanowires, and others [30–34]. For example, SiC nanowires with 20 nm diameter and 20 μm length were grown directly on the surface of bulk SiC ceramic substrate at elevated temperature using aluminum as a catalyst (Figure 1.3a,b) [35]. In another example, diamond nanowires were grown on a Si substrate using the chemical vapor

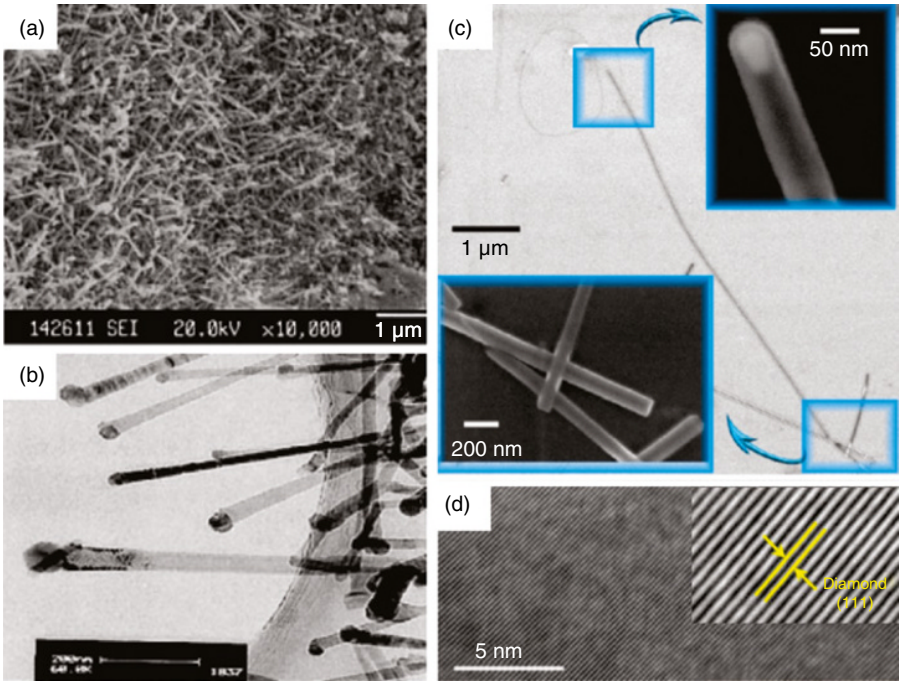

Figure 1.3 (a, b) SEM and TEM images of SiC nanowires growth by the VLS process, respectively. *Source:* Reprinted from Deng et al. [35]. (c) Electron microscopy of diamond nanowires encased within a carbon nanotube shell. The inset in (c) shows a catalyst embedded inside the tip of the nanowire. (d) The high-resolution TEM image of a single diamond nanowire. Inset in (d) shows a zoomed-in view of the crystalline structure of cubic diamond (111) surface. *Source:* Reprinted from Hsu et al. [36].

deposition (CVD) process based on the VLS mechanism with an iron catalyst. These diamond nanowires are straight, thin, and long over tens of micrometers with a high crystallinity and structural uniformity (Figure 1.3c,d) [36]. One of the main advantages of the bottom-up nanowire growth based on the VLS mechanism is that nanowires with different morphologies and structures can be synthesized in a controllable manner depending on the proper choices of the substrates, catalysts, and growth parameters (such as pressure, temperature, and time). For example, Wang et al. demonstrated the possibility to manipulate and control the morphology of VLS grown SiC nanowires from an Eiffel-tower shape to spindle shape by varying the pressure of the precursors. These new morphologies of SiC nanowires are completely different from cone or tip-shaped SiC nanowires commonly reported by other research groups as shown in Figure 1.4 [37]. In another work, Men et al. reported that under nickel (Ni)-based catalysis, SiC nanowires synthesized by VLS process were long and thin, and increased with increasing concentration. In contrast, under Fe-based catalysis, they were short and thick, and the influence of concentration on the morphology of nanowires is negligible [38]. On the other hand, Low et al. investigated the morphological and structural characteristics of GaN nanowires synthesized by Ni-catalyzed CVD method by varying the growth temperatures. The authors found that straight and smooth GaN nanowires with the best elemental composition were achieved at the optimal growth temperature of 950 °C [39]. In another interesting work reported by Krishnan et al., they found that the growth direction of SiC nanowires was dictated by the crystallographic

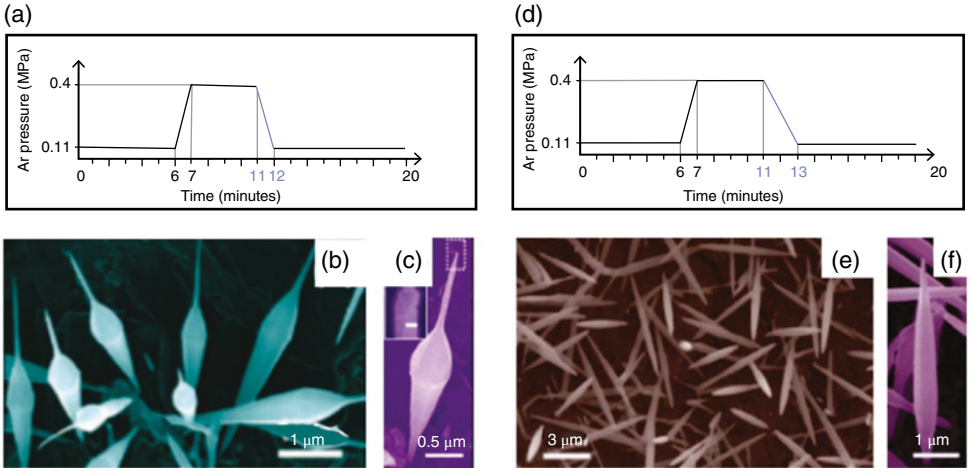

Figure 1.4 SiC nanowires with different morphologies ranging from an Eiffel tower to spindle shape depending on the pressure of the source species: (a) Schematic showing a three-step processing schedule. (b, c) SEM images of the SiC nanowires, showing an Eiffel-tower shape obtained using the processing schedule described in (a). (d) Processing schedule showing the difference in pressure as a function of time compared with the one shown in (a). (e) and (f) SEM image of SiC spindles obtained using the processing schedule described in (d). *Source:* Reprinted from Wang et al. [37].

orientation of the 4H-SiC substrates. This interesting result demonstrated that highly aligned SiC nanowires can be synthesized depending on the choice of substrates [40]. Another key merit of the bottom-up approach based on the VLS process is *in situ* doping by incorporating desired dopant precursors into the VLS synthesis procedure. This is very beneficial to the fabrication of high-performance electronic and photonic devices because such the bottom-up growth method eliminates the requirement for additional destructive processes, such as ion implantation, to introduce additional charge carriers to the as-grown nanowires. For instance, Gao et al. reported, for the first time, the synthesis of Al-doped SiC nanowires. According to their results, the doping levels of these nanowires were effectively controlled by tailoring the Al concentrations in the precursors, which caused redshifts of the photoluminescence bands [41]. In another example, Liu et al. successfully synthesized high-quality GaN nanowires doped with Si using the VLS mechanism, which showed a distinct blueshift from the bulk bandgap emission [42].

Despite these great benefits, the bottom-up nanowire synthesis based on the VLS process has some inherent drawbacks, which is basically induced by the presence of foreign metallic elements serving as catalysts in the synthesis process. These metallic particles usually result in the formation of unavoidable defects and thus lead to negative impacts on optical and electronic properties of the as-grown nanowires as unambiguously proven by numerous studies [43–47]. In this context, Karakostas and coworkers compared GaN nanowires grown by two different methods: catalyst-free or catalyst-induced methods utilizing Ni seeds. According to their findings, the catalyst-induced nanowires contain many more basal-plane stacking faults and thus, the photoluminescence of such nanowires is much weaker compared with that of the nanowires synthesized by the catalyst-free route as shown in Figure 1.5 [48]. A more critical problem is the incorporation of metallic particles within nanowires that typically causes detrimental impacts on device performance. For example, although gold (Au) is the most widely employed catalyst in the VLS process due to its

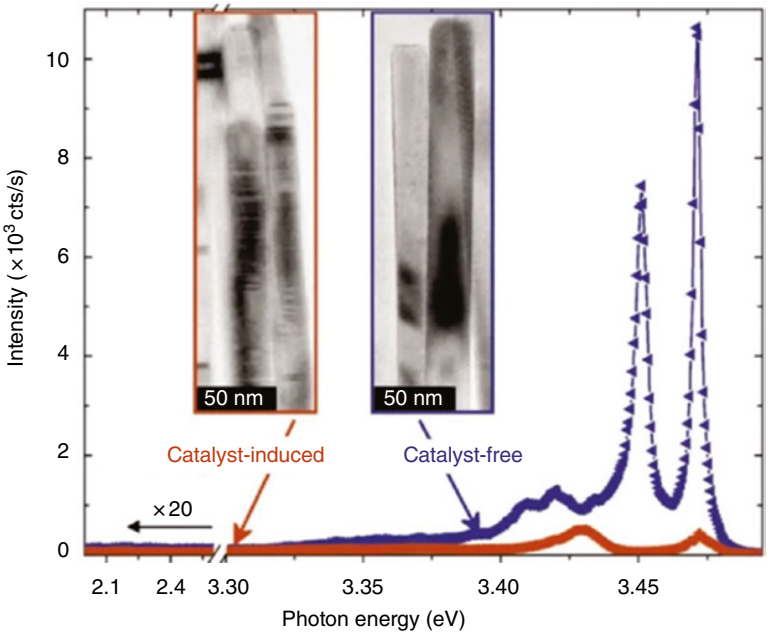

Figure 1.5 Low-temperature photoluminescence spectroscopy (PL) spectra of GaN nanowires grown by catalyst-induced and catalyst-free growth methods. Insets show the corresponding TEM images showing the stacking faults for the case of catalyst-induced growth method. *Source:* Reprinted from Cheze et al. [48].

superior catalyst properties, Au exhibits a fast diffusion from the surface into the underlying Si substrate and then acts as a deep-level trap, reducing the carrier lifetime, which is inherently incompatible with semiconductor technology [49, 50]. To overcome these daunting challenges, a considerable number of studies have been devoted to establishing new strategies for the catalyst-free synthesis of wide bandgap semiconductor nanowires [51–53]. For example, Noborisaka et al. reported the fabrication of GaAs nanowires on a GaAs(111) substrate using selective-area metal–organic vapor-phase-epitaxial growth. In this work, a circular mask opening with a diameter of 50–200 nm was defined on a thin SiO_2 partially coated on the GaAs substrate. As a result, GaAs nanowires with a typical diameter ranging from 50 to 200 nm and a height ranging from 2 to 9 μm were formed on the substrate without any catalysts depending on the opening size of the masked substrate [51]. In another interesting study, Paek et al. demonstrated the possibility to grow GaAs nanowires on a Si substrate using molecular beam epitaxy (MBE) techniques based on the VLS process with different Ga and As fluxes. The authors found that the diameter of GaAs nanowires can be tailored by controlling the Ga and As fluxes under ultra-high vacuum conditions [52]. Detailed information on the catalyst-free synthesis routes of various wide bandgap nanowires will be discussed in the Section 1.3.

1.2.2 Vapor–Solid–Solid Growth Mechanism

The vapor–solid–solid (VSS) mechanism is relatively similar to the VLS growth mechanism. The only difference between these mechanisms lies in their catalyst states. In the VSS process, the catalysts remain in a solid state, while that of the VLS process is in a liquid state. The VSS

process was first introduced by Kamins et al. in 2000 when they synthesized silicon nanowires on Si substrates using $TiSi_2$ islands as catalysts [54]. According to their results, the $TiSi_2$ islands remain solid and anchored to the substrate during the growth, while the silicon nanowires grow out from the $TiSi_2$ islands remaining at their bases as shown in Figure 1.6. This differs from the VLS process, where the growth occurs at the tip of the nanowires when the solubility of Si in the liquid droplet reaches saturation. Compared with the VLS growth with liquid catalysts, the VSS growth possesses several advantages, which could benefit the bottom-up synthesis of wide bandgap semiconductor nanowires. First, the VSS growth can be carried out at reduced temperatures in comparison with the VLS growth due to the catalyst remains in a solid state. Second, the VSS growth can minimize the incorporation of unwanted impurities from the metal catalysts, which is based on the reduction of atom diffusion and solid solubility during the growth of nanowires at lower temperatures. Third, the crystalline structure of solid catalysts may offer a huge opportunity to obtain nanowires with a high degree of structural perfection, regardless of the chosen substrates. Finally, the VSS process may enable more abrupt interfaces in axial nanowire heterostructures by mitigating the so-called reservoir effect due to solid solubility, which is usually much lower than liquid solubility for the same materials [55–57]. For example, Wen et al. demonstrated that single interfaces in Si–SiGe heterostructures with defect-free and close to atomically abrupt can be obtained using solid Al–Au alloy catalyst particles instead of conventional liquid semiconductor–metal eutectic droplets [57]. On the other hand, the VSS growth still remains a shortcoming compared with the VLS growth is that the VSS growth rate is significantly slower than the VLS growth rate at similar growth conditions due to the weaker surface reactivity as well as lower diffusivity through the solid in the VSS process [58]. To overcome this technical barrier, Wen et al. added Al to the Au catalyst to raise the eutectic temperature so that the growth can be achieved at higher temperature with reasonable growth rate but still keep the alloy catalyst in the solid state [57, 59].

To date, the VSS growth mechanism has increasingly attracted researchers as an alternative to grow wide bandgap semiconductor nanowires. For example, Hou et al. reported the Au-assisted growth of GaN nanowires based on the VSS mechanism using the plasma-enhanced chemical vapor deposition (PECVD). The authors claimed that the detachment and migration of Au catalyst seeds in the growth can be controlled by the partial pressure of gallium and nitrogen radicals [60].

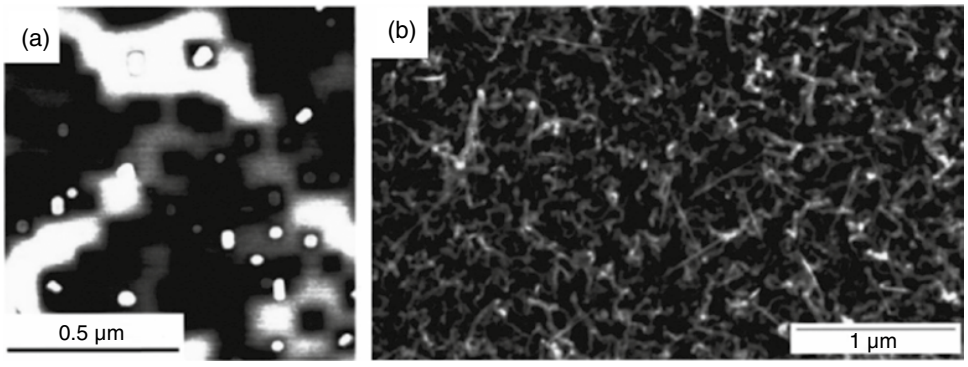

Figure 1.6 (a) Atomic-force micrographs of $TiSi_2$ islands formed by chemical vapor deposition at 640 °C on Si(001) and (b) scanning-electron micrograph of long, dense Si nanowires nucleated on Ti-containing islands grown on Si(001) at 670 °C. *Source:* Reprinted from Kamins et al. [54].

In another example, Wang and coworkers synthesized GaN nanowires via the VSS mechanism by Ni-assisted metal–organic chemical vapor deposition (MOCVD). According to this work, a sputtered nickel film on *c*-plane sapphire was used as a substrate, while trimethylgallium (TMG) and ammonia were employed as precursors. After introducing TMG into the reactor, the nickel film was transformed into Ni_3Ga nanoparticles via thermodynamically favored reaction between Ni and Ga at 900 °C. These nanoparticles keep capturing Ga species and become supersaturated. Consequently, the Ga species react with the decomposed ammonia at the surface of the Ni_3Ga particles to form GaN nanowires [61]. Despite these huge achievements, the VSS growth mechanism remains much less understood in both theoretical and experimental aspects. Therefore, considerable efforts have been devoted in the past years to obtaining a better understanding on the VSS mechanism. In this context, Cui et al. developed a general mass-transport-limited kinetic model to describe the VSS growth process of Si nanowires. In this model, the VSS mechanism proposed by the authors is illustrated in Figure 1.7 and can be described in following steps: (i) atoms diffuse from the vapor phase to adsorb at the surface of catalyst; (ii) the diffused atoms hit the sidewall areas of the nanowires at an incident angle of θ; (iii) the desorption of adatoms from the catalyst; (iv) adatoms diffuse along the sidewalls of the nanowires; (v) the desorption of adatoms from the sidewall; (vi) and (vii) the diffusion and desorption of adatoms from the substrate, respectively; and (viii) adatoms diffuse at the catalyst–nanowires interfaces. Thus, the authors considered three surface diffusion processes and a slow interface diffusion process. The former is associated with the atoms transport pathway, while the later relates to the rate-determining step for the VSS growth of nanowires [62].

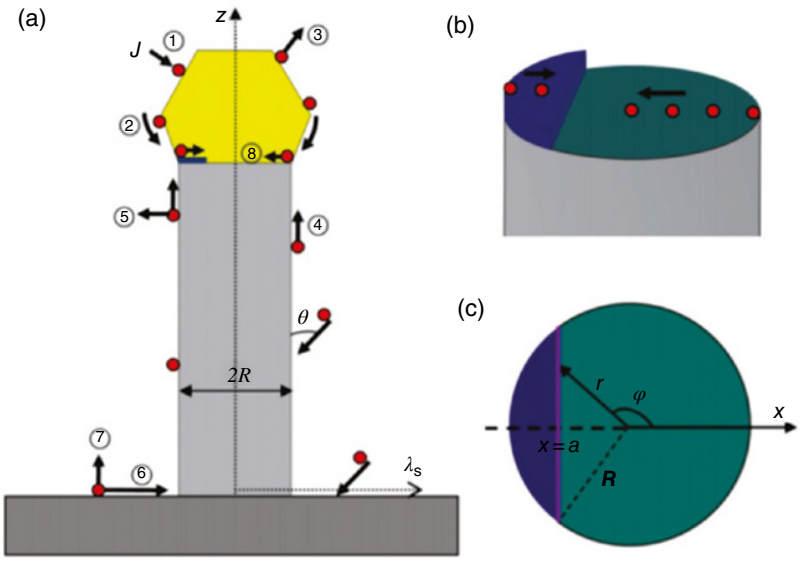

Figure 1.7 (a) Schematic illustration of the step-flow growth of nanowire via VSS mechanism: (1) impinging flux from the vapor, (2) adatoms diffusion flux on the surface of catalyst, (3) desorption from the catalyst, (4) adatoms diffusion flux on the sidewalls, (5) desorption from the sidewalls, (6) adatoms diffusion flux on the substrate, (7) desorption from the substrate, (8) atom diffusion flux in the interface. (b) Detailed atom diffusion and step movement at the catalyst–nanowire interface. (c) Coordinate system used in the calculation of step movement at the catalyst–nanowire interface. *Source:* Cui et al. [62] / American Chemical Society.

This model offers an exact solution to demonstrate the impact of various kinetic parameters on the VSS growth mechanism, which could be extended to various types of wide bandgap semiconductor nanowires. Together with theoretical studies, several experimental studies have also been conducted to get an insight into the VSS growth mechanism. For instance, Maliakkal et al. investigated the VSS mechanism via the nickel-assisted growth of GaN nanowires using MOCVD [63]. The authors proposed that unlike the traditional VLS mechanism where the material is collected directly from the vapor by the liquid alloy, there are three different modes by which reactants can reach the catalyst particles in the VSS process as shown in Figure 1.8a. According to the authors, the correlation between diameter and length of nanowires can provide information to determine the mode in which the reactants reach the catalyst. Interestingly, the authors observed an initial increase in length with

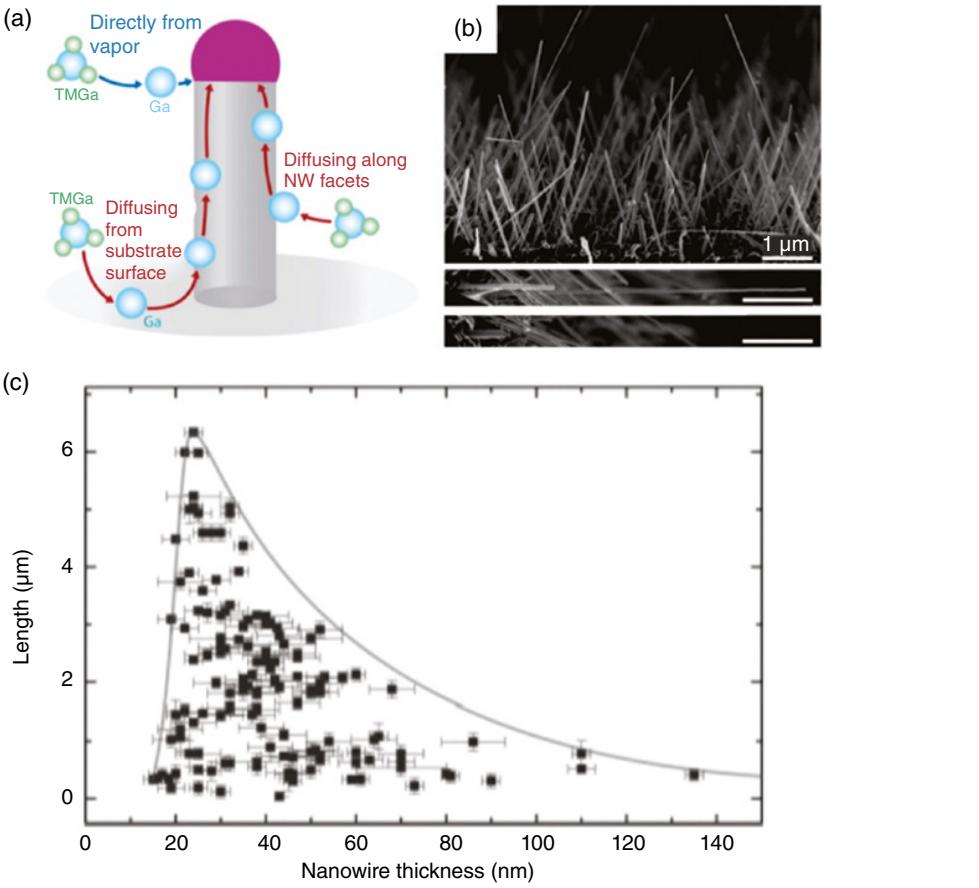

Figure 1.8 (a) Schematic showing the three different modes by which reactants reach the catalyst particle. The supplied precursor molecules can be collected (i) from the vapor phase directly into the catalyst, (ii) from adatoms on the NW side facets diffusing into the catalyst, or (iii) from adatoms on the substrate surface that diffuse along the substrate and NW side surfaces into the catalyst. (b) Side-view SEM image of the GaN NWs grown on *r*-plane sapphire. It is evident that the thick wires are short, and the thin wires are long. Enlarged versions of a couple of representative NWs are shown at the bottom. The scale bars correspond to 1 μm. (c) Plot showing the distribution of length and thickness for more than 130 NWs. *Source:* Reprinted from Maliakkal et al. [63].

increasing thickness of nanowires due to Gibbs–Thomson effect and subsequently, a decrease in length when the thickness of nanowires is larger than a certain value as the consequence of the diffusion-induced growth mechanism as shown in Figure 1.8b,c. In another example, Cheze et al. examined the nucleation of Ni-induced GaN nanowires driven by the VSS process through *in situ* monitoring employed quadruple mass spectroscopy and reflection-high energy electron diffraction [64]. According to their findings, three nucleation stages of the growth were evidenced. The first stage relates to Ga incorporation into the Ni collector. The second stage corresponds to the transformation of the crystal structures of the collector. The third stage is the nucleation of GaN nanowires under the Ni collectors. These findings are expected to provide significant information to control the growth of various wide bandgap semiconductor nanowires based on the VSS mechanism.

1.2.3 Vapor–Solid Growth Mechanism

As mentioned in the previous sections, the VLS and VSS mechanisms offer many huge advantages for the bottom-up synthesis of nanowires; however, the use of foreign metallic particles as catalysts remains an inherent challenge, which significantly limits the possibility to achieve high-performance wide bandgap semiconductor nanowires. Hence, the development of catalyst-free synthesis processes is highly needed for the bottom-up synthesis of nanowires in order to eliminate negative impacts of catalysts on the nanowire growth. In this regard, the vapor–solid (VS) mechanism is currently viewed as a reliable approach to synthesize a series of wide bandgap semiconductor nanowires without the presence of catalysts. Due to the absence of energetically favored catalyst sites to promote the growth, the VS process usually requires a higher synthesis temperature compared with that of the VLS and VSS mechanisms. On the other hand, the synthesis process based on the VS mechanism is relatively simple compared with other catalyst-based synthesis methods. In general, the VS process starts via the decomposition of precursor gases at the chosen substrates induced by high reaction temperatures or the evaporation of precursor powders upon thermal annealing at elevated temperatures [65]. During the VS growth process, three interfaces have to be taken into consideration, including vapor–substrate interface, vapor–solid interface, and solid–substrate interface. The vapor–substrate interface is the place where the nucleation occurs, which plays a crucial role for the VS growth process. The precursors adsorb on the substrate surface and, subsequently, condense into solid to form nucleus. At this interface, the nucleation step can be optimized via controlling various growth parameters, such as deposition temperatures, pressure, and substrate surface conditions. After the nucleus formed, the vapor–solid interface is also important, which could generate the one-dimensional epitaxial growth of nanowires. Otherwise, only nanoparticles can be formed on the substrate surface. The solid–substrate interface is generally associated with the influence of the chosen substrates on several important aspects, such as, the defect density, structure, orientation, and morphology of the as-grown nanowires via the VSS mechanism [66]. Another fundamental aspect influencing the VS growth of nanowires is the supersaturation ratio of the condensing species. In this context, Hsu et al. investigated the VS growth mechanism of Sn nanowires and found that the supersaturation ratio of the condensing species must be maintained below a critical value to ensure anisotropic growth to form nanowires. Otherwise, two-dimensional growth or even isotropic growth can occur. Moreover, homogeneous nucleation in the vapor phase can lead to the formation of powder forms, instead of nanowire forms, at high supersaturation ratios [67].

To date, various types of wide bandgap semiconductor nanowires have been synthesized using the VS mechanism [68–70]. For example, Chen and coworkers synthesized single crystalline 3C-SiC nanowires with lengths up to several tens of micrometers and diameters of 20–60 nm via a simple catalyst-free method based on the VSS mechanism using silicon powders and expandable graphite as raw materials. In this work, the authors proposed the VS mechanism to interpret the growth procedure of SiC nanowires as following: When temperature is up to 200 °C, the expandable graphite begins to expand and generates a porous and loose structure. Subsequently, oxygen in the furnace reacts with silicon and carbon to produce SiO and CO. In the next step, SiO reacts with carbon to form SiC embryos. Finally, the newly formed SiC nucleus deposits on the top of SiC nanowires form the long SiC nanowires [68]. Detailed steps of the VS growth process and the 3C-SiC nanowires obtained by this method are shown in Figure 1.9. In another work, Yazdi and coworkers synthesized highly oriented AlN nanowires with aspect ratio up to 600, diameter in the range of 40–50 nm, and 100 μm lengths via the VS growth mechanism. The as-grown nanowires are dislocation free single crystal and perfectly oriented along the *c*-direction of the wurtzite structure. The authors claimed that the AlN nanowires change in thickness after they have reached a critical length, which contributes to the understanding of the VS growth mechanism [69]. In another example reported by Zhou et al., they synthesized large-scale GaN nanowires by thermal evaporation of GaN powders under controlled conditions based on the VSS mechanism. The as-grown GaN nanowires are about 30 nm in diameter and several hundreds of microns in length, providing excellent dielectric properties. The main feature of the VS growth in this study is that the equilibrium phase diagrams can be used to predict a dislocation and growth conditions, thus enabling rational synthesis for large quantities of single crystalline GaN nanowires at relatively high purity and low cost [70].

Controlling and optimizing the uniformity, morphology, crystalline structures, and defect density of the as-grown nanowires via the VS process play an important role in the bottom-up fabrication of high-performance photonic and electronic devices. This challenging task can

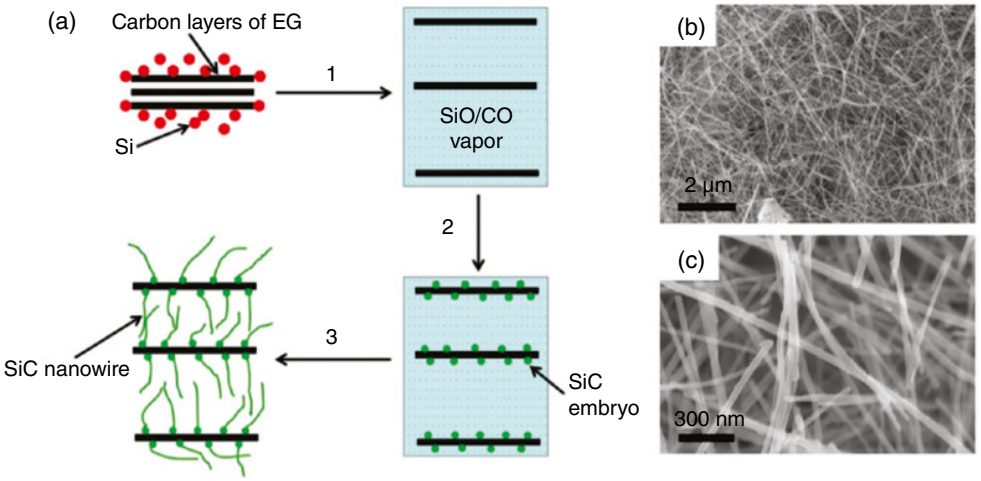

Figure 1.9 (a) A cartoon illustrates the VS growth process of 3C-SiC nanowires: (1) Expandable graphite expands, and SiO/CO vapor is formed; (2) SiC embryos are produced by heterogeneous nucleation; (3) long SiC nanowires grow along the (111) direction. (b, c) SEM images of SiC nanowires at different magnifications. *Source:* Reprinted from Chen et al. [68].

be achieved by tuning the evaporation of precursors, the vapor pressure, the substrate surface temperature as well as a proper selection of raw materials. For example, Wu et al. demonstrated that SiC nanowires synthesized by the VS mechanism can be tuned to cylinder, hexagonal prism, or bamboo shape by simply altering the reaction temperature from 1470, 1550 to 1630 °C, respectively [71]. More interestingly, Shen et al. reported the controlled synthesis of various high-quality GaS nanostructures, ranging from nanowires to nanobelts, hexagonal microplates, and heterostructures via a simple VS method by tailoring the substrate temperature and evaporation source as illustrated in Figure 1.10 [72]. According to their results, GaS nanostructures can be formed with different morphologies depending on the choice of the substrate temperature as shown in Figure 1.11. In particular, single crystal GaS nanowires with uniform diameters of around 20 nm are formed at a substrate temperature slightly less than 800 °C. When the substrate temperature reaches 800 °C, the products were composed of numerous nanobelts with typical lengths of several tens to hundred micrometers. When the substrate temperature is between 800 and 850 °C, many zigzag GaS nanobelts with widths of 1–2 μm were found. At the substrate temperature of 950 °C, GaS microbelts were formed instead of GaS nanobelts. Especially, in the case of lower substrate temperature, only hexagonal GaS microplates were formed at 650 °C [72]. These interesting results unambiguously demonstrated the possibility to control morphologies as well as structures of wide bandgap semiconductor nanowires via tailoring growth parameters in the VSS process.

1.2.4 Solution–Liquid–Solid Growth Mechanism

The solution–liquid–solid (SLS) mechanism is classified as one of the solution-based synthesis processes. This mechanism was firstly introduced in 1995 by Buhro and coworkers when

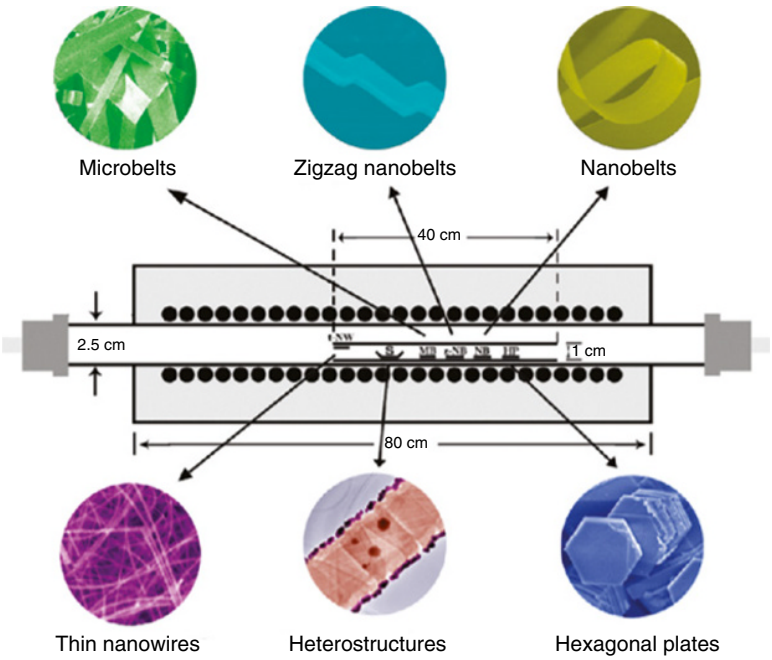

Figure 1.10 Vapor–solid method used for the controlled growth of one-dimensional GaS nanostructures, ranging from nanowires to various types of nanobelts, hexagonal plates, and heterostructures. *Source:* Reprinted from Shen et al. [72].