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Limin Jia · Yong Qin · Jianying Liang ·
Zhigang Liu · Lijun Diao ·
Min An *Editors*

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Novel Traction Drive Technologies of Rail Transportation

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Contents

Overview of Multilevel Inverter Topologies and Modulation Methods

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Abstract. Multilevel inverter has the advantages of good power quality, high inverting efficiency, small electromagnetic interference and so on. It is widely used in power system, power transmission, motor drive, electromagnetic launch and other large power conversion occasions. In this paper, a brief overview of multilevel inverter topologies is given to provide ideas for the construction of multilevel inverters with different applications and characteristics. The main research achievements of existing multilevel inverter technologies are mainly introduced, including classic multilevel topologies, new multilevel topologies, classic modulation methods, and optimized modulation methods. The common topologies are compared, and the new applications of multilevel inverter in various fields are introduced. The development trend of multilevel inverter technology and the latest progress in control are pointed out, which provides a reference for the wide application of multilevel inverter technology in industry.

Keywords: Multilevel inverter · Topology · Modulation method · Development trend

1 Introduction

Multilevel inverter is a kind of power electronic system using multiple DC power supply as input to generate more than two-level AC output [1]. Because multilevel inverter has the following advantages: small output harmonic, small dv/dt, small device voltage stress, low-voltage devices to achieve high-voltage output. Therefore, it is widely used in high-voltage variable-frequency speed regulation system, renewable energy generation, power system, electrified transportation, electromagnetic launch and other fields.

At present, the development of multilevel inverter is still facing great challenges. Scholars at home and abroad have been committed to studying new topologies and modulation methods of multilevel inverter, further improving the inverter efficiency, reducing its cost and complexity, minimizing the number of devices, maximizing the number of output levels, and making the technology have a wider range of applications and greater competitiveness [2].

This paper reviews classic multilevel inverter topologies and new topologies, also summarizes the applications of multilevel inverter in various fields. In addition, this paper introduces classic modulation methods and optimized methods. Finally, the development direction and trend of multilevel inverter are summarized.

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2 Multilevel Inverter Topologies

In 1980, Japanese scholar Nabae A put forward the idea of multilevel inverter [3]. Its basic principle is to output a series of step waves to approximate sinusoidal modulation wave.

According to the generation of output level, the classic multilevel inverter topologies can be divided into three categories: Neutral-Point-Clamped, Flying Capacitor and Cascaded.

(1) Neutral-Point-Clamped (NPC): The DC bus is divided by capacitor and leads out the neutral point to get multiple levels.
(2) Flying Capacitor (FC): By introducing the floating capacitor which can be charged and discharged, the voltage of the floating capacitor is increased or decreased through the DC bus to obtain multiple levels.
(3) Cascaded: Multiple levels are output through modular series connection of two-level or multi-level units.

2.1 Neutral-Point-Clamped (NPC)

The three-level NPC inverter topology was first proposed by Nabae A in 1980, and was extended to arbitrary multilevel structure by Bhagwat P and others at IEEE industrial application annual meeting in 1983 [4].

The different combination of switching devices on or off enables the inverter to output voltage waveforms of various levels, and a single-phase five-level NPC topology is shown in Fig. 1. The NPC multilevel inverter has the advantages of high output power, high equivalent switching frequency, wide transmission bandwidth and low switching loss, but it also has the following shortcomings [5].

(1) A large number of clamping diodes are needed. For an M-level NPC inverter, each phase needs (M-1)(M-2) clamping diodes with the same voltage level. These diodes not only increase the cost, but also bring some difficulties to the installation. Therefore, in practical applications, only inverters with less than seven-level are suitable for this topology, and the universality is not high.
(2) The conduction load of switching devices is unbalanced. In Fig. 1, switch S1 is on only when $U_{out} = U_{dc}$, while switch S4' is off only when $U_{out} = 0$. The difference of conduction load will make the switching devices work in different current values. If the current value of the device is considered according to the maximum conduction load, the current level of 2(M-2) outer devices per phase is too large, resulting in a waste of resources.

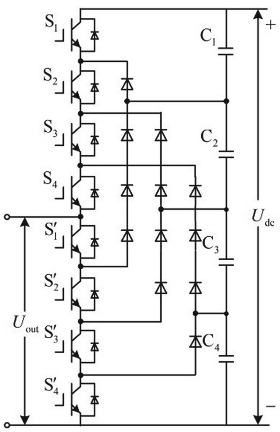

Fig. 1. Five-level NPC topology

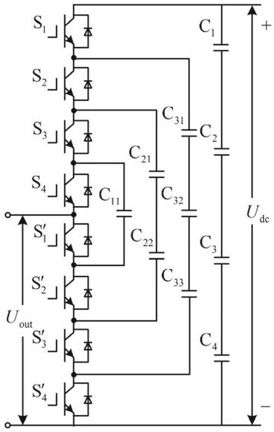

Fig. 2. Five-level FC topology

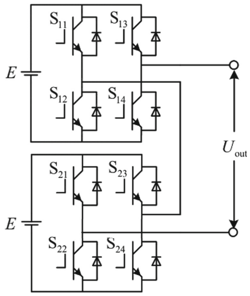

Fig. 3. Five-level CHB topology

2.2 Flying Capacitor

In order to reduce the excessive number of clamping diodes in the NPC multilevel topology, French scholars Meynard T and Foch H proposed the FC topology [6] at the power and energy system conference in 1992. In this structure, the flying capacitor is used to replace the clamped diode, and the DC-link capacitor remains unchanged.

The single-phase five-level FC topology is shown in Fig. 2. In this topology, each phase bridge arm has the same structure. The connection mode of the switching devices is basically the same as that of the NPC. The inner capacitors are independent of each other, and the DC-link is also four series capacitors with the same voltage value. Compared with the NPC, the FC multilevel topology is more flexible, has stronger power device protection ability, and can control the active power and reactive power at the same time. It can play a greater role in HVDC transmission system, but it also inevitably has the following disadvantages [7].

(1) A large amount of storage capacitance is required. If the voltage level of all capacitors is the same as that of switching devices, the M-level FC topology needs (M-1)(M-2)/2 auxiliary capacitors per phase, plus the M-1 capacitor required by the DC-link, which will also bring cost and installation difficulties to the multilevel inverter.
(2) When synthesizing the intermediate level, the system must use a variety of switch combinations to ensure the voltage balance of the DC-link capacitor, which increases the complexity of the control.
(3) Just like the NPC, the FC multilevel topology also has the problem of unbalanced conduction load.

2.3 Cascaded H-Bridge (CHB)

In order to increase the number of levels to obtain a higher output voltage and reduce the output harmonics, Marchesoin M proposed the idea of CHB inverter in 1988, but it was not widely promoted at that time due to various reasons. In 1996, American scholar Peng F systematically proposed the CHB topology and applied it to the field of reactive power compensation. Then, this topology was widely used.

Figure 3 shows a single-phase five-level CHB topology. The CHB topology is composed of several cascaded power units. Each power unit has its own independent DC power supply, and uses four switching devices to form the H-bridge structure. A multilevel inverter cascaded by N power units can output 2N+1 level phase voltage and 4N+1 level line voltage. At the same time, the three-phase inverter system can be easily constructed by triangle or Y-connection.

As a structure of cascaded power units with independent DC power supply, the CHB does not need to use control algorithm to solve the DC-link capacitor voltage imbalance problem of the NPC and FC topology when using low-voltage switching devices to obtain multilevel high-voltage output, which is much simpler in control [8, 9].

In general, the CHB topology has the following advantages:

Table 1. Comparison of the number of devices required for each phase of three multilevel topologies.

	NPC	FC	CHB
Power switch	2(M-1)	2(M-1)	2(M-1)
Clamped diode	(M-1)(M-2)	0	0
Flying capacitor	0	(M-1)(M-2)/2	0
DC-link capacitor	M-1	M-1	(M-1)/2

(1) The CHB can achieve multilevel output, and the number of devices required to achieve the same level is the least. When the above three multilevel topologies output M level, the number of devices required for each phase is shown in Table 1. Without the limitation of clamping diodes or flying capacitors, the CHB multilevel inverters can be easily extended to any level without complicating the main circuit structure.

(2) Each H-bridge unit has the same structure and is easy to be modularized and packaged. When a unit fails and bypasses it, it will not affect other units, and the system reliability is guaranteed.

(3) The DC-link of each H-bridge unit adopts independent DC power supply, so there is no voltage imbalance problem and it is easy to realize PWM control.

Based on the above advantages, the CHB topology is widely used in electromagnetic launch, motor drive, static synchronous compensator (STATCOM), high-voltage DC transmission and other high-power occasions [10]. However, the CHB topology has the following two shortcomings. First, it needs multiple independent DC power supply which is powered by multi winding transformer or energy storage unit. Second, it has no common DC bus, so it is difficult to feedback energy.

3 New Multilevel Inverter Topologies

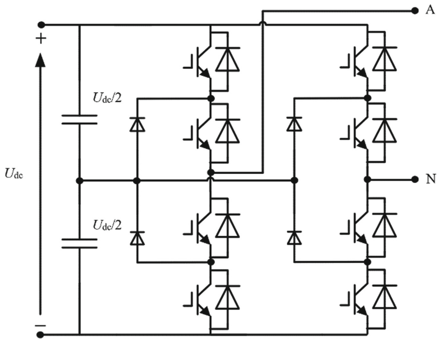

Fig. 4. Single-phase 5L-HNPC inverter topology

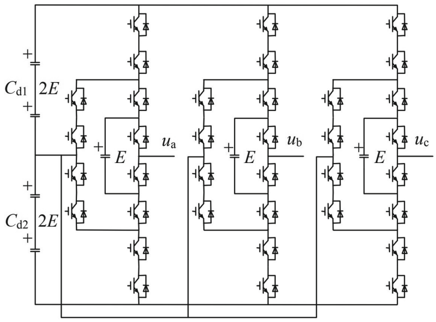

Fig. 5. Three-phase 5L-ANPC inverter topology

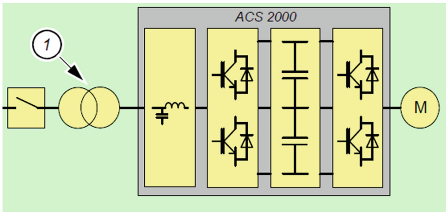

Fig. 6. Circuit structure of ACS2000

In recent years, many novel multilevel topologies have been developed. Most of them are variants or hybrids of three classical multilevel topologies, but most of them have not been applied to industry [11]. Among the new topologies, the five-level H-bridge Neutral-Point-Clamped (5L-HNPC), the three-level Active Neutral-Point-Clamped (3L-ANPC) and the five-level Active Neutral-Point-Clamped (5L-ANPC) have been applied. In addition, some other new topologies are under development, such as asymmetric CHB with unequal DC sources, cascaded NPC with open end load, hybrid NPC-CHB, hybrid FC-CHB and TCHB topologies [12]. Three new multilevel topologies and their applications are introduced as follows.

3.1 Five-Level H-bridge Neutral-Point-Clamped (5L-HNPC)

The hybrid HNPC consists of NPC connected by H-bridge structure. As shown in Fig. 4, the 5L-HNPC consists of two 3L-NPC phase legs based on IGBT. This kind of high-power inverter can be applied in the actual system with power range of 2–8 MW (air cooling) or 5–23 MW (water cooling), and can also be applied in the direct torque control system, with output frequency of 250 Hz and output voltage of 6.9 kV. However, the disadvantage is that with the increase of the number of levels, the number of clamping diodes required also increases sharply, and in order to avoid DC connection short circuit, each H-bridge needs an independent DC source [13], which increases the complexity of the whole system. In reference [14], this kind of hybrid HNPC inverter was studied. In order to improve the current output capability of the HNPC inverter, the idea of two-stage parallel connection of devices and units was adopted, and it was successfully applied in the field of electromagnetic launch.

3.2 Active Neutral-Point-Clamped (ANPC)

In 3L-NPC topology, in order to control the problem of power distribution, and overcome the limitation of DC-link capacitor voltage imbalance, the ANPC is used. All the commutation modes of the ANPC can be used in the new medium-voltage inverter. Another common structure is the 5L-ANPC [15], as shown in Fig. 5. This topology effectively increases the level number of the inverter by adding flying capacitor units, and modularizes the NPC. It solves the problem of capacitor voltage imbalance, and improves the rated power, but correspondingly increases the number of devices, also introduces more switching loss and on-state loss. At present, ABB has developed mature products based on 5L-ANPC topology, such as ACS2000 series. The circuit structure is shown in Fig. 6. Its power level covers 400–1000 kVA and its output voltage is 6.0–6.9 kV.

3.3 Transistor-Clamped H-Bridge (TCHB)

The concept of transistor clamped inverter is similar to that of diode clamped inverter, which provides current path for clamped devices through bidirectional switch. Like the NPC, there is a fully controlled neutral clamped point in the case of three-level, so this topology is also called neutral point controlled inverter, which can work in medium voltage (3.3 kV, 6.6 kV and 9.9 kV) and 48 MW high-power occasions [16]. The switching device can work at a higher frequency by equipping the loss, which effectively improves the maximum output frequency. In reference [17], a three-phase cascaded multilevel inverter is proposed, as shown in Fig. 7(a), which is composed of the five-level transistor-clamped H-bridge unit shown in Fig. 7(b). Multi carrier phase shifted pulse width modulation (CPS-PWM) is used. Experimental results show that compared with the classic inverter, this topology can achieve higher output quality and lower power loss, so it is more suitable for the drive system of high-speed electric locomotive.

4 Modulation Methods of Multilevel Inverter

Pulse width modulation (PWM) is a technology that modulates the pulse width of the switching signal, transforms the DC voltage into a certain shape of voltage pulse sequence by controlling the power switching device, so as to control the frequency and amplitude of the output voltage, and effectively suppress or eliminate harmonics. It is pointed out in reference [18] that the quality of a modulation method is mainly evaluated from the

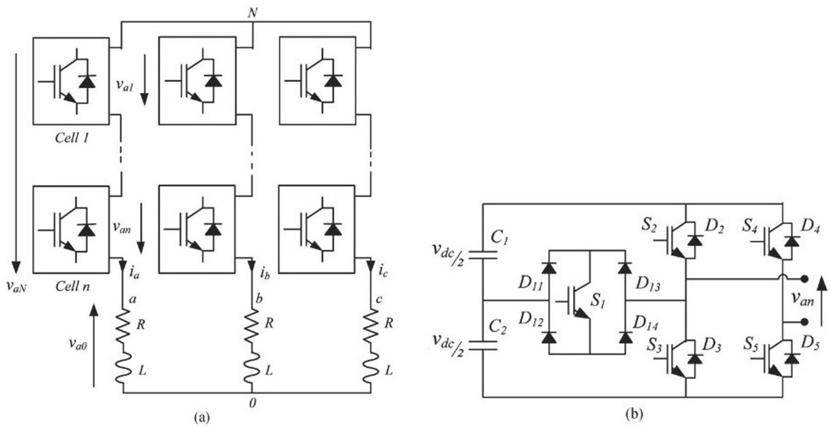

Fig. 7. TCHB: (a) general configuration of the proposed three-phase cascaded multilevel inverter and (b) topology of five-level transistor-clamped H-bridge for each cell.

aspects of current harmonics, switching frequency, torque ripple, sampling frequency and dynamic performance.

In the research of multilevel inverter, modulation technique is very important, which is inseparable from the research of topology. Multilevel modulation methods not only determines whether the inverter function is realized or not, but also have a decisive impact on the output waveform quality, and efficiency of the inverter.

The carrier-based sinusoidal PWM (SPWM) generally uses isosceles triangle as carrier wave and sine as modulation wave. The typical multilevel modulation methods can be divided into level-shifted PWM (LS-PWM) and phase-shifted PWM (PS-PWM) techniques. The SVPWM, LS-PWM and PS-PWM are the three most classic PWM techniques in multilevel inverter [19, 20].

4.1 Space Vector Pulse Width Modulation (SVPWM)

The SVPWM is an advanced and efficient modulation technique proposed by Joachim Holtz in 1980s. The difference between SVPWM and SPWM is that the SPWM focuses on the output of sinusoidal voltage waveform, while the SVPWM is based on the space vector of voltage, which can obtain the circular rotating magnetic field required by the motor and generate constant torque. Therefore, the SVPWM technique has low harmonics, high torque stability and high utilization rate of voltage.

The SVPWM technique is based on the working characteristics of AC motor, focusing on how to make AC motor obtain a constant amplitude circular magnetic field, namely sinusoidal flux linkage. The actual flux linkage generated by different switching modes of inverter is used to approximate the reference circular flux linkage, and the switching state of inverter is determined by their comparison results, forming PWM output voltage waveform [21]. In this method, the excitation method of the motor and the on-off condition of the power switch in the inverter are treated as a unified whole. Therefore, this method is widely used in open-loop and closed-loop systems.

However, the SVPWM technique also has its shortcomings. In N-level inverter, the switching state of power switch is N3, and in five-level and above multilevel inverter, there are many switching states, so the control is extremely complex [22]. In the CHB inverter, the number of output voltage levels is at least five. Therefore, the traditional SVPWM technique is not suitable for the inverter with a higher number of levels.

4.2 Level-Shifted Pulse Width Modulation (LS-PWM)

The basic principle of LS-PWM is: in the M-level inverter, M-1 triangular carriers with the same frequency and amplitude are vertically placed on the upper and lower sides of the coordinate axis, and compared with the same modulation wave. According to the comparison results, the trigger signal of the corresponding switching device is obtained. The LS-PWM mainly includes three types of disposition [23].

(1) The phase disposition (PD) modulation strategy with the same carrier phase is shown in Fig. 8(a), where *Ac* is the triangular carrier amplitude.
(2) The phase opposite disposition (POD) modulation strategy is shown in Fig. 8(b).
(3) The alternative phase opposite disposition (APOD) modulation strategy is shown in Fig. 8(c).

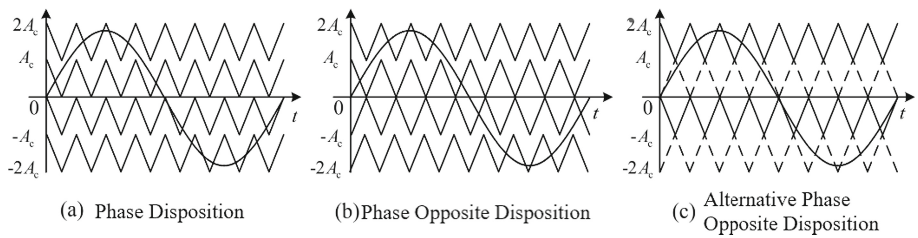

Fig. 8. Five-level LS-PWM

The equivalent switching frequency of multilevel inverter using this kind of modulation method is higher, and it has excellent harmonic characteristics. The system not only has good linearity, but also has a wide transmission bandwidth. However, this kind of modulation method will lead to the unbalanced conduction load of the switching devices in the inverter, especially in deep modulation.

4.3 Phase-Shifted PWM (PS-PWM)

The carrier phase shifted PWM (CPS-PWM) is a modulation method for cascaded inverters with the same inverting unit. The basic principle is that the modulation wave between the cascaded units in the same phase is the same, and the PWM pulse output by each unit is staggered in the horizontal direction by the carrier phase shift. Finally, the multilevel PWM wave is output by using the waveform superposition principle in the multiplexing technology, so that the equivalent switching frequency of the inverter can be improved [24], among which the most representative is the sinusoidal modulation wave CPS-SPWM technique.

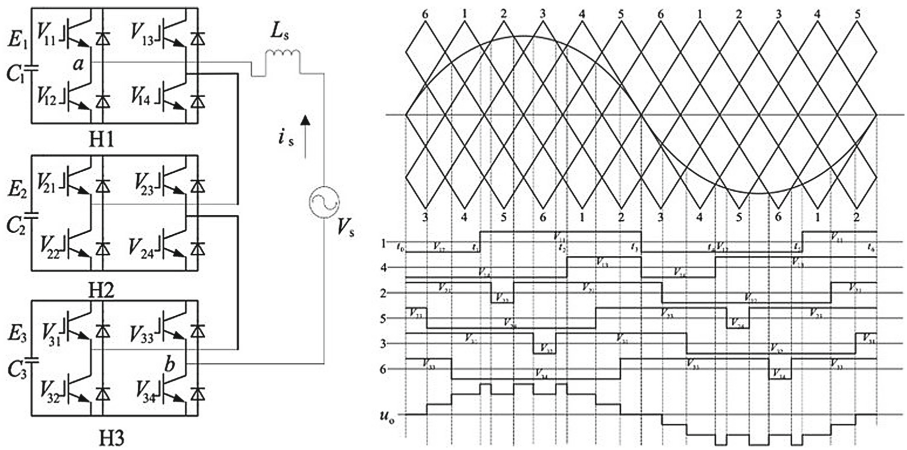

Fig. 9. Seven-level CPS-SPWM

The cascaded multilevel inverter with this modulation method greatly reduces the output harmonics without increasing the switching loss of the device, significantly improves the quality of the output waveform, solves the contradiction between the power processing ability of the switching device and the switching frequency, and completes the power conversion in the high-voltage field with the low-voltage IGBT, so it has been widely used in the high-voltage and high-power field [25]. Because the modulation method of each unit of cascaded inverter is only different in carrier or modulation wave phase, it is more convenient to realize and easy to expand to multilevel. Taking the single-phase seven-level cascaded H-bridge inverter as an example, as shown in Fig. 9, the CPS-SPWM technique is adopted. The six carriers are shifted 360°/6 in turn, then compared with the sinusoidal modulation wave respectively. Finally, the multi-level PWM wave is obtained after the superposition of three H-bridge output waveforms.

4.4 Optimized Modulation Methods

It is pointed out in reference [26] that SIEMENS uses optimal PWM signal generation method, which has the advantages of less calculation, less harmonic, less impact on the neutral point voltage, meeting the minimum pulse width limit, etc., and meets the nearest three vector synthesis method under all working conditions. Firstly, the voltage vector and phase angle in the control system are converted into three-phase voltage, and then the zero-sequence component is superimposed on the three-phase voltage, that is, a certain third harmonic is injected into the sinusoidal modulation wave to reduce the THD of harmonics, improve the quality of output waveform, and improve the utilization rate of voltage.

In reference [27], it is pointed out an optimized method of pulse width modulation (Chaotic Sinusoidal Pulse Width Modulation) which is based on the basic theory of chaos and traditional carrier SPWM method. Chaotic sequence is a non-periodic bounded sequence. It is found that if the carrier frequency is changed by chaotic sequence, the switching frequency can be changed. The switching period can be changed in a certain range. The spectrum can be distributed in a wide frequency domain. The peak value of harmonic can be reduced. The energy of harmonics can be well-distributed, and the electromagnetic compatibility (EMC) of the circuit can be improved.

The central 60° synchronous modulation is a modulation strategy developed on the basis of SPWM, which has the characteristics of high utilization rate of DC voltage, symmetry waveform and low switching frequency. It is often used for the transition from synchronous modulation to square wave modulation in electric locomotive driving system [28].

In reference [29], an optimized algorithm based on GH coordinate system is proposed to solve the problem that the calculation difficulty of SVPWM increases with the increase of the number of levels, which saves the trigonometric function operation in the process of sector judgment and vector action time calculation in traditional SVPWM algorithm. The voltage space vector in rectangular coordinate system is transformed into the vector in GH coordinate system. The vector of each reference voltage is an integer, and there is no calculation of trigonometric function for vector action time. Compared with the traditional SVPWM algorithm, this algorithm has higher computing speed and reduces the actual computing time.

In reference [30], through the analysis of single-phase cascaded H-bridge Neutral-Point-Clamped inverter's switch states, 27 useful switch vectors are obtained. A novel space vector pulse width modulation (SVPWM) method for this nine-level inverter was proposed. The algorithm has the advantages of less computation and easy digital implementation, and can effectively control the balance of capacitor voltage.

In reference [31], it is proposed a harmonic suppression method based on predictive control, which is also implemented online, but the amplitude of each harmonic is considered in real time due to the sliding discrete Fourier transform. The prediction model is used to select switching states to minimize all expected harmonics. The prediction model, together with the sliding discrete Fourier transform, allows this modulation method to be used in closed-loop operation, which has higher dynamic performance.

5 Development Trend of Multilevel Inverter

The introduction of a higher number of levels can essentially improve the quality of multilevel waveform, so the pursuit of a higher number of levels of multilevel inverter has become the direction of future development. Another development direction of multilevel technology is to reduce the volume and mass of inverter.

The switching loss of multilevel inverter still exists, and this part depends on the modulation method. Therefore, for a given topology, it is necessary to reduce the switching loss by optimizing the modulation method and design parameters [32]. In addition to on-state loss and switching loss, the effect of harmonics generated by inverter on efficiency should also be considered. The harmonic losses at the motor and grid sides depend on both the topology and the modulation method. With the continuous development of high and new technology and the increasing demand for reducing the harmonics of inverter output current and voltage, the research on harmonics control technology of multilevel inverter is gradually developed and improved.

Reliability is also a key factor in the future development of multilevel inverters. Some multilevel topologies improve the system fault tolerance margin by adding some hardware, so that the system can operate under fault conditions. As a new technology, predictive control has been applied in the field of multilevel inverter. In reference [33], a model predictive current control (MPCC) strategy is proposed, which uses predictive controller instead of modulator and linear controller to avoid the generation of load side control current. It solves the problem of capacitor voltage imbalance in NPC inverter and reduce the number of commutation, so it is a very promising technology.

It is pointed out in reference [34] that there are two different trends in the development of multilevel inverters: the first is to use simpler circuit structures (such as NPC, ANPC, H-NPC, etc.), and higher rated devices such as IGCT can be used to achieve medium-voltage. The second is the use of modular structure, which is more complex in structure (such as CHB, FC and MMC), but can use IGBT and other lower rated devices to achieve high voltage through series inverting unit. These two methods have their own advantages and will coexist in different application fields in the next few years. On the other hand, the development of mature silicon carbide (SiC) devices can greatly reduce the switching loss, which will be conducive to the penetration of multilevel inverters in industrial applications.

6 Summary

In recent years, a variety of new multilevel inverter topologies and their modulation methods make it more widely used. This paper summarizes the common multilevel topologies and modulation methods, which provides a valuable reference for the industrial application. At the same time, the development trend and direction of multilevel inverter in the future are predicted. With the continuous innovation and application of multilevel inverter topologies, it is necessary to make continuous breakthroughs in modulation techniques, control schemes and development of new power electronic devices in the future to further improve the performance of multilevel inverters.

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Rotor Broken Bar Fault Diagnosis for Induction Traction Motor Considering Low Load Condition

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Abstract. Rotor broken bar fault accounts for more than 5% in induction motor faults. The frequencies $(1 \pm 2s)f_1$ in motor current are recognized as the fault characteristics to detect the fault. However, when the traction motor works under light load, e.g., idling condition, the fault diagnosis algorithm will be invalid as the characteristic frequency approaches to the fundamental frequency f_1. In this paper, a low frequency injection algorithm is adopted to detect the rotor broken bar fault for an induction traction motor under the low load condition. Firstly, the fault characteristic frequency generated by the injected voltage is analyzed. Then the selection of the injected voltage frequency is discussed, and the implementation of the low-frequency voltage injection algorithm for the motor is developed. Finally, the proposed method is validated through the experiment results.

Keywords: Rotor broken bar fault · Traction motor · AC voltage injection · Low load

1 Introduction

Induction motors are widely-used in railway traction applications. According to [1], rotor broken bar fault account for about 5% in induction motor faults. If the early rotor bar fault is not detected in time, it will gradually spread and eventually lead to irreparable failure, which will not only bring economic losses, but also endanger life safety. Therefore, the detection of rotor broken bar fault is of great significance to guarantee the train reliability and safety.

Rotor broken bar fault may be caused by inherent defects such as bubbles in rotor bars in cast rotors, or poor welding between rotor bars and end rings in assembled rotors. In early stage, the degradation of rotor broken bar fault will be present as an exponential function of time. The adjacent rotor bars will replace the broken rotor bar to bear excessive current stress, and thus the fault will spread to adjacent area, leading to gradual deterioration and shorting motor life. Moreover, when rotor broken bar fault occurs, the average output torque of the motor will be reduced, leading to slower system acceleration and longer starting time.

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At present, a lot of research for the detection of rotor broken bar fault has been done. The time domain, frequency domain and time-frequency domain base on the motor current signal analysis (MCSA) are very popular, where the frequencies of $(1 \pm 2s)f_1$ in the motor current (where s is the slip rate and f_1 is the fundamental frequency) are recognized as the characteristics. Initially the motor current was analyzed by FFT [2]. However, when it was used to detect the rotor fault, the spectrum leakage [3] of FFT will lead to the characteristics to be inconspicuous because small slip frequency makes the characteristics close to the fundamental to be submerged. Hence the methods of adding windows [4] are proposed to reduce the influence of spectrum leakage. Furthermore, filtering [5] was used to remove the fundamental component to avoid the influence of spectrum leakage. Moreover, the frequency resolution of FFT is heavily dependent on the length of sampled data, whereas the data length is limited due to the memory of the processor in practice. Consequently, the estimation of signal parameters via rotational invariance technique (ESPRIT) [6, 7], multiple signal classification (MUSIC) [8, 9], ROOT-MUSIC [8], ZOOM MUSIC [3, 9], and other high-resolution spectral algorithms are developed for rotor fault diagnosis.

The characteristics of rotor broken bar fault in motor current are highly dependent on the slip frequency. For an induction traction motor, when the motor works under the idling condition, the slip frequency is close to zero ($s \approx 0$). Consequently, the fault components caused by rotor broken bar fault almost coincidence with the fundamental, leading to the failure of the fault diagnosis method.

In order to solve this problem, a rotor broken bar fault diagnosis method based on the low-frequency voltage injection is proposed in this paper. The rest of this paper is organized as: Sect. 2 introduces the proposed rotor fault diagnosis method under idling condition, where the fault characteristics caused by the injected low frequency voltage are analyzed and the implementation of low frequency voltage injection method for a traction inverter is introduced; Sect. 3 shows the experimental results; in Sect. 4, the conclusion is present.

2 Rotor Broken Bar Fault Diagnosis Under Low Load Condition

When a rotor broken bar fault occurs, it will induce the fault frequencies of $(1 \pm 2s)f_1$ in motor current [10]. According to the above introduction, the fault components almost overlaps with the corresponding fundamental or harmonics when it works under low load condition ($s \approx 0$), leading to the failure of the fault diagnosis method using the traditional MCSA. Next a fault diagnosis method based on the AC voltage injection method is proposed.

2.1 Rotor Broken Bar Fault Diagnosis Method Based on the Low Frequency Voltage Injection

If an AC voltage is injected into a rotor broken bar fault motor, it will produce fault components in motor current. Here it assumes that the frequency of the injected AC voltage is f_{ac}, and the frequency $f_{ac,r}$ induced in rotor is:

$$f_{ac,r} = f_{ac} - f_r \tag{1}$$

Where f_r is the rotor frequency. Rotor broken bar fault leads to rotor asymmetry, so it will produce negative sequence current whose frequency is $f_{ac,r,brb}$ in rotor.

$$f_{ac,r,brb} = -(f_{ac} - f_r) \tag{2}$$

Next, the fault characteristic frequency $f_{ac,brb}$ induced by the above components in stator current is

$$f_{ac,brb} = -f_{ac} + 2f_r \tag{3}$$

Therefore, the injected AC signal will produce a fault characteristic frequency of $(-f_{ac} + 2f_r)$ in motor current, where the fault frequency is the difference between the injected AC signal frequency f_{ac} and $2f_r$. It shows that the characteristic depends on the injected voltage frequency and rotor speed. When choosing the value of injected voltage frequency, the following points should be considered:

(1) The frequency cannot be high. The switching frequency of the traction inverter is low (≤1 kHz) [11], and thus high voltage frequency will lead to the distortion of the output voltage.
(2) $(-f_{ac} + 2f_r) \neq 0$, i.e., $f_{ac} \neq 2f_r$.
(3) $(-f_{ac} + 2f_r) \neq f_1$, i.e., $f_{ac} \neq (2f_r - f_1)$.

Therefore, here it chooses the low voltage frequency to be injected into the motor in this paper, which satisfies the above (1)~(3).

2.2 Implementation of the Low Frequency Injection Algorithm

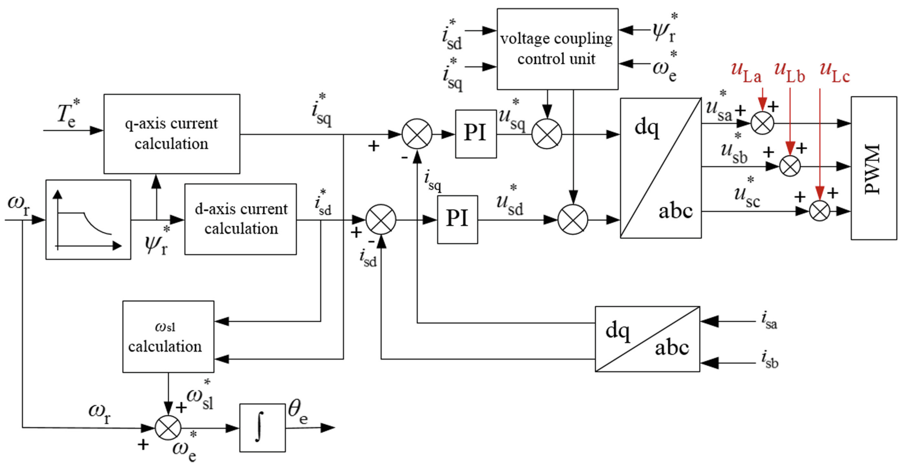

Fig. 1. Principle diagram of the low-frequency voltage injection method

As shown in Fig. 1, it superposes low-frequency voltages u_{La}, u_{Lb}, u_{Lc} into the three-phase voltage $u_{sa}{}^{*}$, $u_{sb}{}^{*}$, $u_{sc}{}^{*}$ as eventual voltage references to the PWM block, where the injected low-frequency voltage u_{La}, u_{Lb}, u_{Lc} are defined as:

$$u_{La} = \begin{cases} U_L \cos(\omega_L t) \\ u_{Lb} = U_L \cos(\omega_L t - 2\pi/3) \\ u_{Lc} = U_L \cos(\omega_L t + 2\pi/3) \end{cases} \quad (4)$$

Where U_L is the amplitude and ω_L is the angular frequency of the injected voltage respectively ($\omega_L = 2\pi f_L, f_L$ is the injected low frequency voltage). On this basis, the rotor broken bar fault can be detected through the extraction of the fault frequency ($-f_L + 2f_r$) in motor current.

3 Experiments Results

Experiments are performed on the ground platform for motor fault diagnosis, as shown in Fig. 2, where the basic framework includes a three-phase voltage source, an auto transformer, a rectifier, and an inverter. The load of the tested motor is imposed through a DC generator that coupled with the induction motor, where the energy produced by the generator is consumed on a load resistance. The test motor is shown in Fig. 3.

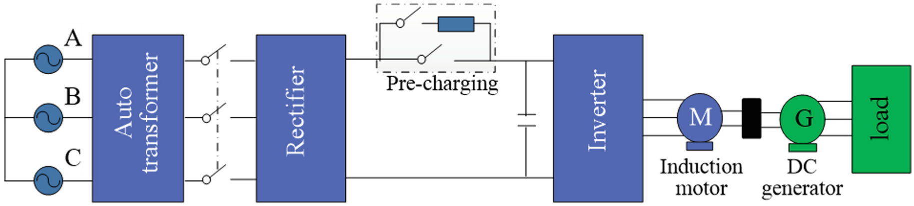

Fig. 2. Schematic diagram of the experimental platform for motor fault diagnosis

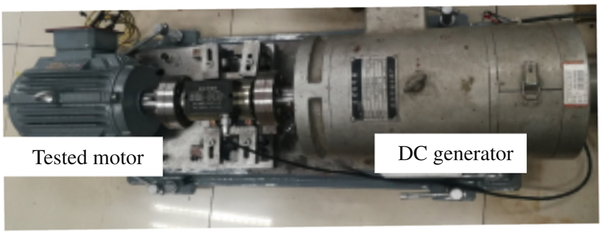

Fig. 3. Photo of the test motor of the experimental platform

Health and fault rotors were replaced and installed in the tested motor. Here both one bar broken and three bars broken rotors are designed and produced, as shown in Fig. 4.

In the test, the motor works in no-load condition (s is very small), and the low frequency voltage is injected to the motor to detect the rotor broken bar fault. The FFT