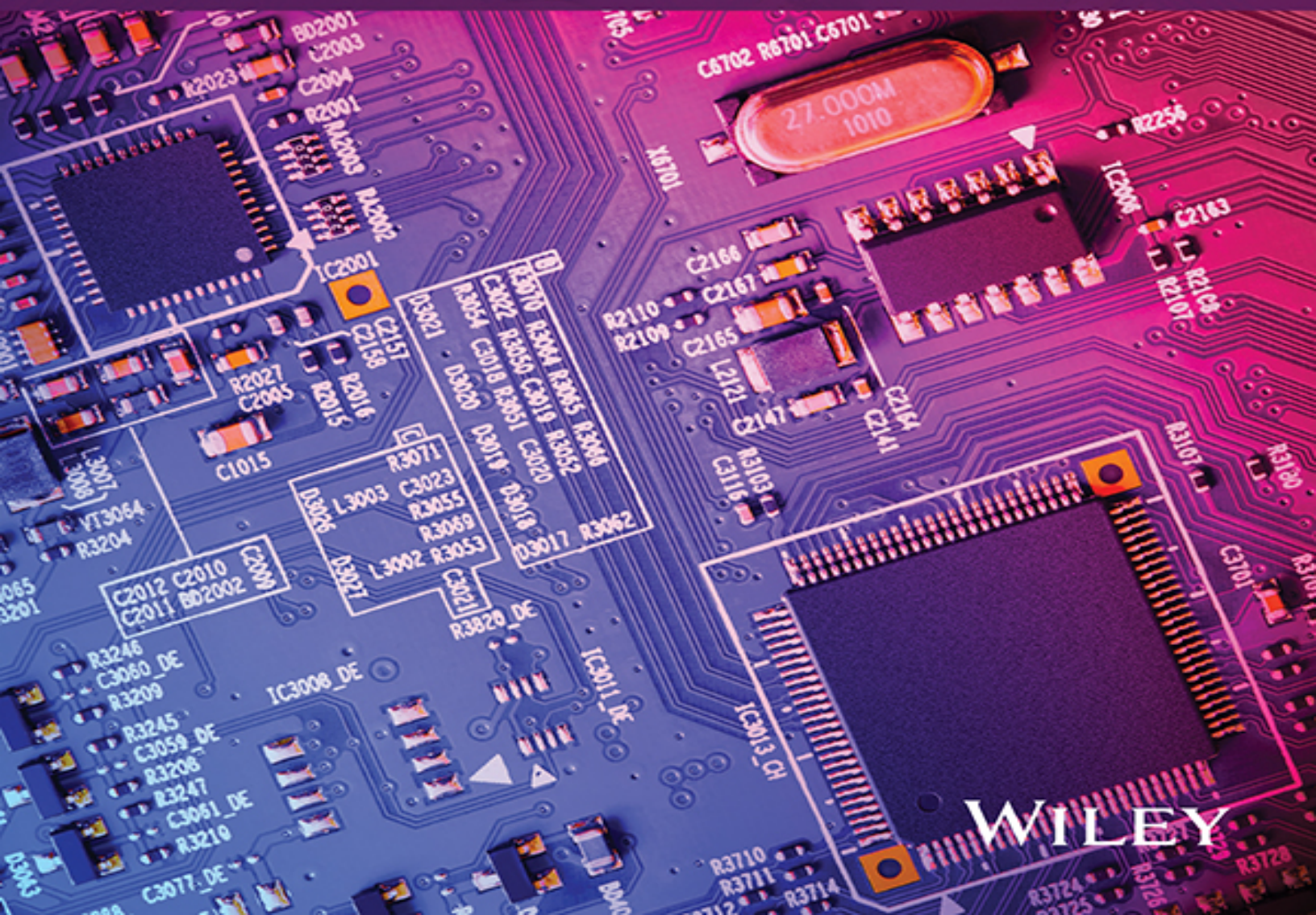


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DIGITAL VLSI DESIGN AND SIMULATION WITH VERILOG



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Digital VLSI Design and Simulation with Verilog

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Preface

Integrated circuits are now growing in importance in every electronic system that needs an efficient VLSI architecture design with low-power consumption, a compact chip area, speed, and operating frequency. The challenge for VLSI system designers is to optimize hardware-software integration for lowering the total cost of product acquisition. So, there is a demand for better technological solutions for advanced VLSI architectures that can be done through hardware description language (HDL). Verilog HDL is one of the programming languages that can provide better solutions in this new era of the VLSI industry. The prefabrication design and analysis of such advanced VLSI architecture can easily be implemented with Verilog HDL using available software tools such as Xilinx and Cadence.

This book mainly deals with the fundamental concepts of digital design along with their design verification with Verilog HDL. It will be a common source of knowledge for beginners as well as research-seeking students working in the area of VLSI design, covering fundamentals of digital design from switch level to FPGA-based implementation using hardware description language (HDL).

The book is summarized in 10 chapters. [Chapters 1](#) and [2](#) describe the fundamental concepts behind digital circuit design including combinational and sequential circuit design. [Chapters 3](#) to 8 focus on sequential and combinational circuit design using Verilog HDL at different levels of abstraction in Verilog coding. [Chapter 9](#) includes implementation of any logic function using a programmable logic device such as PLD, CPLD, FPGA, etc. [Chapter 10](#) covers a few real-time examples of digital circuit design using Verilog. [Chapter 11](#) focuses on System Verilog,

distinct features, comparing Verilog and System Verilog with design example.

About the Authors

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1

Combinational Circuit Design

This chapter describes the combinational logic circuits design and their implementation with logic gates, multiplexers, decoders, etc. Combinational circuits are the major block of any digital design or function [1]. So, a detailed overview before the design and analysis of digital circuit with Verilog modules, plays a significant role in hardware optimization to achieve the desired outcomes.

1.1 Logic Gates

Logic gates are very useful when performing a few basic operations in any digital computer system. These logic gates perform many operations in complex circuits and other control systems, e.g., basic operations like AND, OR, and NOT. The functionality of each basic gate as well as the extended version are discussed in this chapter.

AND operation:

It performs the AND operation. The circuit diagram of the N input AND operation is shown in [Figure 1.1](#).

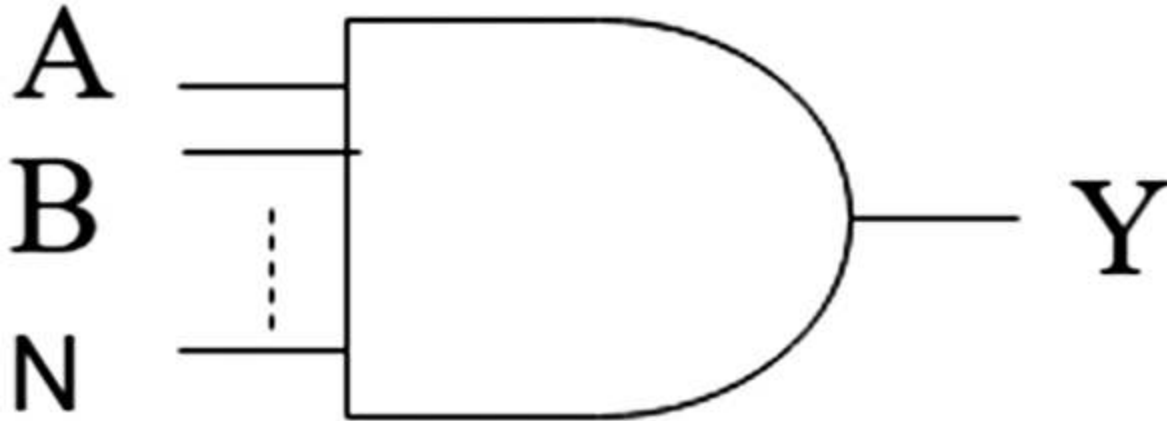


Figure 1.1 Symbol of an AND gate.

The AND gate may have N number of inputs and one output. If the number of inputs are N then $N \geq 2$ conditions must be applied for input operation. Digital inputs are applied in terms of A, B, C.....N, and the output is Y.

The mathematic equation is given below:

$$\begin{aligned}
 Y &= A \text{ AND } B \text{ AND } C \text{ AND } D \dots\dots\dots \text{AND } N \\
 &= A.B.C.D \dots\dots N \\
 &= ABCD \dots\dots N
 \end{aligned}$$

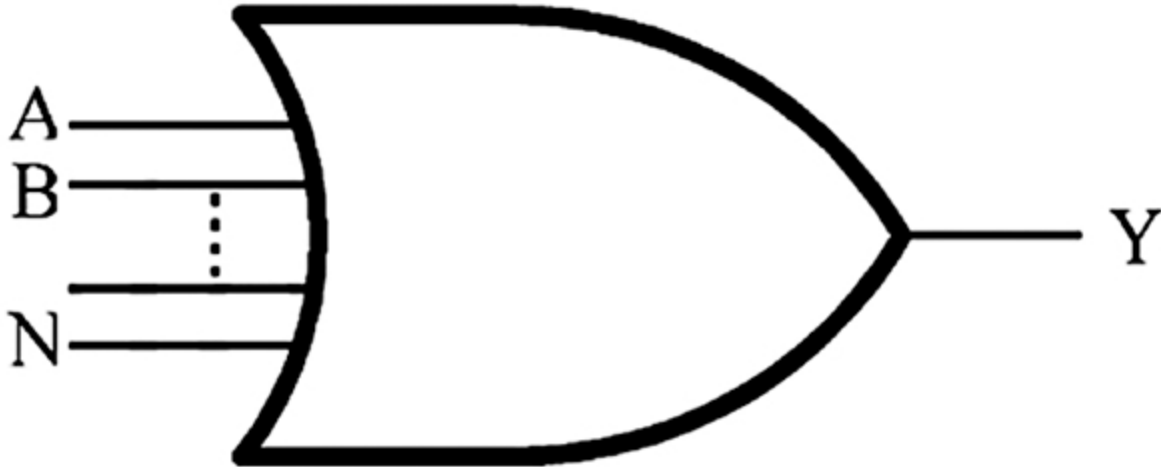
The truth table for an AND gate is provided in [Table 1.1](#)

Table 1.1 T. Table of AND gate.

I/P		O/P
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR operation:

It performs OR operation. The symbol for an OR operation is shown in [Figure 1.2](#).



[Figure 1.2](#) Symbol for an OR gate.

The OR gate may have N number of inputs and one output. If the number of inputs are N then $N \geq 2$ conditions must be applied for input operation. Digital inputs are applied in terms of A, B, C.....N, and the output is Y.

The mathematic equation is given below:

$$Y = A \text{ OR } B \text{ OR } C \text{ OR } D \dots\dots\dots \text{ OR } N$$
$$= A + B + C + D \dots\dots\dots + N$$

The truth table for an OR gate is provided in [Table 1.2](#) .