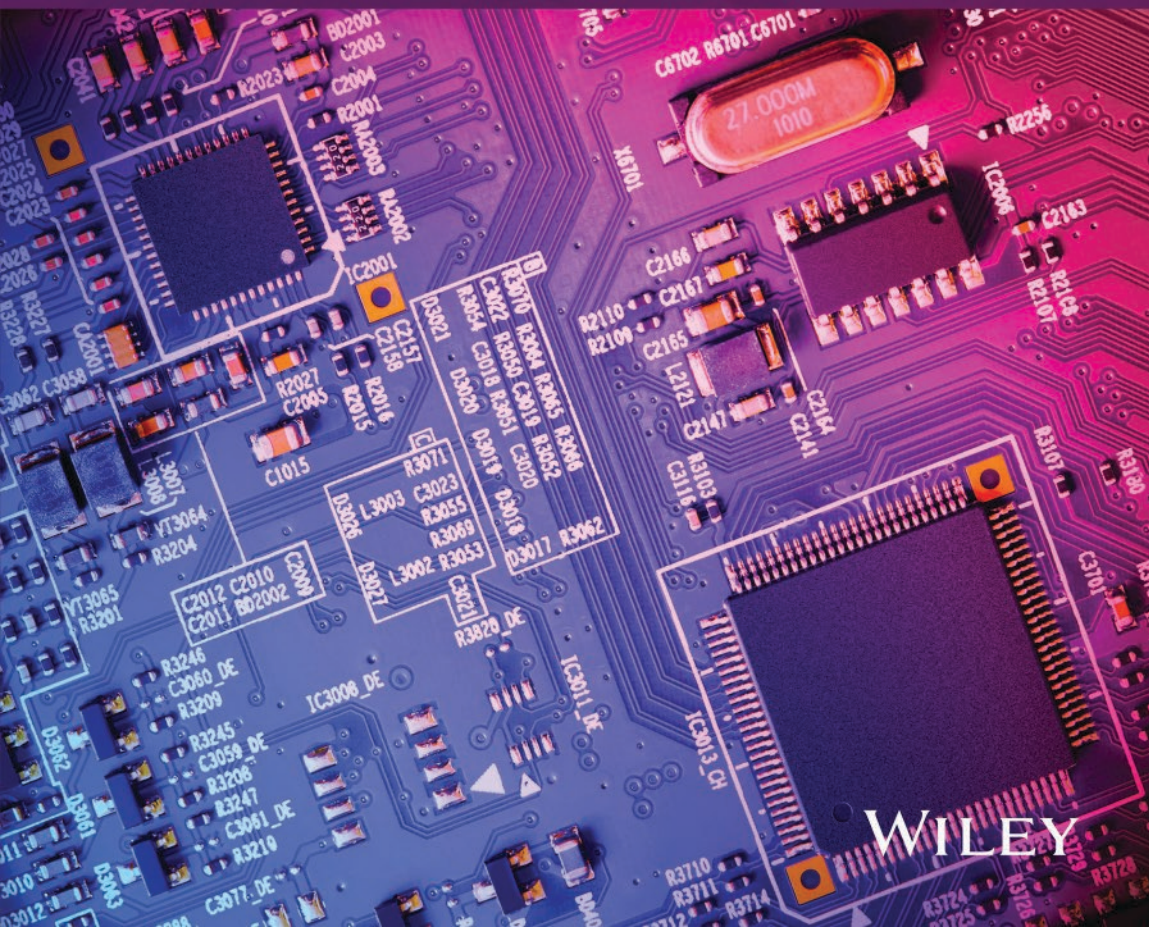
SUMAN LATA TRIPATHI • SOBHIT SAXENA
SANJEET K. SINHA • GOVIND S. PATEL

DIGITAL VLSI DESIGN AND SIMULATION WITH VERILOG



Digital VLSI Design and Simulation with Verilog

Digital VLSI Design and Simulation with Verilog

Dr. Suman Lata Tripathi
Lovely Professional University, Phagwara, Punjab, India

Dr. Sobhit Saxena
Lovely Professional University, Phagwara, Punjab, India

Dr. Sanjeet Kumar Sinha
Lovely Professional University, Phagwara, Punjab, India

Dr. Govind Singh Patel
IIMT College of Engineering, Greater Noida, UP, India

WILEY

This edition first published 2022

Registered Office
John Wiley & Sons, Inc., 111 River Street, Hoboken, NJ 07030, USA

Editorial Office
9600 Garsington Road, Oxford, OX4 2DQ, UK

For details of our global editorial offices, customer services, and more information about Wiley products visit us at www.wiley.com.

Wiley also publishes its books in a variety of electronic formats and by print-on-demand. Some content that appears in standard print versions of this book may not be available in other formats.

Library of Congress Cataloging-in-Publication Data
Names: Tripathi, Suman Lata, author. | Saxena, Sobhit, author. | Sinha, Sanjeet Kumar, author. | Patel, Govind Singh, author.
Title: Digital VLSI design and simulation with Verilog / Suman Lata Tripathi, Sobhit Saxena, Sanjeet Kumar Sinha, Govind Singh Patel.
Description: Hoboken, NJ : John Wiley & Sons, 2022. | Includes bibliographical references and index.
Identifiers: LCCN 2021020790 (print) | LCCN 2021020791 (ebook) | ISBN 9781119778042 (hardback) | ISBN 9781119778066 (pdf) | ISBN 9781119778080 (epub) | ISBN 9781119778097 (ebook)
Subjects: LCSH: Integrated circuits--Very large scale integration--Design and construction. | Verilog (Computer hardware description language)
Classification: LCC TK7874.75 .T75 2022 (print) | LCC TK7874.75 (ebook) | DDC 621.39/5028553--dc23
LC record available at https://lccn.loc.gov/2021020790
LC ebook record available at https://lccn.loc.gov/2021020791

Cover image: © Raigvi/Shutterstock
Cover design by Wiley

Set in 9.5/12.5 STIXTwoText by Integra Software Services Pvt. Ltd, Pondicherry, India

10 9 8 7 6 5 4 3 2 1

Contents

Preface

Integrated circuits are now growing in importance in every electronic system that needs an efficient VLSI architecture design with low-power consumption, a compress chip area, speed, and operating frequency. The challenge for VLSI system designers is to optimize hardware-software integration for lowering the total cost of product acquisition. So, there is a demand for better technological solutions for advanced VLSI architectures that can be done through hardware description language (HDL). Verilog HDL is one of the programming languages that can provide better solutions in this new era of the VLSI industry. The prefabrication design and analysis of such advanced VLSI architecture can easily be implemented with Verilog HDL using available software tools such as Xilinx and Cadence.

This book mainly deals with the fundamental concepts of digital design along with their design verification with Verilog HDL. It will be a common source of knowledge for beginners as well as research-seeking students working in the area of VLSI design, covering fundamentals of digital design from switch level to FPGA-based implementation using hardware description language (HDL).

The book is summarized in 10 chapters. Chapters 1 and 2 describe the fundamental concepts behind digital circuit design including combinational and sequential circuit design. Chapters 3 to 8 focus on sequential and combinational circuit design using Verilog HDL at different levels of abstraction in Verilog coding. Chapter 9 includes implementation of any logic function using a programmable logic device such as PLD, CPLD, FPGA, etc. Chapter 10 covers a few real-time examples of digital circuit design using Verilog. Chapter 11 focuses on System Verilog, distinct features, computing Verilog and System Verilog with design example.

About the Authors

Dr. Suman Lata Tripathi completed her PhD in the area of microelectronics and VLSI from Motilal Nehru National Institute of Technology, Allahabad. She obtained her M.Tech in Electronics Engineering from Uttar Pradesh Technical University, Lucknow and B.Tech in Electrical Engineering from Purvanchal University, Jaunpur. She is associated with Lovely Professional University as a Professor with more than 17 years of experience in academics. She has published more than 55 research papers in refereed IEEE, Springer, and IOP science journals and conferences. She has organized several workshops, summer internships, and expert lectures for students. She has worked as a session chair, conference steering committee member, editorial board member, and reviewer in international/national IEEE/Springer Journal and conferences. She received the "Research Excellence Award" in 2019 at Lovely Professional University. She received the best paper at IEEE ICICS-2018. She has edited more than 12 books/1 book series in different areas of electronics and electrical engineering. She is associated with editing work for top publishers including Elsevier, CRC, Taylor and Francis, Wiley-IEEE, SP Wiley, Nova Science, and Apple Academic Press. She also works as series editor for, "Smart Engineering Systems" CRC Press, Taylor and Francis. She is associated as a senior member IEEE, Fellow IETE and Life member of ISC and is continuously involved in different professional activities along with her academic work. Her area of expertise includes microelectronics device modeling and characterization, low-power VLSI circuit design, VLSI design of testing, and advance FET design for IoT, Embedded System Design and biomedical applications etc.

Dr. Sobhit Saxena completed his PhD at "IIT Roorkee" from the Metallurgical & Materials Engineering Department. He has designed a new hybrid system of Li-ion battery and supercapacitor for energy storage applications. He worked as SEM (Scanning Electron Microscopy) operator for 4 years under the MHRD fellowship. He obtained his M.Tech in VLSI from Shobhit University, Meerut

and B.E. from MIT Moradabad in Electronics and Communication Engineering. He has vast teaching experience of more than 10 years in various colleges and universities. Currently, he is working as Associate Professor in the School of Electronics and Electrical Engineering, Lovely Professional University. He has been awarded the "Perfect Award" four times consecutively (2007–2010) for achieving 100% results. He has published around 12 research papers in SCI-indexed journals and reputed international conferences held at different IITs. His area of expertise includes nanomaterial synthesis and characterization, electrochemical analysis and modeling and simulation of CNT based interconnects for VLSI circuits.

Dr. Sanjeet Kumar Sinha completed a doctoral program in the Department of Electrical Engineering of the National Institute of Technology (NIT) Silchar. He obtained his M.Tech in Microelectronics and VLSI Design from NIT Silchar**.** He is associated with Lovely Professional University as an Associate Professor with more than 10 years of experience in academia. Over the years, he has developed an innovative approach to teaching and conducting research with undergraduates through creating and presenting course materials in both laboratory and classroom settings. He has published around 35 research papers in refereed journals/conferences including Elsevier, IEEE transaction, etc. He has published book chapters in Elsevier, Taylor & Francis, etc. His area of expertise includes microelectronics device modeling and characterization, low-power VLSI circuit design, VLSI design of testing, fabrication & characterization of CNT FET, etc.

Dr. Govind Singh Patel received his Masters degree in Instrumentation & Control Engineering from MD University, Rohtak, India. He has studied and been awarded a PhD in Electronics and Communication Engineering from Thapar University, Patiala, India. He is working as Professor in the Department of Electronics and Communication Engineering, IIMT Engineering College, Greater Noida, UP, India. He has published more than 62 papers in National and International Journals. He has also filed four Indian patents. His area of expertise includes VLSI signal processing, communication systems, low-power VLSI circuit design, VLSI design &testing and advance electronics, design for IoT, and agriculture applications. His one book titled "Smart Agriculture: Deep Learning, Machine Learning and IoT" is in the process of publication with CRC Taylor and Francis.

1

Combinational Circuit Design

This chapter describes the combinational logic circuits design and their implementation with logic gates, multiplexers, decoders, etc. Combinational circuits are the major block of any digital design or function [1]. So, a detailed overview before the design and analysis of digital circuit with Verilog modules, plays a significant role in hardware optimization to achieve the desired outcomes.

1.1 Logic Gates

Logic gates are very useful when performing a few basic operations in any digital computer system. These logic gates perform many operations in complex circuits and other control systems, e.g., basic operations like AND, OR, and NOT. The functionality of each basic gate as well as the extended version are discussed in this chapter.

AND operation:
It performs the AND operation. The circuit diagram of the N input AND operation is shown in Figure 1.1.

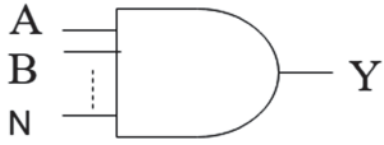


Figure 1.1 Symbol of an AND gate.

Digital VLSI Design and Simulation with Verilog, First Edition. Suman Lata Tripathi, Sobhit Saxena, Sanjeet Kumar Sinha, and Govind Singh Patel.

The AND gate may have N number of inputs and one output. If the number of inputs are N then N ≥ 2 conditions must be applied for input operation. Digital inputs are applied in terms of A, B, C.....N, and the output is Y.

The mathematic equation is given below:

$$Y = A \text{ AND } B \text{ AND } C \text{ AND } D \ldots\ldots\ldots \text{AND } N$$
$$= A.B.C.D \ldots\ldots N$$
$$= ABCD \ldots\ldots N$$

The truth table for an AND gate is provided in Table 1.1

Table 1.1 T. Table of AND gate.

I/P		O/P
A	**B**	**Y**
0	0	0
0	1	0
1	0	0
1	**1**	**1**

OR operation:

It performs OR operation. The symbol for an OR operation is shown in Figure 1.2.

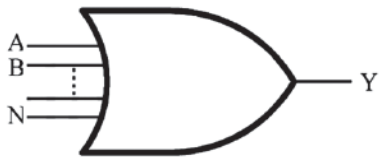


Figure 1.2 Symbol for an OR gate.

The OR gate may have N number of inputs and one output. If the number of inputs are N then N ≥ 2 conditions must be applied for input operation. Digital inputs are applied in terms of A, B, C.....N, and the output is Y.

The mathematic equation is given below:

$$Y = A \text{ OR } B \text{ OR } C \text{ OR } D \ldots\ldots\ldots \text{ OR } N$$
$$= A+B+C+D \ldots\ldots + N$$

The truth table for an OR gate is provided in Table 1.2.

Table 1.2 Truth table of an OR gate.

I/P		O/P
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	1

NOT operation:
This is also called an inverter. The symbol for the NOT gate is shown in Figure 1.3. It has a single input device and it generates an inverted output. Table 1.3 describes the truth table of a NOT gate. The mathematical equation is written as:

$$Y = \text{NOT } A$$
$$= \overline{A}$$

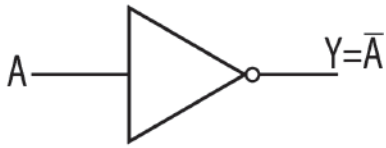


Figure 1.3 Symbol for a NOT gate.

Table 1.3 Truth table of a NOT gate.

I/P	O/P
A	**Y**
0	1
1	0

1.1.1 Universal Gate Operation

Universal gates are those in which any logical expression can be realized. The NAND and NOR gates are very popular and are widely used for realization of logical expressions. Therefore, these two NAND and NOR gates are used to implement other gates so these are called universal gates.

NAND operation

This is a universal gate. The operation NOT-AND is known as a NAND operation. It has N number of inputs and one output like other basic gates. However, two inputs and one output NAND gate are shown in Figure 1.4. Table 1.4 provides output values of a NAND gate in terms of inputs. The Boolean equation is given below:

$$Y = \overline{A.B}$$

Figure 1.4 Symbol for a NAND gate.

Table 1.4 Truth table of a NAND gate.

I/P		O/P
A	**B**	**Y**
0	0	1
0	1	1
1	0	1
1	1	0

NOR operation

This is a universal gate. The operation NOT-OR is known as a NOR operation. It has N number of inputs and one output similar to basic gates. The symbol diagram of two inputs and one output is shown in Figure 1.5. Table 1.5 gives output values of a NOR gate in terms of inputs. The Boolean equation is given below:

$$Y = \overline{A + B}$$

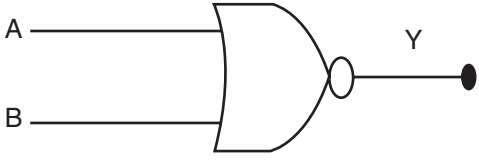


Figure 1.5 Symbol for a NOR gate.

Table 1.5 Truth table of a NOR gate.

I/P		O/P
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	0

EX-OR Operation

The operation EX-OR is used in many applications. It has N number of inputs and one output like other basic gates. The symbol diagram of two I/P and one O/P is shown in Figure 1.6. Table 1.6 provides the output values of an EX-OR gate in terms of inputs. Its mathematic equation is given below:

$$Y = \overline{A \oplus B}$$

Figure 1.6 Symbol for a NAND gate.

Table 1.6 Truth table of a NAND gate.

I/P		O/P
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

1.1.2 Combinational Logic Circuits

This type of circuit depends upon the I/Ps in that particular instant of time. A memory element is not available. A combinational circuit may have a number of sub-systems as shown in Figure 1.7.

Figure 1.7 Diagram of a combinational logic circuit.

There are many ways to design these combinational logic circuits. These include:

1. Boolean expression
2. Set of statement
3. Truth table

These designs are used to design combinational logic circuits. However, a number of methods are also available to simplify Boolean function. These include:

a) Algebraic method
b) K-map method
c) Variable entered method
d) Tabulation method

Standard representation for logical functions
Any logical functions can be represented in terms of their logical variables. Logical variables and their functions are in binary form. There are two standard forms generally being used in circuit designing.

1. Sum of product (SOP)
2. Product of sum (POS)

Apart from the form above, other forms are also available to design circuits. However, these forms are conveniently suitable for the design process. This is discussed in more detail in the next subsection.

1.2 Combinational Logic Circuits Using MSI

This subsection describes the simplification and realization of the combinational logic circuits using gates. These methods are used to integrate complex functions in the form of IC. There are many devices are available such as adders, multiplexers, de-multiplexers, decoders, and multipliers.

1.2.1 Adders

An adder is a combinational logic circuit that performs arithmetic sums of binary numbers and produces corresponding outputs.

Half Adder

This is a basic adder that performs arithmetic sums of two inputs and gives the corresponding output in terms of sum and carry. The diagram of a H. adder is shown in Figure 1.8.

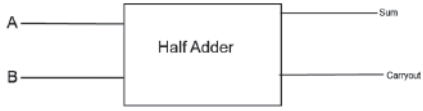


Figure 1.8 Block diagram of a H. adder.

A and B are I/Ps and O/Ps and are the sum and carry of the H. adder. The truth table is given in Table 1.7.

Table 1.7 Truth table of a half adder.

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Mathematical expressions for the H. adder are:

$$\begin{aligned} \text{Sum} &= \bar{\text{A}}\text{B} + \text{A}\bar{\text{B}} \\ &= A \oplus B \\ \text{Carry} &= \text{AB} \end{aligned}$$

The circuit diagram of the H. adder is shown in Figure 1.9.

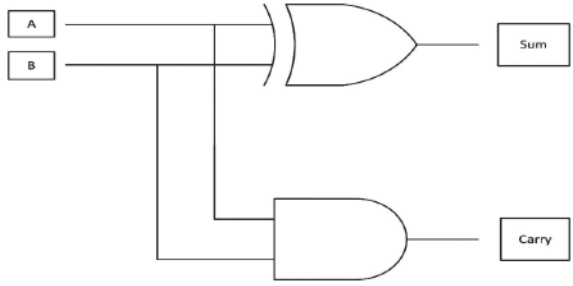


Figure 1.9 Circuit diagram of a half adder.

Full Adder

This performs the arithmetic sum of three inputs and gives the corresponding two outputs in terms of sum and carry. A block diagram of the full adder is shown in Figure 1.10. Table 1.8 provides the truth table of a full adder circuit where output variables (Sum, Cout) are expressed in terms of input values.

Figure 1.10 Block diagram of a full adder.

Table 1.8 Truth table of a full adder.

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean expressions for the F. adder are:
K-Map for Sum:

	B'Ci'n	B'Cin	BCin	BCin'
A'		①		①
A	①		①	

$$\text{Sum} = A \oplus B \oplus \text{Cin}$$

K-Map for Cout:

	B'Ci'n	B'Cin	BCin	BCin'
A'			1	
A		1	1	1

$$\text{Cout} = AB + BCin + Cin\,A$$