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High Efficiency Power Amplifier Design for 28 GHz 5G Transmitters

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For my parents, Somaya and Mohamed.

Nourhan Elsayed

Preface

The wireless communication market has witnessed a substantial level of development and growth in recent years. The ever-increasing number of subscribers, demand for higher data rate, and better connectivity has driven the markets to provide more efficient communication schemes with a low cost-to-market. The available mm-wave spectrum has driven work towards introducing 5G technology. 5G technology is expected to operate in the 28 GHz band with high peak-to-average power ratio (PAPR). This is a consequence of orthogonal frequency division multiplexing (OFDM) modulation combined with QAM modulated OFDM carrier signals that enable high data rates and high spectral efficiency.

The power amplifier (PA) is a key building block in a transmitter and is the most power-hungry component in modern systems. To offer lower cost of integration, it is desirable to have the entire transceiver system, including the PA, on a single CMOS chip. Some of the major challenges that CMOS power amplifiers face at mm-wave frequencies are limited output power per transistor and low power added efficiency. The recent availability of scaled CMOS technology with cut-off frequency larger than 300 GHz has opened the possibility of implementing mm-wave systems at a high level of integration. Despite that, stringent requirements on the PA to achieve the desired efficiency, linearity, and output power while operating at lower supply voltages still impose a challenge. This has driven a lot of research towards different circuit techniques, and design trade-offs for power amplifiers in scaled CMOS technologies. However, there is still a clear gap in achieving the desired performance in PAs dedicated towards 5G applications.

The first part of this book presents the design of highly efficient PA architectures in 22 nm FDSOI technology at 28 GHz. This effort was done in order to achieve high efficiency while maintaining the stringent linearity and output power requirements imposed by high PAPR signals. Four different PA architectures were designed: one based on linear PAs, two switching PAs, and one hybrid. All these PAs were fabricated in GlobalFoundries and measurement results are presented and compared with simulation. The first PA presented is based on a Doherty architecture with a Class-A PA as the main amplifier, and Class-C as the auxiliary amplifier, both

utilizing the stacking technique to overcome the low breakdown voltage of the devices.

A switched-mode Class-E PA was also designed utilizing the cascode topology. A novel technique of switching the cascode device along with the input device, referred to as *pulse injection*, has been employed to maximize efficiency. The PA achieves peak measured power added efficiency (PAE) of 35%, drain efficiency (DE) of 45%, and 8.5 dB power gain. While this PA achieves high efficiency, linearity is still a concern. As a means of linearization, a Class-E based Doherty PA was designed in order to utilize the high efficiency achieved from the auxiliary Class-E PA while maintaining linearity due to the Doherty configuration. The Doherty-based Class-E PA achieves a measured peak PAE of 32% and 31% at 6-dB back-off and hence maintains the efficiency at high and backed-off power levels, with a gain of 17 dB.

Next, a current mode Class-D (CMCD) PA utilizing the cascode topology was designed. The CMCD PA also utilizes pulse injection to switch the cascode device via a tunable transmission line as a delay element. Measurement results show a measured peak PAE of 46% and drain efficiency (DE) of 71% with a saturated output power of 19 dBm. This PA reports the best performance compared to other CMCD current mode Class-D PAs in literature at mm-waves.

Finally, the measured Class-E Doherty-based PA is integrated into a 4 phased-array transmitter design utilizing a novel active power divider. Measurement results of the stand-alone power divider were used to validate its functionality. Simulation results are presented for the full transmitter chain. Currently, a PCB is being developed to measure and validate the 4-phased-array transmitter design.

All in all, with the speeding race to offer 5G communication scheme to the market, this book aims to fill the gap in research between achieving high efficiency and a high level of integration through utilizing scaled CMOS technology (22 nm FDSOI).

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