Anatoly Belous
Vitali Saladukha

The Art and Science of Microelectronic Circuit Design

Springer

The Art and Science of Microelectronic Circuit Design

Anatoly Belous • Vitali Saladukha

The Art and Science of Microelectronic Circuit Design

Springer

Anatoly Belous
Integral
Minsk, Belarus

Vitali Saladukha
Integral
Minsk, Belarus

ISBN 978-3-030-89853-3 ISBN 978-3-030-89854-0 (eBook)
https://doi.org/10.1007/978-3-030-89854-0

This Springer imprint is published by the registered company Springer Nature Switzerland AG
The registered company address is: Gewerbestrasse 11, 6330 Cham, Switzerland

Preface

This book is intended primarily for students, teachers, undergraduates, engineers and technicians specializing in the field of microelectronics and its numerous applications. In addition, the contents of the book can be useful to scientists and specialists in the field of design, organization of production, and operation of radio-electronic devices and systems for household, industrial and special (space and military) purposes. In fact, the materials of this book are a practical guide (handbook) for the design of modern silicon digital microcircuits and systems-on-a-chip (SoC).

At the time of this book's publication, there are quite a lot of texts devoted to this area of focus, for example, *Handbook of Digital CMOS Technology and System* by Abbas Karim; *Handbook of Digital Technology for High Speed Design* by Tom Granberg; and *Design Techniques for High-Frequency CMOS Integrated Circuits: From 10 GHz to 100 GHz* by Zhiming Deng.

Here it is worth recalling a number of major "classic" publications on this subject matter written many years ago, which can still be seen in the workplaces of today's "electronics" engineers.

The publication closest to the topic discussed here and widely known to students, *The Art of Circuit Design* monograph, a classic textbook on digital and analogue circuitry, was written by American practical scientists Paul Horowitz from Harvard University and Winfield Hill from Rowland Institute for Science, Cambridge, Massachusetts. Its first English edition (*Cambridge University Press*) was published in 1980 and has subsequently gone through dozens of editions and is still in demand by students today.

This excitement around the book written by American specialists and its ongoing popularity among a wide range of readers can be explained, on the first hand, by broad coverage of its subject area, that is, the basics of designing radio electronic circuits, and by extensive background information on the element base ("bricks" that make up radio electronic devices) at the time of writing the book.

And, on the second hand, in contrast to classical textbooks with an abundance of mathematical calculations and physical formulas, the authors outlined here all the basic (at that time) aspects of designing radio electronic devices, in simple language

and with a large number of clear practical examples, at a level that is understandable even to "poorly trained" readers.

For its popularity, extraordinary for such publications, among students and electronics engineers, the book received a well-deserved informal title in the 1990s, *"the bible of electronics"*.

It is obvious that over the past 40(!) years since writing of this book, the element base of microcircuits, radio electronic devices and systems, subject to the well-known Moore's law, has changed fundamentally. Those "bricks", brilliantly described in this "bible of electronics", have long ago been incorporated into larger "building blocks" (IP-blocks or "Intellectual properties") that modern IC and SoC are "assembled" of; new elements that simply could not be implemented technologically in the past have also appeared; and basic elements that operate on entirely new physical principles and mechanisms have emerged.

A major advantage of the book, proposed by the authors, is specifically a detailed description of the principles of operation and rules for application of these present-day basic elements in microelectronic devices. For example, elements implemented on modern bipolar field technology (BiCMOS) just did not exist at the time of publication of the last English edition of the "bible"; the same can be said about micropower CMOS basic functional components.

Until now, *The Semiconductor Circuitry: Handbook by Tietze U., Schenk Ch.* is also used in the training courses of many universities. In Germany and Russia, this book has survived more than 20 editions. Although this book deals only with the structures of the simplest semiconductor elements, which are practically not used in microelectronic devices today (except for elements of power electronics, studied in detail in that book), nevertheless, regular versions of this reference manual are still periodically issued by publishers and are in demand by specialists and students, since more "up-to-date" publications have not been available on sale until now.

Today in the US, UK and European book markets, there are a number of other books devoted to circuit design of modern microelectronic devices. Most of them, however, consider only individual components of a complex design problem and describe particular technologies (methods for reducing power dissipation, increasing performance, simulation and protection against spurious effects) in relation to specific technology basis, such as CMOS, bipolar, BICMOS and SOI.

The motivation of the authors to write these chapters on "circuit design" was the desire to help a wide range of students, teachers and engineers, specializing in the design and operation of various microelectronic devices, to understand physical mechanisms of processes occurring inside these "bricks" used to build modern ICs and systems-on-a-chip.

This book is based on the seminar materials of the lecture courses read by the authors for many years in Russian and Belarusian universities and academic institutions for students, graduate students, undergraduates and teachers of the following specialties: electronics and microelectronics; design and technology of electronic means; instrument engineering; computer science and computer engineering;

electronic engineering, radio engineering and communication; and automation and control.

In addition, we used the results of our own research, previously published in monographs (including those published abroad), patents and articles, as well as the results of our practical activities in the field of design and application of microelectronic devices.

Figuratively speaking, the modern students and engineers, specializing in the sphere of microelectronics and its applications, can derive from these books, articles and social nets the detailed and comprehensive description of some solitary "trees", but they will have to apply the strenuous efforts to gain the whole picture of the "forest".

Therefore, the authors have aspired for the quite ambitious challenge – to create the integral picture of such "microelectronic forest", consisting of individual "trees" (chapters). Each of the chapters is consistently dealing with major milestones of modern microcircuit design, ranging from description of physical concepts of transistor operation, basic libraries and design flows, methods of logic designing of low power consumption microcircuits, assembly technologies of microcircuits and systems on chip to quality management methods based upon special test structures.

Meanwhile, the authors have taken guidance from the following ***principles*** of construction of the chapter material, which was rather easy to formulate, but quite hard to encompass in the process of writing the book:

1. For the sake of being a popular edition amongst the vast circle of readers (engineers and students), the book should meet simultaneously the integral functions of both the classic manual and a brief reference book, being with the finesse of the captivating reading.
2. The book should comprise only those methods, schematic and technological solutions whose effectiveness was proven earlier with the practice of their application.
3. In the textual part of the book, it is necessary to use the maximum possible scope of the graphic material, reflecting the effectiveness of the various working scenarios.

The following introduction provides a brief summary of each of the chapters of this book.

Circuit Design The largest scope of material (four chapters) in our book is devoted to the fundamentals of circuit engineering of modern microelectronic devices (microcircuits and systems-on-a-chip). This is due to the fact that our book eliminates a number of "gaps", obvious to the specialists in this field, in a large volume of existing scientific and technical literature on issues relating to the analysis of operating peculiarities, design methods and fundamentals of practical application of digital microcircuits in modern microelectronic devices.

Here, a large set of effective ***circuit design solutions*** of basic elements is presented to meet the requirements for modern complex-functional, high-performance and reliable microelectronic devices.

This topic deserves a more detailed explanation.

As you know, the process of developing any digital microcircuit consists of two main interrelated stages: *logic design*, which determines the logical organization (architecture), command system, interface, structure of control and data processing devices, including timing diagram of operation, and *circuit design*, which includes a set of objectives for selecting a technological basis, converting logic circuits into electrical circuits at a transistor level, choosing circuitry solutions for basic elements and synchronization methods, and designing power supply circuits and devices for protection against external and internal interference and static electricity charges.

While methodology and ways of solving problems of the *logic design* stage are widely enough reviewed in numerous foreign and domestic publications, this is unfortunately not the case with the *circuit design* stage.

So, in numerous educational scientific and technical literature, existing at present, methods of designing various functional blocks of combinational (decoders, multiplexers, demultiplexers, adders, multipliers, etc.) and sequential types (automata with memory as flip-flops, registers, counters, etc.) are described in detail, and various methods and means of their computer-aided design are also discussed.

In this case, these nodes and blocks are represented at the level of "small squares" described in the language of Boolean algebra ("AND", "NOT", "AND-NOT", "OR-NOT", etc.) or in the form of graphical symbols (D-trigger, R-S-trigger, DV-trigger, etc.).

Of course, this procedure is a mandatory and integral initial stage of the end-to-end design process of any microelectronic device. However, both the designer and the end user of a microelectronic device must understand what is "inside" these blocks and nodes. The designer needs this in order to ensure the required values of electrical and dynamic parameters of the device under design by selecting the appropriate elements (transistors) and their connections.

The user or operator of this microelectronic device needs to know the "stuffing" of these blocks in order to understand specific features of a particular microelectronic device functioning in its various operating modes.

After all, even the structure of such a simple "brick" as an internal memory device of a microcircuit, D-trigger, can be implemented by dozens of different circuitry solutions for interconnecting its component transistors. And a modern student should clearly understand how this synthesized block (a set of "squares") "turns into" the layout of the corresponding area of an IC's semiconductor chip, where placement of transistors on chip surface by organizing appropriate links and interconnections of these transistors and their connections with other blocks allows you to implement a preset algorithm for the functioning of the block (node).

But this D-trigger can be implemented using various technologies like CMOS, BiCMOS and bipolar (STTL, ECL, I^2L), each with its own "subtle aspects", and this is how these four chapters on "circuit design" appeared.

The four chapters of this book on "circuit design" address such a complex problem: numerous examples are given for the basic blocks of modern microelectronic devices at the level of transistors and their interconnections. It is shown, for example, that the simplest D-trigger, depending on its circuit design, will provide different numerical values required by the designer, such as response time, load capacity, noise immunity and power consumption.

An additional peculiarity of these four chapters on "circuit design" is a detailed description of various types of matching devices (elements) – input and output ones, which provide electrical and time correlation during microcircuit operation in a finished radio electronic device, as well as methods and circuitry solutions for reducing energy consumption of modern microcircuits, as an ever-relevant problem.

After all, it is the circuitry solutions of microcircuit basic elements that finally define numerical values of electric, static and dynamic characteristics, power consumption, response time, noise immunity, and even the area of an IC chip.

Design Libraries for Submicron Microcircuits

Another separate "training" chapter focuses on the contents and basic rules for the development and application of design libraries for submicron microcircuits, known in the design communities as "design kits" or PDK (Process Design Kits).

Recently, due to the emergence of separate (independent of microcircuit designers) semiconductor fabrication plants engaged in custom serial production of microcircuits (Integrated Circuits Foundry, ICF) and in connection with the objective need to share standard design tools and "purchased" IP blocks (intellectual properties) from other companies, it is the design libraries (PDKs) that became the main link between designers and manufacturers of microcircuits.

This chapter details the typical design flow and PDK structure, minimum contents of a basic library and minimum list of standard elements (cells), level translators, current source models, input and output buffers, and typical data files of design library. Specific instructional (educational) PDK by Synopsys is also described here.

Design Flows Used for Submicron Microcircuits This chapter deals with the study of design flows of modern submicron microcircuits. Here, the specifics of selecting a particular design flow in dependence on initial requirements of a microcircuit customer are considered. The contents of the basic stages of design flow are described, that is, system, functional and physical design as well as design verification. Specific features of designing microelectronic products at a higher level of complexity, that is, systems-on-a-chip (SoC), are examined in detail: development trends, detailed design flows, design methodologies, significant peculiarities of SoC system design stage and basic components of CAD tools for the system level. To

"reinforce" the studied material, clear practical examples of SoC simulation process, described in the Cadence Incisive Simulation Environment, will be given here with the author's comments.

Fundamentals of Low-Power CMOS-Microcircuits Logic Design This chapter deals with the peculiarities of low-power CMOS microcircuit *logic* design. The developmental challenges of modern submicron technology force IC designers to seek ever-new techniques and methods of design, aimed at reducing power consumption caused by leakage currents, whose importance and contribution increases significantly with the decrease in design rules. This chapter reviews new methods of logic design of CMOS microcircuits with reduced power consumption, based on the mathematical apparatus of probabilistic evaluation of various optimization options by the predicted so-called "switching activity" of main blocks (nodes) of the designed microcircuit. The basic stages of such a logic design are presented here, starting from selection of required logic element basis, logic synthesis in this chosen basis, optimization procedure for two-level logic circuits, optimization of multi-level logic circuits built on both two-input and multi-input logic gates, and finishing with procedures for "technology mapping" and evaluation of power consumption of the designed (synthesized) microcircuit both at logic and circuit design levels.

At the end of the chapter, the applicable hardware-software complex for the logic design of micro-power CMOS IC is described in detail.

Quality Management Systems for IC Manufacturing It is known that a developer-designed microcircuit is then usually sent to a semiconductor fabrication plant to manufacture pilot samples (experimental prototypes). Global practice of the last decade shows that only about 40% of designed microcircuits meet the requirements of original specification (terms of reference) after manufacture; therefore, sometimes full compliance of products with the technical design assignment and, beyond that, the "targeted" yield can be achieved only after a number of successive iterations (corrections).

In order to improve efficiency and reduce the time for analysis and identification of the causes of failure to achieve the specified characteristics or yield percentage of the designed microcircuit, the process flow often uses special test structures placed on the chip (wafer) of the designed IC. Understanding physical mechanisms of IC failures is necessary not only for proper selection of microcircuit design solutions, taking into account permissible and critical levels of current density in active semiconductor structures and interconnections, and electric field strength in dielectric layers, but it is also required for developing appropriate measures to identify and reject potentially unreliable microcircuits at various stages of serial production.

This chapter will discuss the key principles of formation of such semiconductor test structures "built in a chip (or a wafer)", the definition of their list and functions, the foundations of step-by-step reliability prediction of the designed IC based on the

results of statistical processing of numerical values of the measured parameters of such test structures. Mathematical models linking obtained statistical distribution of technical parameter values of the microcircuits with specific reliability indexes are presented and explained herein; specific practical examples of process optimization with the help of special test wafers are also given.

Minsk, Belarus

Anatoly Belous
Vitali Saladukha

Acknowledgements

The authors would like to express their gratitude to the colleagues who actively participated in the preparation and discussion of the contents of this book, whose critical comments, advice and additions contributed to improving both the structure of this book and the material presented in it: V. Borisenko, V. Bondarenko, V. Stempitsky, A. Silin and L. Lynkov.

The authors extend their special thanks to the colleagues who provided the original materials of their own theoretical and practical research on the subject matter of this book, whose inclusion in the book greatly enhanced the practical focus of this work: P. Bibilo, L. Cheremisinova, A. Petlitsky and T. Petlitskaya.

The authors enclose their gratitude to the reviewer V. Labunov, academician at the National Academy of Sciences of Belarus and foreign elected member of the Academy of Sciences of the Russian Federation, whose specific comments and suggestions have significantly contributed to the formation of the final shape of this book, offered to the reader.

The authors are also grateful to O. Antipenko for her high-quality execution of a large amount of work on technical design of the book's manuscript. They also offer thanks to E. Kartashova and K. Gaivoronsky for their contribution in preparation of the graphic images, to the employees of the publishing house TEKHNOSPHERE, to O. Kuleshova and S. Orlov for the providing graphic materials, and to V. Chikilev, M. Biryukova, L. Ignatovich, Yu. Sizov, N. Mazurina, I. Kurshatsova and V. Ilyenkov for assistance in translation of the textual materials of the book.

Contents

1 Standard Characteristics of Digital Microcircuits 1
1.1 Structure of Digital Microcircuits 1
1.1.1 General Structure of Digital Microcircuits 1
1.1.2 Architecture of Internal Cells of Digital Microcircuits . . . 3
1.1.3 Architecture of Digital Microcircuit Matching Elements 10
1.2 System of Main Parameters and Chracteristics of Digital Microcircuits 20
1.2.1 Functional Parameters of Digital Microcircuits 20
1.2.2 Electical Parameters of Digital Microcircuits 21
1.2.3 Dynamic Parameters of Digital Microcircuits 23
1.3 Schematic Implementation of Digital Microcircuits 25
1.3.1 Power Characteristics of Standard Logic Cells of Digital Microcircuits 25
1.3.2 Schematic Implementation of Standard Digital Microcircuits 34
1.3.3 Techniques of Digital Microcircuits Element Base Selection 38
1.4 Impact of Destabilizing Factors on Serviceability of Digital Microcircuits 39
1.4.1 Immunity of Digital Microcircuits to Electrostatic Discharge 40
1.4.2 Microcircuits Overload Tolerance 46
1.4.3 Dependence of Electrical Characteristics of Digital Microcircuits Upon Operational Modes 47
1.4.4 Immunity of Digital Microcircuits to the Impact Produced by Interferences 49
1.5 Parasitic Elements and Effects in Digital Microcircuits 63
1.5.1 Parasitic Transistor Elements Inside Digital Microcircuit Dice 63

1.5.2 Miller's Effect . . . 69
1.5.3 Latch-Up Effect . . . 71
References . . . 76

2 Schematic Solutions of Digital CMOS Microcircuits . . . 79
2.1 Standard Logic Cells of Digital CMOS Microcircuits . . . 79
2.1.1 Static CMOS Logic Cells . . . 80
2.1.2 Standard LC of Dynamic CMOS Logic . . . 99
2.2 Memory Elements of the Digital CMOS Integrated Circuits . . . 113
2.2.1 Memory Elements, Clocked by the Level of the Synchrosignal . . . 114
2.2.2 Memory Elements, Clocked by the Synchrosignal Edge . . . 121
References . . . 122

3 Schematic Technical Solutions of the Bipolar Integrated Circuits . . . 125
3.1 Digital Integrated Circuits on the Bipolar Transistors with the Schottky Diodes . . . 125
3.1.1 Basic TTLS Logic Elements of Digital Integrated Circuits . . . 126
3.1.2 Basic Logic Elements of Schottky Transistor Logic . . . 133
3.1.3 Basic Logic Elements of the Integrated Schottky Logic . . . 136
3.1.4 Base Logic Elements of the Diode-Transistor Logic with Schottky Diodes . . . 139
3.2 Memory Elements of TTLS Integrated Circuits . . . 140
3.2.1 Memory Elements, Synchrosignal Edge Cycled . . . 140
3.2.2 Memory Elements, Cycled by the Level of the Synchrosignal . . . 150
3.3 Schematics of the Input Matching Elements of the TTLS Integrated Circuits . . . 153
3.3.1 Input Matching TTLS Elements of Integrated Circuits with the standard TTL input levels . . . 153
3.3.2 Input ME TTLS of Integrated Circuits with the Enhanced Load Capacitance . . . 157
3.3.3 Input ME TTLS of the Integrated Circuits with the Paraphrase Outputs . . . 158
3.3.4 Input ME TTLS Integrated Circuits with Memory . . . 160
3.3.5 Input BE TTLS of Integrated Circuits with the Enhanced Noise Immunity . . . 163
3.3.6 Input Matching Element with Conversion of the Signal Levels . . . 170
3.3.7 Protection Diagrams of the Input ME TTLS Integrated Circuits . . . 176

3.4 Schematics of the Output Matching Elements of TTLS Integrated Circuits . . . 179
3.4.1 Output ME TTLS of Integrated Circuits with Standard TTL Output Levels . . . 179
3.4.2 Output ME of TTLS Integrated Circuits with Memory . . . 188
3.4.3 Output ME of TTLS Integrated Circuits with Conversion of signal levels . . . 190
3.4.4 Schematics of the Protection Circuits of the Output ME of TTLS Integrated Circuits . . . 193
3.5 Digital Integrated Circuits on the Basis of the Integrated Injection Logic . . . 206
3.5.1 Varieties of the Basic Elements of the I^2L Integrated Circuits . . . 211
3.5.2 Memory Elements of I^2L Integrated Circuits . . . 219
3.5.3 Schematics of the Input Matching Elements of the I^2L Integrated Circuits . . . 225
3.5.4 Protection of the I^2L Pins of the Integrated Circuits from Overvoltage and Static Electricity . . . 240
References . . . 241

4 Circuit Engineering of Bi-CMOS IC . . . 243
4.1 Basic Logic Elements of Bi-CMOS IC . . . 243
4.2 Bi-CMOS IC Memory Elements . . . 255
4.3 Circuit Engineering of Bi-CMOS IC Input Matching Components . . . 256
4.3.1 Input MC of Bi-CMOS IC with Signal Level Conversion . . . 257
4.3.2 Input MC of Bi-CMOS IC with Increased Load Capacity . . . 261
4.3.3 Input MC of Bi-CMOS IC with Paraphase Outputs . . . 261
4.3.4 Input MC of Bi-CMOS IC with Increased Noise Immunity . . . 262
4.3.5 Input MC of Bi-CMOS Memory IC . . . 263
4.3.6 Circuit Engineering of Input MC of Bi-CMOS IC Protection . . . 263
4.4 Circuit Engineering of Bi-CMOS IC Matching Output Components . . . 264
4.4.1 Output MC of Bi-CMOS IC with the Formation of CMOS Output Levels . . . 264
4.4.2 Output MC of Bi-CMOS ICs with the Formation of TTL Output Levels . . . 265
4.4.3 Output MC of Bi-CMOS IC with the Formation of ECL Output Levels . . . 268

4.4.4 Output MC BI-CMOS Memory ICs 270
4.4.5 Circuit Engineering of the Output MC BI-CMOS IC Protection Circuits 270
References 270

5 Structure and Specific Features of Design Libraries for Submicron Microcircuits 271
5.1 Development Process Flow and Standard Structure of a Process Design Kit (PDK) 271
5.2 Terms and Definitions Used to Describe PDK Components 274
5.3 PDK Standardization 274
5.4 Mixed Analog/Digital Microcircuit Design Flow 279
5.5 Summarized Information Model of Mixed Analog-Digital IC Design 281
5.6 Specifying Basic PDK Components and Standard Elements List 283
5.7 Development Features of Digital Libraries for Designing ASICs with Submicron Design Rules 283
5.8 Structural and Circuit-Level Features of Designing Basic Cells for Submicron Microcircuits Library 292
5.8.1 Voltage Level Shifters 293
5.8.2 Power Gating Circuits 294
5.8.3 Isolation Library Cells for Submicron Microcircuits 295
5.8.4 "Always-on" Buffers 297
5.9 Standard PDK Data Files 300
5.10 Standard PDK Current Source Models (CCS) 302
5.11 Methods and Examples of Standard IC Design Tools Adaptation to 90, 65, and 45 Nm Microcircuit Design 304
5.11.1 Synopsys Tutorial (Educational) Design Kit: Capabilities, Applications, and Prospects 304
5.11.2 Synopsys EDK Overview 304
5.11.3 Synopsys Digital Standard Cell Library 308
5.11.4 I/O Standard Cell Library 310
5.11.5 Standard Set of PDK Memory Modules 311
5.11.6 Phase-Locked Loop (PLL) 311
5.11.7 Geography of EDK Applications and Prospects 311
5.12 Contents of Educational Design Kits Provided by IMEC 312
References 316

6 Digital IC and System-on-Chip Design Flows 317
6.1 Choosing the IC Design Flow 317
6.2 System Design Stage 321
6.3 Functional Design Stage 324
6.4 Logic Design Stage 327
6.5 Physical (Topological) Design Stage 329

6.6 Stage of Physical Verification and Preparation for Production . . . 331
6.7 Project Certification . . . 333
6.8 SoC Design Flow . . . 334
6.8.1 Trends in the Development of Design Tools . . . 334
6.8.2 SoC Design Methodology . . . 335
6.8.3 SoC Design Flow . . . 338
6.8.4 SoC System Design . . . 340
6.8.5 CAD Software for the System Level . . . 343
6.9 Practical Example of the System-on-Chip Simulation . . . 345
6.9.1 Standard Design Flow of the SoC of Cadence Company . . . 345
6.9.2 Description of the Simulation and Verification Environment . . . 345
6.9.3 Project in the Cadence Incisive Environment . . . 350
References . . . 353

7 Fundamentals of CMOS Microcircuits Logic Design with Reduced Power Consumption . . . 355
7.1 Basics of Low-Power-Driven Logic Synthesis of CMOS Microcircuits . . . 356
7.2 Identification of Power Dissipation Sources in CMOS Microcircuits . . . 358
7.3 Probabilistic Evaluation of Optimization Options by Predicted Switching Activity of IC Nodes . . . 360
7.4 Selection of Element Basis for Low-Power CMOS Microcircuit Design . . . 362
7.5 Logic Synthesis of CMOS Microcircuits in the Basis of Library Elements . . . 363
7.6 Power Dissipation-Driven Optimization of Two-Level Logic Circuits . . . 366
7.7 Selection of Basic Gates for Technology-Independent Functional Circuit . . . 368
7.8 Optimization of Multilevel Logic Circuits of Multi-input Gates . . . 369
7.9 Optimization of Multilevel Logic Circuits of Double Input Gates . . . 371
7.10 Technology Mapping . . . 374
7.11 Estimation of Power Consumption of Designed CMOS Microcircuits at Logic and Circuitry Levels . . . 375
7.12 Low-Power CMOS Microcircuit Design Technology with ELS Package . . . 377
7.13 ELS Software Package Architecture . . . 378
7.14 Functional Capabilities of ELS Software Package . . . 380
References . . . 384

8 Fundamentals of Building a Quality Management System for Manufacturing Submicron Integrated Circuits Based on Test Structures 387
8.1 Methodology of the Organization of Technological Test Control in the Process of Design and Production of Microelectronic Products 388
8.1.1 Place and Role of Semiconductor Test Structures in the Process of Manufacturing Integrated Circuits 388
8.1.2 Classification of Technological Test Structures 390
8.1.3 Methods of Placing Test Structures on Semiconductor Wafers 392
8.2 Principles of Control of the Process of Manufacturing Chips Using Test Structures 394
8.2.1 Assessment of the Quality of the Process Based on the Method of Interoperative Control of Wafers 394
8.2.2 Typical Composition of the Test Module for Monitoring Production Processes 395
8.2.3 Typical Composition of Test Structures for Quality Control of Submicron ICs 396
8.2.4 Statistical Processing of Measurement Results of Test Structures 398
8.3 Forecasting the IC Yield Based on the Results of the Test Control 399
8.3.1 Features of Simulation of the IC Yield 399
8.3.2 Model of Postoperative Separation of Defects in the Technological Process of IC Manufacturing 404
8.4 Typical Structure of the System of Technological Process Test Quality Control 407
8.4.1 Features of the Organization of Test Modules for Bipolar and CMOS ICs 407
8.4.2 Typical Example of the Use of Test Modules for the Analysis of the Manufacturing Process in the Conditions of Mass Production 411
8.5 The Main Technological Factors Affecting the Reliability of Microelectronic Products 413
8.5.1 Fundamentals of the Theory of Reliability of Semiconductor Devices and Integrated Circuits 413
8.5.2 Ways to Improve the Reliability of the Metallization System of Integrated Circuits and Semiconductor Devices 417
References 422

Index 425

Chapter 1
Standard Characteristics of Digital Microcircuits

This chapter provides well-marshaled and interpreted essential technical characteristics of up-to-date digital microcircuits: summarized general structure of microcircuits, architecture of internal standard cells and matching components, and system of essential parameters (functional, electrical, and dynamic parameters).

There are elaborated key options of schematic implementation of basic logic elements of digital microcircuits, impact of destabilizing factors to their serviceability (tolerance to electrical and temperature overloads, impacts produced by external and internal electrical noises, including noises by supply lines and common lines).

The chapter concludes with the insight into the main parasitic elements and parasitic effects in digital microcircuits (parasitic transistors, latch-up effects, Miller effect, etc.)

1.1 Structure of Digital Microcircuits

1.1.1 General Structure of Digital Microcircuits

It is a common fact that one of the main trends in microelectronics is constant persistent increase of functional complexity of digital microcircuit which is attained essentially through increase in the number of elements being integrated into a semiconductor chip and ongoing improvement of schematic solutions implemented in standard cells. Main trends leading the way to increase of functional complexity of digital microcircuits are reduction of cell linear dimensions (scaling) at simultaneous reduction of the applied supply voltage value which results in reduction of the total value of their loading capacitances. However, marginal growth of cell number on a chip is limited by maximum tolerable chip area (S_{KP}) and maximum tolerable power dissipated by a package of a digital microcircuit ($P_{package}$). Reduction of cell power consumption and miniaturization of their sizes tend to cut down their output currents and also noticeably affect their load-carrying capacitance and interference immunity

A. Belous, V. Saladukha, *The Art and Science of Microelectronic Circuit Design*,
https://doi.org/10.1007/978-3-030-89854-0_1

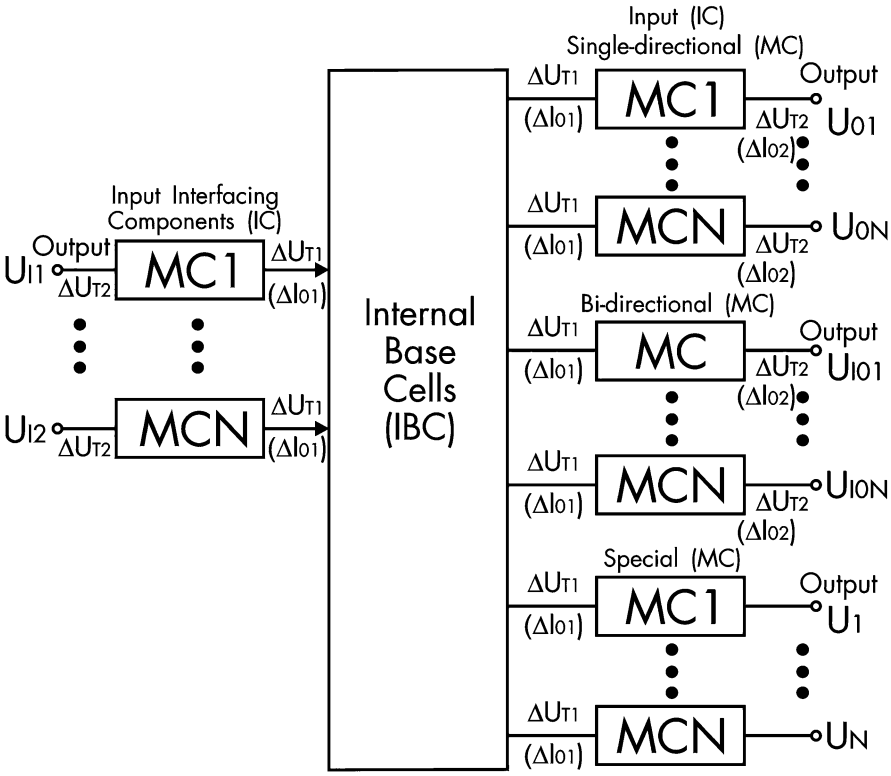

Fig. 1.1 Generalized architecture of digital microcircuits [1]

of microcircuits. Whereas internal interferences inside of microcircuits are comparatively small and loading capacities of microcircuit internal cells are not high, using low-power cells with low output currents as the internal cells does not normally create any problems, making it possible to decrease the value of logic voltage drop and to obtain in the process high-speed performance, low power consumption, and larger integration scale of digital microcircuits.

However, when such cells are used to receive the signals external for microcircuits, the value of aggregated interference immunity of microcircuits is being reduced, and rather low load-carrying capacitance of the cells not infrequently prevents from obtaining the specified high-speed performance of microcircuits when numerous external loading is being controlled. As a consequence, in digital microcircuits, the architecture depicted in [1] is widely used where elements having two values of logic voltage (currents) swing are used ΔU_T (ΔI_O). The architecture of digital microcircuits is shown in Fig. 1.1 and contains two standard types of cells: internal base cells (IBC), with input (output) logic swing ΔU_{TI} (ΔI_{OI}) of low value $\Delta U_{TI} \approx 0.2 \div 1.5$ V ($\Delta I_{0I} \approx 0.1 \div 1$ mA), and external matching components (MC), with input logic swing ΔU_{T2} of higher value (switching threshold $U_T = 1.5 \div 15$ V)

and output matching components with logic input swing equal to logic swing of IBC ΔU_{T1} and output matching components with input logic swing equal to logic swing of IBC ΔU_{T1} and output logic swing ΔU_{T2} (ΔI_{O2}) of higher value $\Delta U_{T2} \approx 2 \div 15$ V ($\Delta I_{O2} \approx 1 \div 50$ mA).

Thus, in such a way, internal base cells with small voltage (current) swing ΔU_{T1} (ΔI_{O1}) and output **matching components (MCs)** with higher output currents ΔI_{O2} support high-speed performance of microcircuits, and high switching threshold ΔU_{T2} of input MCs contributes to better interference immunity of microcircuits. Whereas the values of internal ΔU_{T1} (ΔI_{O1}) and external ΔU_{T2} (ΔI_{O2}) logic swing levels considerably differ, the input MCs are performing as converters of logic levels from external ΔU_{T2} into internal ΔU_{T1} (ΔI_{O1}), and output matching components (MCs) generate the external levels with swing ΔU_{T2} (ΔI_{O2}) from the internal ones with swing ΔU_{T1} (ΔI_{O1}).

Along with the matching components of the said types, digital microcircuits may apply bidirectional matching components which both receive external levels with their further conversion into the internal ones and also generate external levels from the internal ones. Moreover in microcircuits, there may be applied some special matching components for the purpose of connecting the external components (quartz resonators, capacities, etc.) not implemented in the microcircuits, providing reference voltages, receipt of analog signals, etc.

1.1.2 Architecture of Internal Cells of Digital Microcircuits

Internal base cells are divided into two main groups of cells: logic cells (LC) and memory cells (MC).

Base Logic Cells Base logic cells (LC) of digital microcircuits are used for logic conversion of the input data provided in binary or in any other code and generating potential (or current) levels of output signals with electrical characteristics which correspond to the data being coded at LC output and support the LCs being joined together [1].

The most elementary architecture of base logic cell incorporates two components (Fig. 1.2): switching (toggling) component, (SC) converting input data U_I, and loading component (LC), which affords generating the relevant level of output signals U_O. Loading component (LC) may be either input signal U_I controlled (bar line in Fig. 1.2) or non-controllable one. Depending on the method of data transmission, logic cells may be divided into two big groups: asynchronous or static and synchronous or dynamic ones. The architecture of logic cells falling into the first group is shown in Fig. 1.2, and here the time of output signal U_O generation is determined by intrinsic delay time t_P of logic cell. Architecture of logic cells falling into the second group is shown in Fig. 1.3 [1], and here time t_P of output signal generation U_O is quantized at specific moments of time set by the signal frequency delivered to clock C input. Option with logic cells falling into the second group may

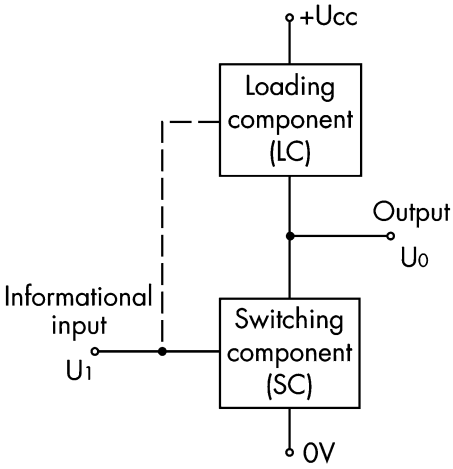

Fig. 1.2 General structure of internal base static logic cell [1]

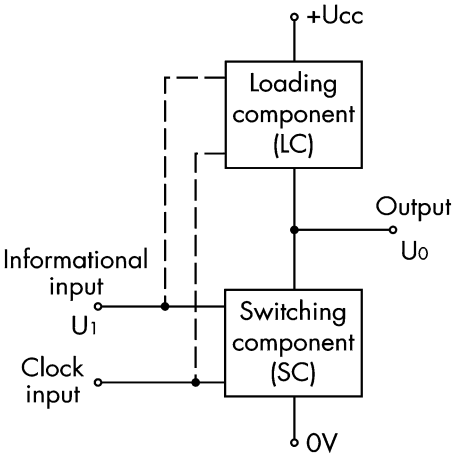

Fig. 1.3 Architecture of internal base dynamic logic cell

be implemented with a few clock inputs which is called polysynchronous. In such a logic cell, the time of input signal generation depends on the string of clock signals. Architecture of logic cell shown in Fig. 1.2 has one data input; hence it performs the simplest logic conversions of input data signal U_I. Therefore, to increase the number of logic functions, the logic cell circuit is supplemented with an additional logic component (LC).

Logic component (LC) may be introduced either at LC input (Fig. 1.4a) (LC of type CMOS, TTLS) or at LC output (Fig. 1.4b) (LC of I^2L type), and it allows generating logic function of *N* input data signals or N output functions of single input signal. The most function-ridden is the logic cell containing the logic component both at input (LC1) and output (LC2) LC (Fig. 1.4c) which enables generation of N output logic functions of M input data signals. For such LCs, however, generation of

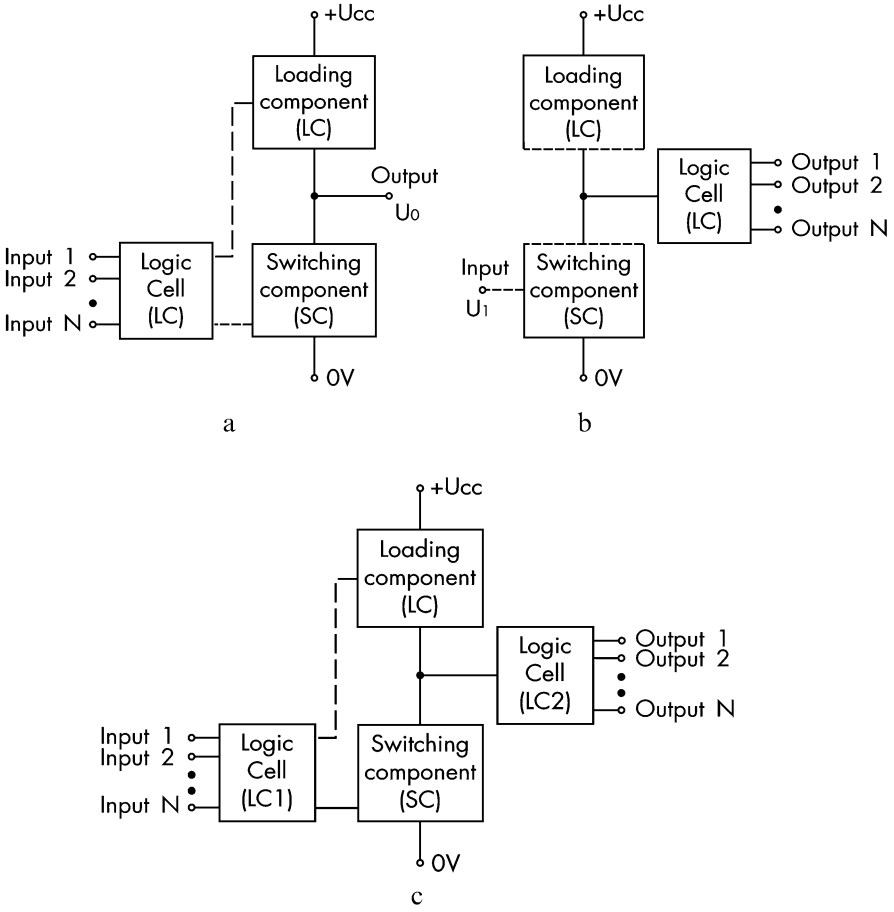

Fig. 1.4 Architecture of internal base logic cells: (**a**) multi-input; (**b**) multi-output; (**c**) multi-input\multi-output base logic cell

appropriate levels of signal and logic swing ΔU_T. appears to be quite a tricky problem.

System of parameters of internal LC incorporates:

1. *Static parameters.*

U_{0H}, U_{0L}–output voltage of signal high and low levels.
$\Delta U_T = U_{0H} - U_{0L}$–logic voltage swings.
I_{OH}, I_{OL} ~ output current of high and low level.
U_T–threshold switching voltage.
ΔU_T^+, ΔU_T^-,–reserve of interference immunity to positive and negative interferences.

I_{IH}, I_{IL}–input current of high and low levels.
N–load-carrying capacity

$$N = \min\left\{\frac{I_{OL}}{I_{IL}}; \frac{I_{OH}}{I_{IH}}\right\};$$

I^{c}_{CCL}, I^{c}_{CCH}–consumption current in static states of low and high levels.
U_{CC}–supply voltage.

2. *Dynamic parameters*.

t_{pLH}, t_{pHL}–delay time of logic cell switching at switching ON/OFF,
t_{HL} (τ_r), t_{LH} (τ_f)–front duration of logic cell switching ON/OFF,
τ_{IH}, τ_{IL}–maximum duration of input signal front/cut,
F–maximum LC switching frequency.
I_{CCF}–dynamic LC consumption current.

Since in digital microcircuits, base logic cells (LC) are responsible for major logic loading; the requirements as below are applied to them:

(a) Maximum number of logic functions performed by a single LC.
(b) High-speed performance of logic and other functions.
(c) Minimum power consumption in static and dynamic operational modes.
(d) Minimum number of circuitry components relevant for LC implementation.

Memory Base Cells In digital microcircuits the built-in memory cells (MC) are intended for saving and storage of data. In the capacity of such memory cells, both elementary memory cells with control circuits intended for storing data bulks and complex memory cells of "clock' triggers" type may be used. Depending upon the method of data storage, memory cells pertaining to the first type may be both static and dynamic ones. In MC of static type, the data saved may be stored as long as desired. The body of static memory cell is a bi-stable cell formed by cross-joining of two inverting logic cells. Block diagram of such memory cell by the example of CMOS logic cell is shown in Fig. 1.5a. Dynamic memory cells (MC) (Fig. 1.5b) incorporate one LC and an additional memory cell (MC), arranged as per charge accumulation principle with writing circuits. Having in mind that over the time on the storage component loss of charge may occur, i.e., some data may be lost, such memory cells need recurrent restoration (regeneration) of the state. Methods of MC data formation when LC of various types are in use are elaborated in [2–4].

An extensive group of memory cells used in contemporary digital microcircuits is formed by trigger circuits with two stable states which are set at providing the respective signal combination to the control inputs and held within the time set by the designer after the effect created by these signals expires. In digital microcircuits, flip-flops RS, D, JK, and T have gotten the most widespread use. Depending upon

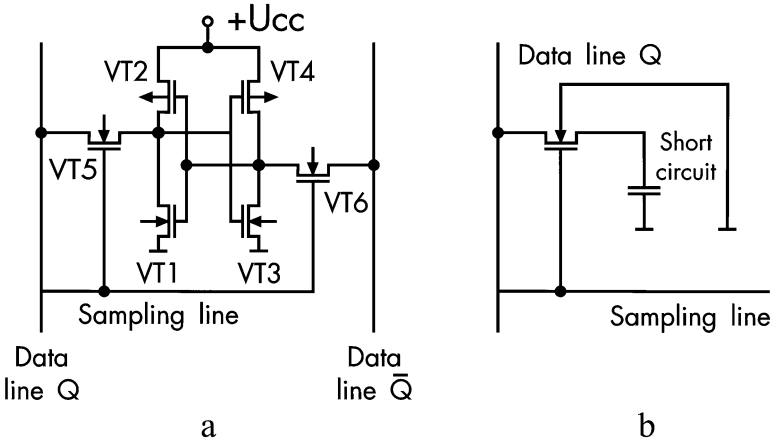

Fig. 1.5 Block diagram of the elementary memory cells (MC) of static (**a**) and dynamic (**b**) types

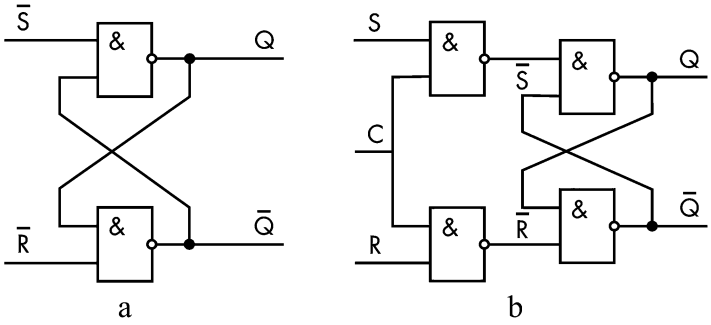

Fig. 1.6 Block diagram of unclocked RS flip-flop (**a**) and clocked flip-flop (**b**) with application of logic cell of type "NAND" [1]

the types of memory components used in flip-flops, they are divided into static, dynamic, or combined static-dynamic. If the state of flip- flop alters over entering the clock signal, then such flip-flops are referred to as "clocked flip-flops." In unclocked (asynchronous) flip-flops, toggling occurs when the relevant combination of input signals enters the control inputs. In digital microcircuits, clocked flip-flops synchronized by either signal level or signal front have gained the most extensive use.

Conventional unclocked RS flip-flop is made as the simplest bi-stable cell controlled by R&S input (Fig. 1.6a). The problem for RS triggers is that occurrence of even short pulses at inputs R, S may lead to erroneous setting of the flip-flop. Therefore, when working with RS flip-flops, one as a rule uses an additional clock signal *C*, limiting the time when inputs R, S are in active state (Fig. 1.6b).

The flip-flops clocked by signal front as illustrated by an example of Dt-type flip-flop tend to alter their state when the respective clock signal front arrives at clock input: positive or negative. At static levels of clock signal, the state of flip-flop is

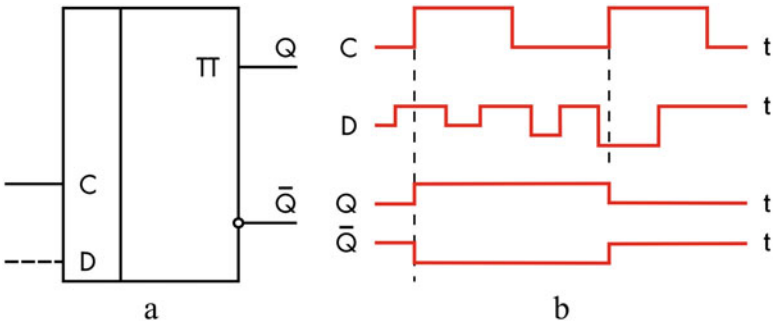

Fig. 1.7 Designation (**a**) and operational time diagrams (**b**) of signal front clocked Dt-type flip-flop

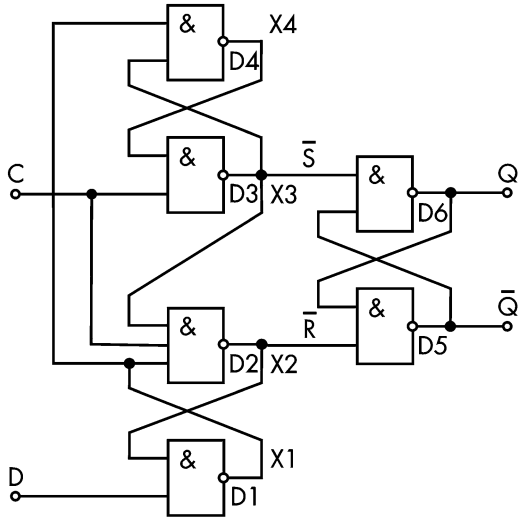

Fig. 1.8 Example of functional diagram for signal front clocked Dt flip-flop

retained irrespective of the levels of input signals. Time diagram showing operation of such flip-flop via example of Dt-type flip-flop is shown in Fig. 1.7b. An example of functional diagram of front clocked Dt-flip-flop on "NAND" logic cell is shown in Fig. 1.8 [1]. The state of flip-flops clocked by clock signal level may vary during the time when EN clock pulse is in effect when data signals enter D input. Within the pause, when EN clock signal level varies, the state of triggers does not depend on input signal levels. Designation of D-type flip-flop is available in Fig. 1.9a, and its operational time diagram is shown in Fig. 1.9b. If in the flip-flop pertaining to the said group only one output is in use, sometimes it is called "latch." An example of D-type flip-flop functional circuit clocked by signal level on the base of logic cell with function "NAND" is shown in Fig. 1.9c.

Other types of flip-flops may be generated on the base of clocked RS-type flip-flop via joining into various configurations. Thus, JK-type flip-flop is formed through sequential joining ("master-slave" type) of two RS-type flip-flops

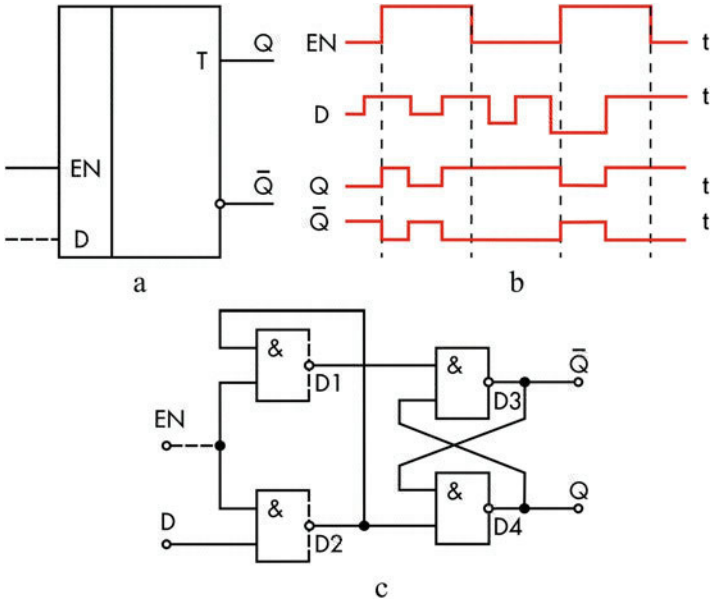

Fig. 1.9 Designation (**a**) time diagrams (**b**) and an example of functional diagram (**c**) of signal level clocked D flip-flop

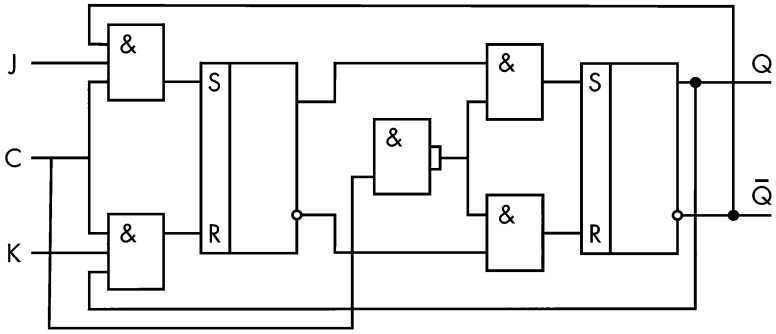

Fig. 1.10 JK flip-flop block diagram

(Fig. 1.10) by means of establishing feedbacks from outputs Q,Q of output RS-type flip-flop ("slave") to inputs R,S of input RS flip-flop ("master").

T flip-flop is created from JK flip-flop with recourse to introducing one T input linked with both outputs J, K.

In greater depth, the methods of flip-flops forming by means of logic cells of diverse types are covered in literature [1, 2, 4].

The system of memory cell (MC) static parameters is similar to the system of static parameters of internal logic cells (LC) of digital microcircuits. System of MC

dynamic parameters in addition to the system of internal LC dynamic parameters of digital microcircuits incorporates the parameters as follows:

t_L, t_H–minimum duration of clock signals of low and high levels,
t_{SU}–preset time, i.e., minimum time of providing data signal till clock signal when stable writing into memory cell takes place,
t_H–holding time p minimum time of holding data signal after providing the clock signal when steady writing in memory cell takes place.

For Memory Cells (MC) of dynamic type there is an additional parameter t_{REC} – that is maximum period of MC refreshing signal when no data is lost in the MC. Whereas in majority of cases MC circuits are built on the basis of internal base logic cells, the key requirements applied to them for further use in digital microcircuits are similar to the requirements applied to the base logic cells (LC). However, unlike base LCs where high-speed performance appears to be more critical parameter, for MC, where passive storage is the standard mode (excluding signal digital processing microcircuits), the more relevant parameter is static consumption current.

1.1.3 Architecture of Digital Microcircuit Matching Elements

Input matching components (MC) in modern digital microcircuits are intended for the following purposes: generation of internal logic levels for digital microcircuits, protection of internal chains against external electrical impacts (interferences, static discharges, etc.), gaining of external input electrical signals, storing of input signals levels at their receiving in digital microcircuits, enhancement of sensitivity level, high-speed performance, and interference immunity of digital microcircuits. Output interface elements of digital microcircuits are intended for generating external for microcircuits output voltage levels (current), generation of appropriate output signal front durations, gaining of microcircuits internal LC signals, protection of internal microcircuits chains against external electrical influences (interferences, static discharge, overloads, etc.), and temporal storing of output signal levels at their outputting from microcircuits.

Input Matching Components The major elements of input marching component are shown in Fig. 1.11.

The fundamental part of input matching component is comprised of signal level conversion circuit which transforms external input levels into internal ones, which are distinguished by microcircuit internal logic cells (LC). Therefore, input matching components may be split into two groups:

(a) Input matching components (MC) with input levels which coincide with the levels of microcircuit internal LCs (TTL input levels, TTL levels of internal LC; CMOS input levels, CMOS levels of internal LC; etc.)

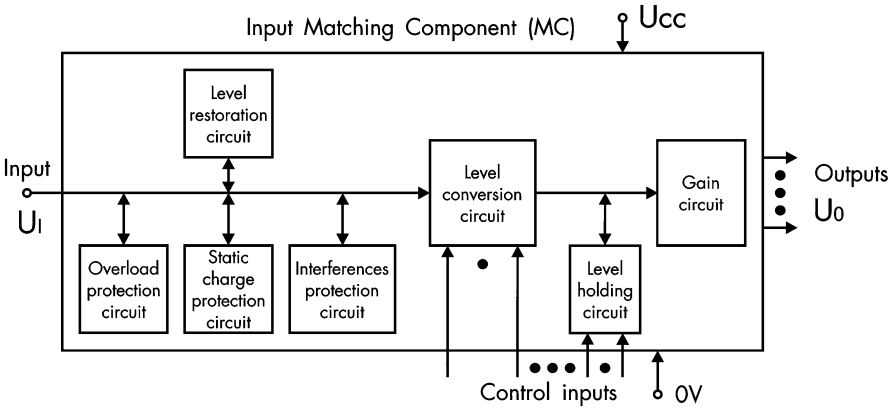

Fig. 1.11 Standard structure of input matching component (MC) of digital microcircuit [4]

(b) Input MCs with conversion of signal levels (for instance, input TTL levels, CMOS levels of internal LC; input ECL levels, TTL levels of internal LC; etc.)

Whereas there exist three most widely applied and fundamentally different systems of logic signal levels, TTL. CMOS, ECL, and I2L, hereinafter, the conversion circuits of input MC levels of the listed level types are addressed.

At MC's output, there may be introduced signal gain circuit which amplifies the input levels and generates high output currents to control greater number of LC internal inputs. Outputs of matching components may be single ones (may generate either direct or inverse signal to input one) and multiple (they may generate a few direct and inverse signals to input one). If it is necessary to store the levels of input signals, it is possible to complete input matching component with a memory cell responsible for temporal storage of input levels and their provision to matching component output by control signal. In the capacity of storage circuits, there may be used memory cells clocked by front of control signal level. For protection of the internal components from the external influences on the MC circuit there can be introduced the protection circuit from the static electricity and the protection circuit from the extreme values of currents / voltages at the MC inputs. If the MC input is connected with the signal source, that generates the noises, the special protection circuits are used, reducing sensitivity to these noises. Here the best case efficiency may be attained at implementing MC's circuit with transfer characteristic of hysteresis type.

At application of digital microcircuits, it may happen so that no fixed input levels are provided to microcircuit inputs, i.e., to microcircuit inputs an unknown potential is supplied (that is particularly dangerous for CMOS microcircuits). In such a case at MC's input there may be introduced a level recovery circuit, eliminating the "floating potential" effect at MC' input.

System of input MC's parameters consists of:
Static parameters:

I_{IH}, I_{IL}–input current of high and low levels.
l_{IA}–maximum input break down current,
I_D–current of clamp diode.
U_{TH}, U_{TL}–input threshold voltage of high and low levels.
U_{IH}, U_{IL}–input voltage of high and low levels.
U_{0H}, U_{0L}–output voltage of high and low levels.
I_{0H}, I_{OL} ~ output current of high and low levels.
N–load-carrying capacity of matching component.
$U_{I\ max}$, $U_{I\ min}$–maximum and minimum tolerable input voltages.
U_{ESD}–maximum tolerable value of electrostatic potential.
I_{CCL}, I_{CCH}–static consumption current of IC in ON/OFF state.
U_{CC}, U_{SS}–supply voltage.
0 V, U_{dd}–zero potential voltage (ground).

Dynamic parameters

t_{pHL}, t_{pLH}–delay time of MC's triggering at switching ON/OFF,
t_{HL} (τ_r), t_{LH} (τ_f)–MC's switching ON/OFF front duration,
τ_{IH}, τ_{IL}–maximum duration of input signal front/cut,
F–maximum frequency of input signal.
I_{CCF}–MC's dynamic consumption current.

Considering that in digital microcircuits input matching components do not have logic content and are intended mainly for matching purposes, they should be in compliance with the following major requirements applied to them:

(a) Maximum reserves of interference immunity against stresses produced by various noises.
(b) Minimum number of circuit elements contributing to reduction of the area taken by the matching component on a chip of digital microcircuits and to increase in the number of matching components located along the chip perimeter.
(c) Minimum conversion and matching time, i.e., delay times t_{pLH}, t_{pHL} and durations of fronts t_{HL}, t_{LH} should be of minimum value, which helps minimize the influence produced by high-speed performance of input matching components at aggregated high-speed performance of microcircuits.
(d) Minimum consumption current in static I_{CCL}, I_{CCH} and dynamic modes I_{CCF}.

The diagram of input matching component available in Fig. 1.11 contains a maximum number of functional blocks used in MC. However, depending upon modes of input MC's application in digital microcircuits, the block diagram of matching component may be simplified at the expense of excluding some separate functional blocks and circuits depending upon application conditions of microcircuits.

Input Matching Major components of output MC's architecture are shown in Fig. 1.12.