Springer Handbook of Semiconductor Devices

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Springer Handbook of Semiconductor Devices

With 1335 Figures and 71 Tables

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Foreword by Chihiro Hamaguchi

The first semiconductor device, named "point-contact transistor," was demonstrated on the 17th of December 1947 by John Bardeen, Walter Brattain, and William Shockley at Bell Laboratories. About a month later (January 1948), Shockley invented the "junction transistor." The first demonstration of a radio receiver made with point-contact transistors was performed in December 1947. The design of solid-state devices for electrical amplification was organized at Bell Laboratories under the guidance of Shockley, who was also interested in a new device to control surface electrons with a metal gate. A FET-like transistor had already been patented in the USA by Julius Edgar Lilienfeld in January 1930; the idea was not realized because of the high density of surface states in silicon. The difficulty was resolved by using an oxide surface layer processed in high-temperature vapor atmosphere, as proposed by C. Frosch in 1954; the deposition of a metal gate on the oxide layer was achieved by J. Attala and D. Kahng at Bell Laboratories in 1959. First, PNP and NPN junction transistors were commercialized and used to design solid-state circuits; however, the Si-MOSFET, invented afterwards, revealed its superiority over the junction transistor, in view of designing and manufacturing digital circuits.

So many people were involved in the early development of integrated circuits (ICs); among them, Jack Kilby of Texas Instruments (hybrid integrated circuit, 1958) and Robert Noyce at Fairchild Semiconductor (monolithic integrated circuit, 1959) played a very important role in the opening of IC technologies. The advancement of IC technology is well explained by Moore's law: "the number of transistors in a chip of integrated circuits doubles every two years." Moore's expectation expresses quite well the history of ICs from 1970 till 2020. This advancement has been supported by many new technologies, materials, processes, circuit-design strategies, and others. Starting from the simple planar technology, structures are now more complex and three dimensional. The technological revolution in the field of the semiconductor devices radically changed many aspects of the social organization (communications, economy, transportation, and all the primary necessities of everyday life), so that in the present time, human beings find it difficult to survive without ICs.

Semiconductor-device operations are based on fundamental electrical and optical properties of the materials, as anyone can easily agree about just by leafing through this *Springer Handbook of Semiconductor Devices*. The knowledge of energy band structures is essential for understanding any device operation. In other words, energy band calculations provide knowledge on electronic and optical properties of semiconductors. Many semiconductor properties are well understood on the basis of the effective masses of electrons in the conduction band and holes in the valence bands, in addition to the (direct or indirect) band gap. Pioneer data from cyclotron resonance experiments in Ge and Si were interpreted by the theory based on $k \cdot p$ perturbation method by G. Dresselhaus, C. F. Kip, and C. Kittel in 1955, and revealed the many-valley structure of the conduction band and the spin-orbit splitting of the valence bands in these elemental semiconductors. The energy band calculation in the full Brillouin zone for 14 semiconductors of the diamond and zinc-blende structures was reported for the first time by M. L. Cohen and T. K. Bergstresser in 1966 by means of the pseudopotential method. More advanced theoretical approaches have been reported afterwards, and some of them are dealt with in this handbook.

This *Springer Handbook of Semiconductor Devices* provides a quite useful framework suitable to guide the interested reader across a massive amount of information, and achieves an almost complete review of the basic and advanced knowledge of semiconductor devices. The editors planned to cover the present status and future development of semiconductor devices, including physics, structures, processing, designing, and simulation. Part I is concerned with the technological aspects of semiconductor devices, and deals with the manufacturing of semiconductor memory devices together with the technology of processing, measuring parameters, advanced lithography, and dielectric materials. In addition, FinFETs and advanced technologies for future materials and devices are discussed. Part II deals with basic semiconductor devices and applications, including Si-based devices such as MOS devices, MOSFETs, capacitors, and CCDs. Part II also deals with the topics of sensors, semiconductor lasers, and solar cells. Part III deals with new-generation devices and architectures, such as resonant-tunneling devices, bioelectronics, spin-based devices, quantum-computing devices, and other innovative structures. Part IV is devoted to device modeling and process simulation, where both classical device-simulation tools and more advanced methods are described in detail.

Even though many kinds of semiconductor devices are still designed and produced, and new and advanced devices are expected to appear in the future, this handbook can be considered a milestone reference, since it covers a large spectrum of devices and surveys their structures and properties in depth. The editors selected the topics cleverly, and the contributors are specialized and outstanding scientists from all over the world. Therefore, on the basis of my experience in this field, I consider this *Springer Handbook of Semiconductor Devices* the most important guide book for researchers, in industries and academic institutes, as well as graduate students. I congratulate the editors and all the authors for bringing such an excellent handbook to publication.

Professor Emeritus at Osaka University
IEEE Life Fellow
March 2021

Chihiro Hamaguci, Ph. D.

Foreword by Herman Maes

I was born in the year 1947, the blessed year so to speak of the revolutionary invention of the point-contact transistor by Shockley, Bardeen, and Brattain. Perhaps this explains my fascination to this day for semiconductors, the physics, the devices, and the technology, in that order. I had the pleasure to admire this first "transistor" at the Bell Labs in Murray Hill, New Jersey. I moreover have had the privilege to meet John Bardeen and attend a few of his classes during my postdoctoral research stay at University of Illinois Champaign-Urbana in 1974–1975. I even had a brief, accidental encounter with William Shockley in 1974. I graduated as an electronic engineer at the Katholieke Universiteit Leuven, Belgium, in 1971 at a time when the semiconductor industry had in fact only just come out of the starting blocks. Intel just launched its Intel 4004, the first processor-on-chip consisting of 2,300 transistors. We were still within the first phase of the semiconductor saga, a few years after Gordon Moore had reported his findings on the evolution in size of the first integrated circuits (IC) and launched his predictions, later known as Moore's Law. Only on the basis of a few data points, Moore concluded and predicted that the number of transistors in ICs on a chip would double every year with innovations in lithography as the main driving force to enable transistor scaling. How more visionary could a man be? And exactly these kinds of bold statements have been so typical and have, as we experienced, in fact been driving the development of this fascinating semiconductor technology field over the past nearly 65 years. This is commonly referred to as self-fulfilling prophecy.

During our engineering training in the late 1960s, a somewhat older professor, close to retirement, actually strongly doubted whether those semiconductors would eventually break through and therefore still spent a lot of attention to the usefulness, properties, and application of vacuum tubes. Fortunately for us, there was this other, young, dynamic, visionary professor, Roger Van Overstraeten (the founder of imec in 1984), who had obtained his

Ph.D. from Stanford University and who had returned a few years earlier to our university. He was so enthusiastic and inspiring about the latest developments and opportunities of semiconductor science and technology that he could convince many of us to fully engage ourselves in that direction. My fascination was aroused and from then gradually turned into passion and hunger for knowledge. So, we started to look for suited books. In these early years, appropriate textbooks were still scarce. The books that were being produced mostly focused on specific technological and solid-state physics issues. I personally remember a few of these while in college, the SEEQ series on the bipolar transistor, Andy Grove's *Physics and Technology of Semiconductor Devices*, and of course Simon Sze's standard work *Physics of Semiconductor Devices*, which saw its first edition in 1969. Over the past 50 years, numerous new handbooks have become available, many of them covering in detail specific disciplines or aspects of the strongly expanding field of semiconductor devices. However, at this early stage there was a need of books providing a broad-scope and balanced mixture of state-of-the-art, prospect, insight and context of all inherent aspects of semiconductor technology, devices and applications, offering high level treatments with more than mere encyclopedic knowledge, with attention to interdisciplinary aspects and to the mutual support of the various disciplines: such books, in fact, remained rather scarce.

After about 45 years in the twentieth century and 20 years in this twenty-first century, the industrialized world has been marked by extremely rapid technological (r)evolutions. We witnessed the incredible and far-reaching developments of the semiconductor industry with growing amazement and disbelief, even to those who were involved in the process from the first rank. This was largely due to the extremely successful scaling endeavors by research and industry. The Intel 4004 processor that we referred to earlier was realized in the 10 μm technology node, today we have reached the 5 nm node (a feature size scaling by 2,000), allowing fabrication of chips with over 50 billion transistors! Semiconductor technology today is a very mature, established industrial discipline. The entire semiconductor market is close to 500B$ and expected to further grow year after year, with even a doubling in 10 years' time. This industrial progress went hand in hand with (and was also steered by) profound societal changes in its most diverse aspects and led us into the Information Age. Semiconductor devices, ICs, and products played an undeniably prominent role in these tremendous transitions. They are now used in every corner of our "digital" society and are taking an increasingly crucial and essential role in almost all economic sectors, information technology, multimedia, communication, automation, robotics, transport, medical and health sector, games, education, environment, energy, cryptography, smart buildings, and smart cities.

But we are today on the verge of a new disruptive landslide. The transition from the Information Age to the Digital Age is taking place, with expected revolutions in the interfaces for speech recognition, augmented reality, virtual reality, and artificial intelligence, just to name a few. Our businesses and the economy will have to realize that this transition will not come gradually, in small steps. After all, a characteristic of a revolution is that the change comes abruptly and is accompanied by breaking with the past. And if we had thought to have reached the pinnacle of technologically possible developments, we realize that many even more far-reaching technological breakthroughs will be needed in the future.

The semiconductor industry is facing a new era in which device scaling and cost reduction will no longer continue to proceed on the path followed for the past few decades. Further advanced nodes, even when feasible, may no longer bring the desired cost benefit. Moreover, R&D investments in new lithography solutions and devices below 5 nm nodes are rising substantially. Therefore, the insatiable and ever-increasing demand in the digital era forces the industry to come up with ever more innovative and sophisticated technology solutions to bridge the gap and improve cost/performance while at the same time adding more functionality through integration. The so-called More-than-Moore devices (including

MEMS and sensors, CMOS Image Sensors, power devices, THz devices) represent this new functional diversification of technologies, combining performance, integration, and cost not merely limited to CMOS scaling. Their role is expected to become more and more predominant. Semiconductor device and technology engineers and scientists will therefore have to continue the quest for ingeniously new electronic devices and functionalities. We are in fact on the cusp of big changes.

More than ever, semiconductor researchers, scientists, and engineers will have to maintain the widest possible view of these rapidly evolving fields. They need to be constantly and continuously curious, interested, amazed, fascinated, and triggered by the evolution and the developments in their own fields but also in the domains adjacent but often complementary to their own specialization. They therefore need to acquire thorough yet easy-to-digest, appropriate, timely, and reliable knowledge on the state of the art but also on the newest developments and trends in these domains. And above all, they count on obtaining this information from specialists and experts in these fields.

A handbook is a book capable of being conveniently carried as a type of ready reference work, providing information, facts, insights, and instructions on a particular field, subject, or technique, designed to be easily consulted and providing useful, quick, but solid and reliable answers in a certain area. It covers and offers scientific basics, fundamentals, methods of research, general principles, functional links, and review of established or potential applications. Moreover, even in rapidly expanding fields, the information and content need to be sufficiently timeless.

Springer Handbooks respond to such needs fully and successfully. They strive to provide and maintain the highest standards of references in well-selected fields and key areas of physical and applied sciences and technology. They are intended for practitioners in academia and industry, as well as graduate students. They are allowing fast yet comprehensive review and easy retrieval of reliable key information.

It is Springer Handbooks' tradition to come up *at the right time* with new, well-considered initiatives for launching appropriate reference books. Recent examples have been the handbooks on nanotechnology, robotics, mechanical engineering, and automation.

Today certainly is the right time to launch this Springer Handbook on semiconductor devices, considering the transition to the even more challenging post-scaling era.

Conceiving and realizing such a handbook is a daring, challenging, and ambitious endeavor. It is a major undertaking and requires vision, significant organizational skills, and commitment. One also needs to have a network of experts who look up to the editor.

This Springer Handbook on semiconductor devices you have in hand fully meets the strict requirements and high-level standards of the Springer Handbook series. It provides comprehensive coverage of numerous technological and fabrication aspects of advanced semiconductor devices, focusing not only on advanced "traditional" structures but also on ingeniously new and often futuristic, beyond CMOS, and More-than-Moore concepts for many applications. Rightly so, strong attention was paid to the indispensable advanced modeling and simulation methods for predictive and supporting purposes, as well as an outlook toward near or far future needs. This handbook is not the first one covering semiconductor technology and device disciplines, and it will undoubtedly not be the last one. But the differentiator, the USP of this handbook according to me, is this mixture of broad scope, thoroughness of treatment with still sufficient accessibility, the wide range of concepts for many applications, and the foresight. And, worth noting, all chapters have been written by international experts, innovators, and leaders in their field. The reasoned interpretations of developments in each area are commendable and often unique. The editors did a wonderful and tremendous job in not only selecting the 45 rightful and relevant topics but also in inviting the right specialists to treat these topics and share their expertise and experience with the knowledge-hungry reader.

This has resulted in an extensive, voluminous yet digestible standard work that deserves to be on the shelf of graduate students of nanoelectronics, and researchers in academia and industry who are active or intend to be active in this field and who are looking for in-depth, up-to-date information. Finally, also practicing scientists and engineers who want to expand their know-how in adjacent fields will strongly benefit from this book.

I would like to congratulate the editors and all the authors for their excellent contributions, one by one, bringing this ambitious and formidable challenge to a successful conclusion.

Professor Emeritus Katholieke Universiteit Leuven, Belgium Herman E. Maes, Ph.D.
Former Senior VP imec, Leuven, Belgium
March 2021

Preface

No other class of materials than semiconductors, since the early identification of their electrical, optical, and thermal properties at the beginning of the nineteenth century, has been so deeply investigated and used to design all kinds of devices. The first theoretical models about the physics of semiconductors, based on quantum-mechanical grounds, fueled the design of solid-state diodes and transistors; these, in turn, have opened new horizons to electronics, computer science, and sensors, and have greatly impacted the global market with annual revenues of the order of 500 billion US dollars in the present days.

In turn, semiconductor companies pushed ahead the search of new semiconductor materials and structures suited for specific applications, and urged academia and the industry's R&D toward the elaboration of more and more powerful simulation tools to inquire about the effects of miniaturization, interfaces, and doping on device performance and reliability, or to benchmark specific semiconductor properties before investing resources in expensive innovations of the production lines.

All the above justify the effort of putting together, in this *Springer Handbook of Semiconductor Devices*, many cross-disciplinary competences about present-day and near-future semiconductor devices, namely modern concepts in solid-state physics, material science, growth and process technology, device design, and advanced simulation strategies.

When we speak about semiconductor devices, what we consider "future" is very often already "present time" somewhere in the world. Thus, this handbook not only includes the most recent progress in research and technology of conventional semiconductor devices and sensors but enlarges its view to include some specific topics related to new materials and designs, presently at the frontier between science and technology, nonetheless suitable to be employed in the next-generation semiconductor-technology challenges.

The handbook is organized in four parts: 1. Technological Aspects; 2. Basic Devices and Applications; 3. New-Generation Devices and Architectures; 4 Modeling. Almost 100 leading scientists from both academia and industry were invited to contribute to the 45 chapters of the handbook, which has been conceived for professionals and practitioners, material scientists, physicists, and electrical engineers working at universities, industrial R&D, and production. Each chapter is self-contained and refers to related topics treated in other chapters when necessary, so that the reader interested in a specific subject can easily identify a personal path through the massive contents of the handbook.

We are very grateful to all the authors who joined this ambitious enterprise, to the referees who generously contributed to improve the quality of the final outcome, to Springer's editors who patiently followed our work step by step, and, last but not least, to Prof. Chihiro Hamaguchi (Osaka University) and Prof. Herman Maes (KU Leuven and imec) for providing forewords based on their long-term experience in the field of semiconductor science and technology.

May 2021 M.R., R.B., S.R.

Contents

Part I Technological Aspects 1

1 CMOS Manufacturing Processes 3
Aaron Douglas Lilak and Patrick H. Keys

2 Semiconductor Memory Technologies 37
Paolo Fantini, Giorgio Servalli, and Paolo Tessariol

3 BCD Process Technologies 67
Giuseppe Croce, Antonio Andreini, Paola Galbiati, and Claudio Diazzi

4 Measuring Techniques for the Semiconductor's Parameters 117
Alessandra Alberti, Filippo Giannazzo, Francesco La Via, Salvatore Lombardo, Antonio M. Mio, Giuseppe Nicotra, Stefania M. S. Privitera, Riccardo Reitano, Fabrizio Roccaforte, Corrado Spinella, and Emanuele Rimini

5 Interconnect Processing: Integration, Dielectrics, Metals 169
Shyng-Tsong Chen, Nicholas A. Lanzillo, Son Van Nguyen, Takeshi Nogami, and Andrew H. Simon

6 Wet Chemical Processes for BEOL Technology 219
Cornelius Brown Peethala, James J. Kelly, Donald F. Canaperi, Mahadevaiyer Krishnan, and Takeshi Nogami

7 From FinFET to Nanosheets and Beyond 259
Nadine Collaert

8 Advanced Lithography 279
Alberto Roncaglia

9 Advanced Technologies for Future Materials and Devices 309
Francis Balestra

Part II Basic Devices and Applications 329

10 MOS Capacitors, MOS Transistors, and Charge-Transfer Devices 331
Massimo Rudan, Susanna Reggiani, and Giorgio Baccarani

11 Electrostatic Doping and Devices 371
Raymond J. E. Hueting and Gaurav Gupta

12 Planar MOSFETs and Their Application to IC Design 391
Salim El Ghouli and Denis Rideau

13 Silicon Power Devices 423
Noriyuki Iwamuro

14 Silicon Carbide Power Devices 491
B. Jayant Baliga

15 GaN-Based Lateral and Vertical Devices 525
Matteo Meneghini, Srabanti Chowdhury, Joff Derluyn, Farid Medjdoub, Dong Ji, Jaeyi Chun, Riad Kabouche, Carlo De Santi, Enrico Zanoni, and Gaudenzio Meneghesso

16 Bipolar Transistors and Silicon Diodes 579
Jean-Michel Sallèse and Farzan Jazaeri

17 Memory Challenges 603
Carlo Cagli and Luca Perniola

18 Silicon Sensors 635
Benedetto Vigna, Ernesto Lasalandra, Sarah Zerbini, and Mario Aleo

19 Solar Cells 699
Stephen M. Goodnick and Christiana Honsberg

20 X-Ray Detectors 747
Safa Kasap and Zahangir Kabir

21 Photodetectors Based on Emerging Materials 777
Jiantong Li and Mikael Östling

22 Terahertz Electronic Devices 807
Frédéric Aniel, Gregory Auton, David Cumming, Michael Feiginov, Sebastian Gebert, Tomás González, Chong Li, Alvydas Lisauskas, Hugues Marinchio, Javier Mateos, Christophe Palermo, Aimin Song, Jeanne Treuttel, Luca Varani, and Nicolas Zerounian

23 Semiconductor Lasers 851
Martin R. Hofmann and Stephan W. Koch

Part III New-Generation Devices and Architectures 865

24 Heterojunction Tunnel Field-Effect Transistors 867
Paolo Paletti and Alan Seabaugh

25 Carbon-Based Field-Effect Transistors 905
Zhenxing Wang, Daniel Neumaier, and Max Christian Lemme

26 Negative Capacitors and Applications 931
Muhammad Ashraful Alam, Nicolò Zagni, Atanu Kumar Saha, Niharika Thakuria, Sandeep Thirumala, and Sumeet Kumar Gupta

27 Flexible Electronics and Bioelectronics Devices 959
Chen Jiang, Xiang Cheng, Hanbin Ma, and Arokia Nathan

28 Biodegradable Electronics 1019
Giovanni Antonio Salvatore, Lan Yin, and Fanqi Dai

29 Resistive-Switching Memories 1043
Peng Huang, Yudi Zhao, and Jinfeng Kang

30 Phase-Change Memories 1093
Enrico Piccinini and Carlo Jacoboni

31 Spin-Based Devices for Digital Applications 1123
Viktor Sverdlov and Siegfried Selberherr

32 Memristive/CMOS Devices for Neuromorphic Applications 1167
Valerio Milo, Gerardo Malavena, Christian Monzio Compagnoni, and Daniele Ielmini

33 Nanoelectronic Systems for Quantum Computing 1201
David K. Ferry

Part IV Modeling 1231

34 Compact/SPICE Modeling 1233
Wladek Grabinski and Daniel Tomaszewski

35 Process Simulation 1259
Jürgen Lorenz and Peter Pichler

36 A Digital Twin for MEMS and NEMS 1303
Jan G. Korvink, Kirill V. Poletkin, Yongbo Deng, and Lihong Feng

37 Macroscopic Transport Models for Classical Device Simulation 1335
Johann Cervenka, Robert Kosik, Markus Jech, Martin Vasicek, Markus Gritsch, Siegfried Selberherr, and Tibor Grasser

38 Grid Generation and Algebraic Solvers 1383
Aurelio Giancarlo Mauri, Benedetta Morini, Simona Perotto, and Fiorella Sgallari

39 Spherical Harmonics Expansion and Multi-Scale Modeling 1413
Bernd Meinerzhagen and Christoph Jungemann

40 Charge Transport Models for Amorphous Chalcogenides 1451
Rossella Brunetti and Massimo Rudan

41 Application of the $k \cdot p$ Method to Device Simulation 1491
Antonio Gnudi, Elena Gnani, Susanna Reggiani, and Giorgio Baccarani

42 *Ab initio* Methods for Electronic Transport in Semiconductors and Nanostructures 1515
Massimo V. Fischetti, William G. Vandenberghe, Maarten L. Van de Put, Gautam Gaddemane, and Jingtian Fang

43 Quantum Transport in the Phase Space, the Wigner Equation 1559
Jean Michel Sellier and Philippe Dollfus

44 The Nonequilibrium Green Function (NEGF) Method 1583
Kerem Y. Camsari, Shuvro Chowdhury, and Supriyo Datta

45 Tight-Binding Models, Their Applications to Device Modeling, and Deployment to a Global Community 1601
Gerhard Klimeck and Timothy Boykin

Index 1641

About the Editors

Massimo Rudan received a degree in electrical engineering in 1973 and a degree in physics in 1976, both from the University of Bologna, Italy. His research interests are in the field of physics of carrier transport and numerical analysis of semiconductor devices and solid-state sensors. In 1986, he became a visiting scientist, on a one-year assignment, at the IBM Thomas J. Watson Research Center at Yorktown Heights, NY, studying the discretization techniques for the Boltzmann transport equation. In 1990 he became Full Professor of Electronics, and in 2021 Professor Emeritus, at the University of Bologna. An IEEE Life Fellow, and a recipient of the 1998 Körber Foundation Award, Massimo Rudan has coordinated several research projects funded by the European Commission, international companies and foundations, the National Council of Research, and the National Ministry of University and Research.

Rossella Brunetti received her master's degree cum laude in physics in 1981 and her Ph.D. degree in physics from the University of Modena, Italy, in 1987. Since 2002, Rossella Brunetti is Associate Professor of Condensed Matter Physics in the Department of Physics, Informatics and Mathematics at the same university. Her research activity has mainly been focused on charge transport, in both semi-classical and quantum conditions, in semiconductor structures and devices. Rossella Brunetti is experienced in a variety of numerical techniques (mainly the Monte Carlo, Molecular Dynamics, and Hydrodynamic Methods) which have been applied to validate theoretical models against experiments and to predict new effects. In the past few years, Rossella Brunetti focused her research on transport properties of chalcogenide materials in view of their applications in the field of emerging memory devices.

Susanna Reggiani received her Ph.D. degree in electrical engineering from the University of Bologna in 2001. Since 2001, she is with the Department of Electronics and the Advanced Research Center for Electronic Systems (ARCES) at the same university. Her scientific activity has been devoted to the physics, modeling, and characterization of electron devices, with special emphasis on transport models in semiconductors. She has been involved in projects dealing with TCAD analysis of power MOSFETs, modeling and characterization of hot-carrier stress degradation and reliability of wide-bandgap semiconductors, and modeling of package influences on high-voltage ICs. In 2020, she became full professor in the School of Engineering at the University of Bologna.

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Part I

Technological Aspects

1 CMOS Manufacturing Processes

Aaron Douglas Lilak and Patrick H. Keys

Contents

1.1 Introduction . . . 3

1.2 CMOS FinFET Process . . . 4

1.3 Ion Implantation . . . 4
1.3.1 Beam Line Ion Implant . . . 4
1.3.2 Ion Stopping . . . 5
1.3.3 Amorphization and Channeling . . . 5
1.3.4 Impact of Implant Process Knobs upon Resultant Distributions of Implanted Ions and Implant Damage . . . 8
1.3.5 Consideration for Implant into Nonplanar Surfaces . . . 10
1.3.6 Plasma Implant . . . 10
1.3.7 Implant Sputtering and Backscattering . . . 11
1.3.8 Implant Ion Beam Mixing . . . 12

1.4 Thermal Annealing . . . 12
1.4.1 Annealing Methods . . . 12
1.4.2 Diffusion . . . 14
1.4.3 Dopant Activation/Clustering/Deactivation . . . 16
1.4.4 Semiconductor Recrystallization . . . 17
1.4.5 Simulators . . . 17
1.4.6 Oxidation . . . 17
1.4.7 Solid Source Diffusion . . . 17

1.5 Deposition . . . 17
1.5.1 Deposition Methods . . . 17

1.6 Etch . . . 19
1.6.1 Wet Etch . . . 19
1.6.2 Dry Etch . . . 20
1.6.3 Chemical Mechanical Polish or Chemical Mechanical Planarization . . . 20
1.6.4 Etch Selectivity . . . 20
1.6.5 Atomic Layer Etch . . . 21
1.6.6 The Coloring Problem . . . 21

1.7 Lithography . . . 21
1.7.1 Fundamental Lithographic Process . . . 22
1.7.2 Lithographic Constraints Due to Light Source . . . 22
1.7.3 The Role of the Stepper/Scanner and Impact to Feature Resolution . . . 23
1.7.4 The Role of Resist in Lithographic Process . . . 23
1.7.5 Lithographic Enhancement Techniques . . . 23
1.7.6 Multiple Patterning Approaches . . . 24
1.7.7 Post-optical Lithographic Techniques . . . 27

1.8 Metalization and Contact Formation . . . 29
1.8.1 Silicide Contact to Transistor . . . 29
1.8.2 Interconnect Stack . . . 30
1.8.3 Damascene Metal Processes . . . 31
1.8.4 CMOS Process Technology Development through Nontraditional Techniques . . . 31
1.8.5 Substrate Engineering and Hybrid CMOS Integration . . . 32
1.8.6 Stress Engineering . . . 34

1.9 Summary . . . 35

References . . . 35

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Abstract

In this chapter, we will discuss the common fabrication processes and methods utilized in the fabrication of CMOS devices. This discussion will include doping techniques such as ion implantation and diffusion along with a discussion of etch, deposition, and lithography techniques used to pattern and fabricate devices at the nanometer scale. This chapter will conclude with a survey of foreseeable changes which are emerging in regard to semiconductor manufacturing processes.

Keywords

Semiconductor processing · TCAD · Etch · Deposition · Lithography · CMOS · Ion implantation · Stress engineering · Oxidation

1.1 Introduction

Over the last 70 years, transistors have progressed from being manufactured by hand out of chunk of germanium, gold foil, and glue at Bell Labs to the integrated devices which

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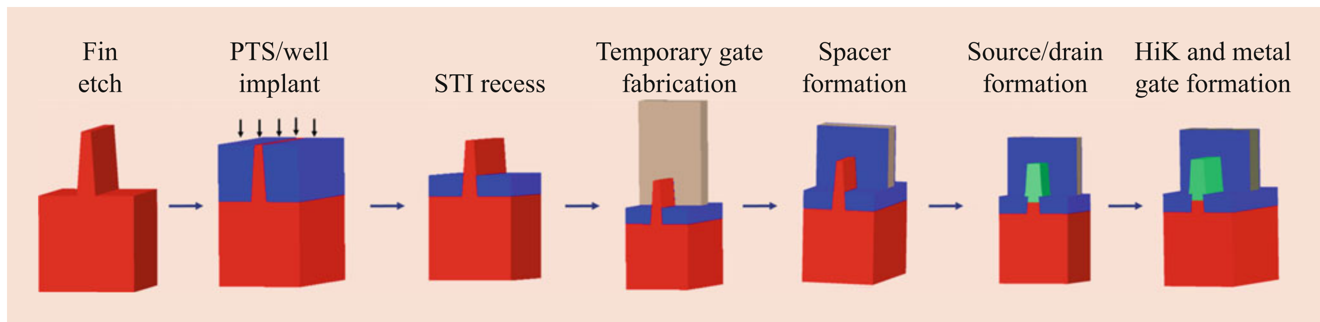

Fig. 1.1 Example process steps of a FinFET transistor fabrication flow using a variety of process techniques

have densities measured in the billions/cm^2 and emerge from multi-billion dollar facilities that look more like hospitals than factories. This chapter will discuss the manufacturing processes used to create these devices at such scale and quantity.

This discussion will begin with an introduction to doping and activation techniques including ion implant and diffusion. As semiconductor assemblies are built in a layer-by-layer manner by adding and subtracting materials and dopants, the tools used for deposition, etch, and lithography will be described. Finally, a discussion of foreseeable process-related trends will conclude this chapter.

1.2 CMOS FinFET Process

The fabrication of transistors is more an art than it is a science; however, these fabrication processes do tend to follow a similar series of operations. While there are embodiments and numerous variations of these steps and operations and resultant geometries; a (much) simplified block process flow for fabrication of a FinFET transistor through front-end fabrication is shown in Fig. 1.1. The operations and flow variations required to implement these processing steps and those required to add electrical interconnections in the back-end fabrication are described within this chapter.

1.3 Ion Implantation

Ion implantation is a means of material modification used in semiconductor fabrication. This material modification may be done for purposes of introducing doping, creating regions of damage, removal of material or cleaning of a surface, modification of etch properties of a material, or for purposes of intermixing a material surface in order to modify a subsequent deposition process. Ion implantation is utilized in both front-end and back-end processes. Ion implantation tools are broadly categorized as either beam line or plasma immersion tools.

1.3.1 Beam Line Ion Implant

Beam line ion implantation tools used in modern CMOS fabrication can trace an origin to the ion implantation device patented by William Shockley in [31] . In his patent “Forming Semiconductive Devices by Ionic Bombardment,” Shockley first illustrates how atoms of one material may be ionized from a gas phase, accelerated to a known energy with an applied voltage, and then implanted into a semiconductor wafer.

In Shockley’s original patent, a gas containing a dopant specie, for example, boron trifluoride, is allowed to flow into the assembly through tubing indicated as (22) in Fig. 1.2. Atoms of this gas are ionized and accelerated through use of an applied voltage between a cathode (32) and an anode (31). A wafer (25) is placed on the holder assembly (26) and conductive base (48, 49). By manipulating the flow rate of gas and arc used to ionize the particles, a beam current may be adjusted. This current may be measured as it exits the conductive base in the implanter and is a measure of the number of implanted charges and hence related to the number of implanted impurity ions. By adjusting the voltage applied between the cathode and anode, the energy of each implanted ion may be manipulated in order to change the range and distribution of the implanted ions. The ions may be introduced at a tilt or rotation by manipulating the orientation of the wafer holder assembly.

Modern ion implantation tools like in Fig. 1.3 have evolved from this basic configuration of Shockley, but share the same fundamental concepts. Mass selection is accomplished through passing the ion beam through a magnetic field and series of apertures. Additional magnets and computerized control enable the shaping of the ion beam, and the beam can be rastered across the wafer. Single-wafer tools have evolved into batch process tools which mount wafers on a rotating assembly and can process

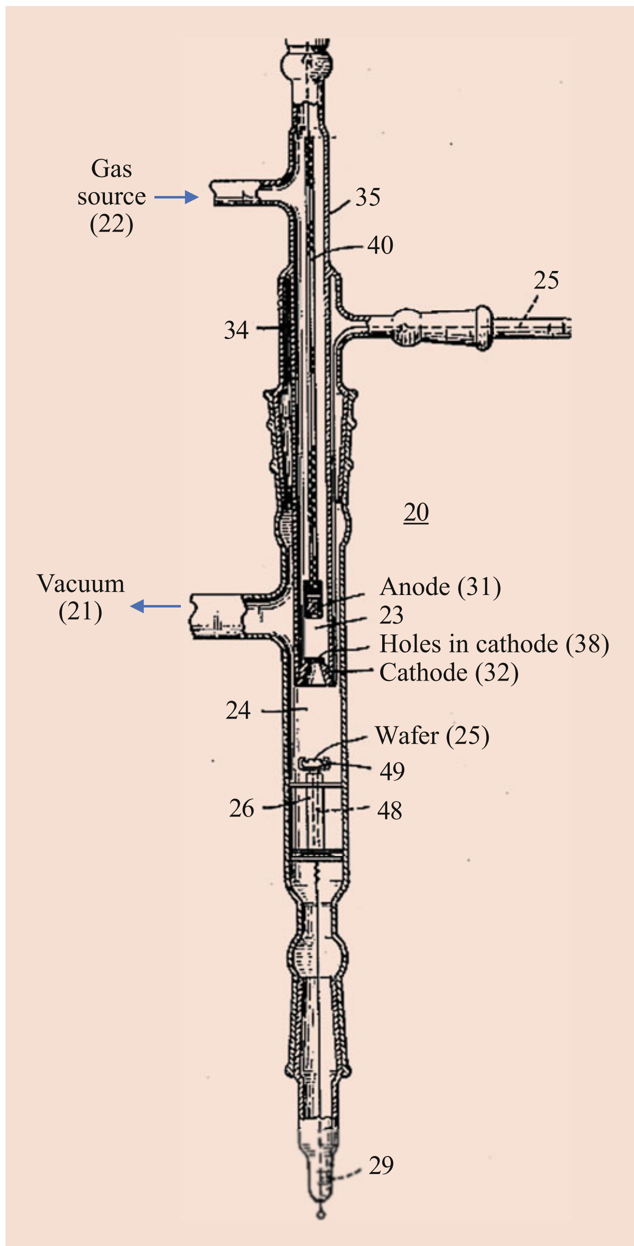

Fig. 1.2 The ion implanter assembly proposed in Shockley's original patent for an ionic bombardment apparatus. Most of the functional elements of this crude device are in place in modern ion implanters

multiple wafers simultaneously. Wafer temperature can now be adjusted during the implant process, and specialized tools have been developed for high-current, high-voltage, and other applications.

While ion implantation was initially largely integrated in CMOS processes for the purposes of introducing doping, it has since evolved as a means of material modification. Particularly in the BEOL metallization and contact processes, beam line implant continues to find new applications. A representative list of implant species from the periodic table is shown in Fig. 1.4.

1.3.2 Ion Stopping

An implanted ion interacts with both the electrons and atoms in a target material and loses kinetic energy at a rate of dE/dx in a process referred to as stopping. Nuclear stopping involves interactions with the atoms of the target material, and electronic stopping involves interactions with the electrons of the target material, and the total stopping is represented by the sum of the two components. Several derived and empirical relationships have been proposed to express these nuclear and electronic stopping components. These stopping powers may be simulated with the aid of a computer program such as SRIM as shown for silicon in Fig. 1.5.

1.3.3 Amorphization and Channeling

For a single-crystal semiconductor material, the stopping power of the crystal to the implanted ion can vary significantly as the orientation of the beam relative to the crystal surface is changed. Ion implanters enable this orientation adjustment through tilt of either the ion beam or surface of the wafer relative to the ion beam and through rotation of the wafer relative to the ion beam. Ions which experience a relatively lower stopping power are referred to as being channeled. Channeling is common for low-dose implants such as V_t adjust or well implants or for implants of lower-mass species such as boron.

Plots such as that of Fig. 1.6 indicate a very significant implant beam orientation dependence to the resultant implant profile. A fluctuation of less than a degree in tilt or rotation or slight fluctuation in wafer orientation can result in a significant difference in a channeled tail. This effect can result in a fabrication process with very high sensitivity to implant beam orientation or with significant process fluctuation. One approach to alleviate this sensitivity is to intentionally implant highly channeled implants such as boron wells (P-well) in an off-channel orientation such as 7 degrees tilt or 7 degrees tilt/22 degrees rotation for a (100) orientated silicon crystal where possible. This effect is shown in Monte Carlo simulation in Fig. 1.7.

Amorphization refers to the process of accumulating damage within an ordered crystalline or polycrystalline material until the atomic positioning within the crystal becomes randomized. A randomized crystal will not experience channeling on ions. Ion implantation is a common means used for amorphizing semiconductor crystals due to ability to adjust the depth of amorphization through the use of ion energy, the ability to determine the area of amorphization through the use of lithography to pattern implant blocking layers, and the ability to adjust the amount of implant damage through the use of implant dose (see Fig. 1.8).

Fig. 1.3 A schematic of a modern ion implanter

Fig. 1.4 Periodic table showing a partial list of beam line implant species regularly available for CMOS processing. The darker shaded atoms comprise a historical list of the silicon dopant species and the lighter shaded atoms reflect those which are commonly used for material modification purposes. This list continues to expand

Ion = Silicon [14], mass = 27.977 amu

Target density = 2.3212E+00 g/cm^3 = 4.9770E+22 atoms/cm^3

======= Target composition =========

Atom name	Atom numb	Atomic percent	Mass percent
Si	14	100.00	100.00

====================================

Bragg correction = 0.00%
Stopping units = MeV / (mg/cm^2)
See bottom of table for other stopping units

Ion energy	d*E*/d*x* elec.	d*E*/d*x* nuclear	Projected range	Longitudinal straggling	Lateral straggling
10.00 keV	4.592E−01	1.687E+00	174 A	87 A	63 A
11.00 keV	4.816E−01	1.695E+00	188 A	93 A	68 A
12.00 keV	5.031E−01	1.701E+00	201 A	99 A	72 A
13.00 keV	5.236E−01	1.704E+00	215 A	105 A	76 A
14.00 keV	5.434E−01	1.706E+00	229 A	110 A	80 A
15.00 keV	5.624E−01	1.705E+00	242 A	116 A	84 A
16.00 keV	5.809E−01	1.704E+00	256 A	121 A	88 A
17.00 keV	5.988E−01	1.702E+00	269 A	127 A	92 A
18.00 keV	6.161E−01	1.699E+00	283 A	132 A	96 A
20.00 keV	6.494E−01	1.690E+00	310 A	143 A	103 A

Fig. 1.5 SRIM simulation of stopping components for a silicon implant into a silicon substrate

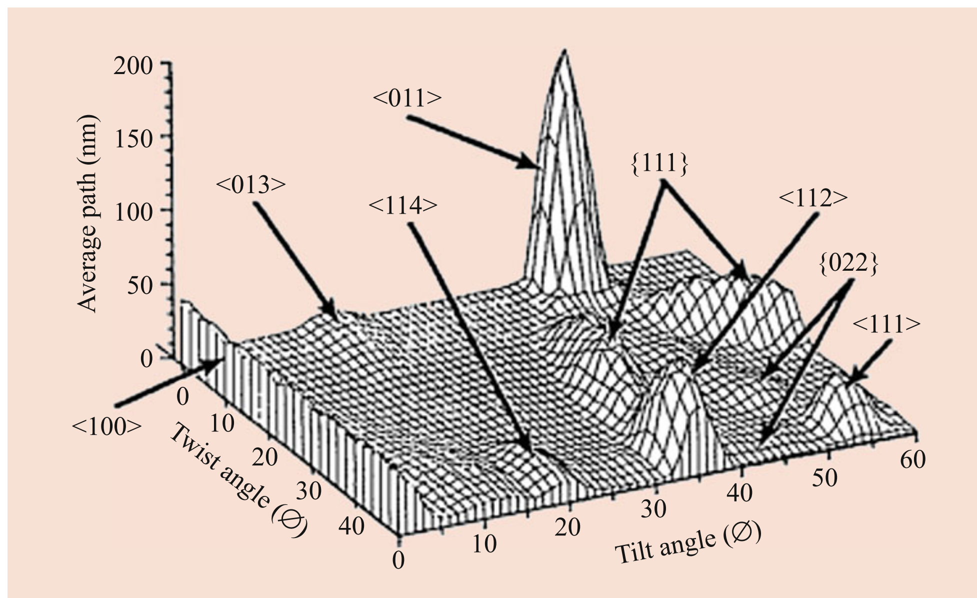

Fig. 1.6 Monte Carlo simulation results of 5 keV B-11 ions implanted into (100) oriented silicon as a function of tilt and twist of the wafer. Regions of this plot reflecting a low average path indicate implant into a randomized crystal orientation, while those which experience longer implant average path lengths reflect crystal orientations which present a highly ordered atomic cross section to the ion implant beam

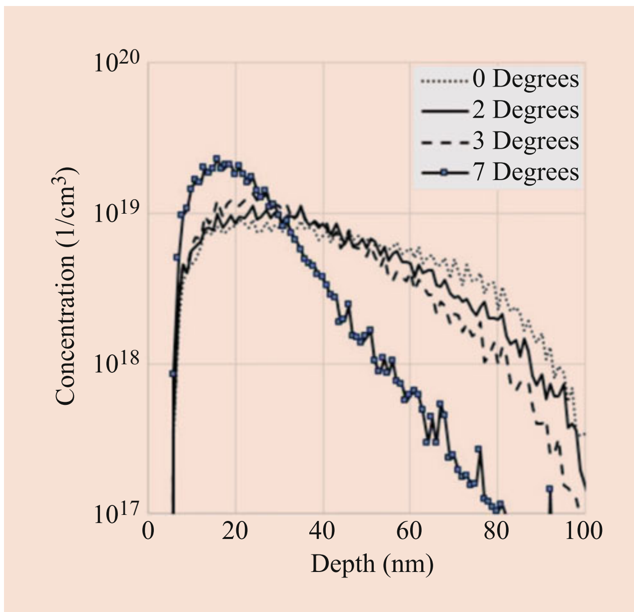

Fig. 1.7 Monte Carlo simulation of 3 keV boron implant at 5e13/cm^2 dose implanted into a (100) orientated silicon wafer. A slight variation in tilt angle toward (110) results in a substantial reduction in channeling tail of the implant

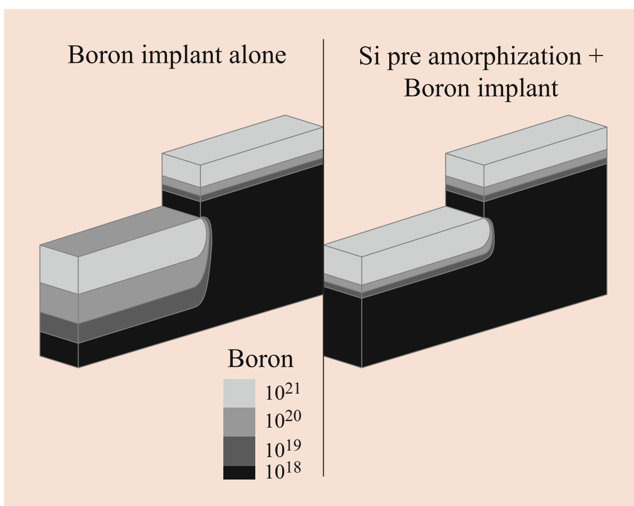

Fig. 1.8 Simulation showing the impact of a pre-amorphizing implant upon a subsequent non-amorphizing boron implant. In both cases, the boron implant is identical. In addition to a much more abrupt vertical implant profile, the lateral profile is also several nm more abrupt for the process which includes a pre-amorphizing implant

Amorphization may be accomplished by the same implants which are used to induce doping. This process is referred to as self-amorphization. For a group IV semiconductor crystal such as Si or Ge, self-amorphization commonly occurs with higher mass implanted species such as In, Sb, As, or P. Self-amorphization with lighter atoms such as B may be achieved through the use of cluster species such as BF2. In a region which is self-amorphized, the damaged location and ion positioning will largely overlap. It is common in a self-amorphized material to see a strong dependence between the implanted dose and measured projected range of the implant with the lightest dose self-amorphizing implants experiencing a longer projected range due to channeling which occurs before the self-amorphization process is completed.

Amorphization may also be accomplished through the use of a separate non-doping or co-implant specie. For a group IV semiconductor, amorphization without introducing doping is commonly achieved through the use of an implant specie from group IV such as Si, Ge, or Sn or through the use of an implant of a noble gas specie such as Ar, Kr, or Xe or through the use of species such as F or cluster implant species which do not contain a dopant atom. In a separately amorphized or pre-amorphized region, the damage and ion profiles need not overlap.

In addition to amorphization, another means of minimizing channeling is through the use of an amorphous capping layer placed above a crystalline semiconductor region. In this case, the amorphous capping layer serves to randomize the ion trajectories before they reach the semiconductor.

Amorphization and implant damage are important effects in that they significantly impact the channeled tail of an implanted ion distribution. This can manifest as a shallower vertical or more abrupt lateral junction. For this reason, CMOS processes which involve tip extension implants, source/drain implants, or source/drain contact implants may involve an implant of a non-doping specie performed prior to the implant of a doping specie. This implant may or may not be (separately) amorphizing and serves to confine the implanted doping laterally which may lead to improved device short channel effects, reduced device V_t, and higher channel mobility.

1.3.4 Impact of Implant Process Knobs upon Resultant Distributions of Implanted Ions and Implant Damage

The electrical behavior and characteristics of a transistor are heavily impacted by the placement and concentration of dopant atoms. Integration and optimization of a transistor fabrication process requires a thorough understanding of the positioning of both damage and ion, as well as an understanding of how processes downstream from the implant operation are impacted by the results of a prior implant operation. Such understanding is normally gained through the use of TCAD tools and the models upon which these tools are based. The principal outputs of these simulations are the ion profile and the crystal damage profile. These quantities may then be utilized in TCAD models to create profiles of excess damage which may drive dopant diffusion, grow and nucleate extended defects such as {311}'s and end-of-range

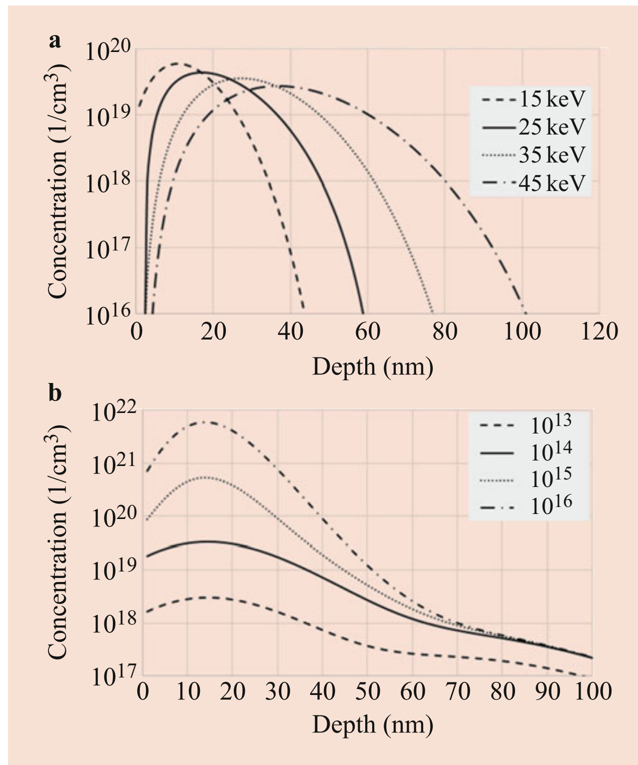

Fig. 1.9 (**a**) Simulation of arsenic implant at 15/25/35/45 keV at fixed 1e14/cm^2 dose into a randomized (100) Si crystal. As energy of the implant is increased, the resultant profile is deeper and broader. (**b**) simulation of 10 keV phosphorus implant into an undamaged (100) Si crystal. As the dose is increased, the fraction of channeled ions is decreased which results in a profile shape change

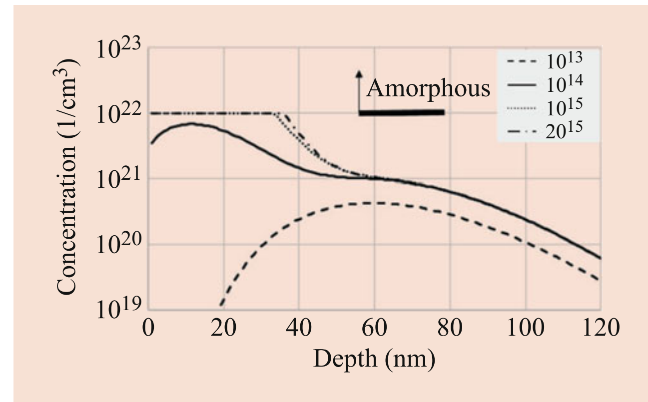

Fig. 1.10 Simulated cascade damage resultant from a 10 keV phosphorus implant into (100) Si at doses of 1e13 to 2e15/cm^2. The 1e15 and 2e15/cm^2 implants will result in an amorphous layer being formed in the structure. As implant dose is increased, the peak cascade damage also increases until amorphization is reached. Increasing dose further will lead to an increase in the depth of amorphization

(EOR) loops, lead to dopant deactivation or clustering, and initiate recrystallization of an amorphized layer. Therefore, it is critical to understand the impact of implant parameters upon these quantities.

The two most fundamental implant parameters are dosage/dose and implant energy. The implant dose is commonly measured in units of 1/cm^2 and represents the number of ions which are implanted per unit area as measured perpendicular to the ion beam. The measurement of implant dose perpendicular to the ion beam results in an effective dose reduction at wafer surface for an implant in which the wafer is tilted at time of implant and not orientated perpendicular to the ion beam.

Implant profiles for arsenic and phosphorus are shown in Fig. 1.9. As energy of the implant is increased, the resultant profile is deeper and broader. As the dose is increased, the fraction of channeled ions is decreased which results in a profile shape change. Both of these effects can be modeled with either Monte Carlo implant simulations or with continuum models which utilize shape functions (as shown in these figures).

The implant damage can also be modeled with TCAD tools, as demonstrated in Fig. 1.10. As would be expected, increasing the implant dose will lead to an increase in implant damage until amorphization is reached. In many TCAD implant models, amorphization is represented as a threshold function in which a region is amorphized if the damage exceeds a value. This damage is a measure of the quantity of vacancies which have been introduced to the crystal lattice due to collisions and recoil events and the interstitials which are created as the recoiled atoms come to rest. Computationally efficient models such as those of Hobler have been proposed to describe these effects and are commonly used in TCAD tools to describe implant damage. A measure of the vacancies injected from an implanted ion can also be determined through a Monte Carlo implant simulator such as MARLOWE or SRIM.

Until recently, most ion implants used in CMOS processes were performed at room temperature. Modern implant tools, however, now have the ability to perform the implant into either a heated or cooled substrate. An implant into a heated substrate will tend to dynamically heal implant damage during the implant, and heated implants have found applications for situations where amorphization must be avoided such as high-dose well implants for a bulk FinFET process. Conversely, cryogenic (or chilled) implants have found applications where abrupt amorphizations are desired such as for pre-amorphization implants done at contact formation.

For high-volume manufacturing, it is common to operate the implanter at the highest reasonable beam current (and hence the lowest time on the tool to achieve the desired dose); however, ion implanters can operate at different beam current levels, and this is a knob which is also used for process optimization at times. It has been shown experimentally that