Real-Time Electromagnetic Transient Simulation of AC-DC Networks

Venkata Dinavahi, Ning Lin

IEEE PRESS

IEEE PRESS SERIES ON POWER ENGINEERING

Mohamed E. El-Hawary, *Series Editor*

WILEY

Real-Time Electromagnetic Transient Simulation of AC–DC Networks

IEEE Press
445 Hoes Lane
Piscataway, NJ 08854

IEEE Press Editorial Board
Ekram Hossain, *Editor in Chief*

Jón Atli Benediktsson
Anjan Bose
David Alan Grier
Elya B. Joffe
Xiaoou Li
Lian Yong
Andreas Molisch
Saeid Nahavandi
Jeffrey Reed
Diomidis Spinellis
Sarah Spurgeon
Ahmet Murat Tekalp

Real-Time Electromagnetic Transient Simulation of AC–DC Networks

Venkata Dinavahi
Ning Lin

IEEE PRESS SERIES ON POWER ENGINEERING

IEEE PRESS
WILEY

Copyright © 2021 by The Institute of Electrical and Electronics Engineers, Inc. All rights reserved.

Published by John Wiley & Sons, Inc., Hoboken, New Jersey.
Published simultaneously in Canada.

No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, recording, scanning, or otherwise, except as permitted under Section 107 or 108 of the 1976 United States Copyright Act, without either the prior written permission of the Publisher, or authorization through payment of the appropriate per-copy fee to the Copyright Clearance Center, Inc., 222 Rosewood Drive, Danvers, MA 01923, (978) 750-8400, fax (978) 750-4470, or on the web at www.copyright.com. Requests to the Publisher for permission should be addressed to the Permissions Department, John Wiley & Sons, Inc., 111 River Street, Hoboken, NJ 07030, (201) 748-6011, fax (201) 748-6008, or online at http://www.wiley.com/go/permission.

Limit of Liability/Disclaimer of Warranty
While the publisher and author have used their best efforts in preparing this book, they make no representations or warranties with respect to the accuracy or completeness of the contents of this book and specifically disclaim any implied warranties of merchantability or fitness for a particular purpose. No warranty may be created or extended by sales representatives or written sales materials. The advice and strategies contained herein may not be suitable for your situation. You should consult with a professional where appropriate. Neither the publisher nor author shall be liable for any loss of profit or any other commercial damages, including but not limited to special, incidental, consequential, or other damages.

For general information on our other products and services or for technical support, please contact our Customer Care Department within the United States at (800) 762-2974, outside the United States at (317) 572-3993 or fax (317) 572-4002.
Wiley also publishes its books in a variety of electronic formats. Some content that appears in print may not be available in electronic formats. For more information about Wiley products, visit our web site at www.wiley.com.

Library of Congress Cataloging-in-Publication Data

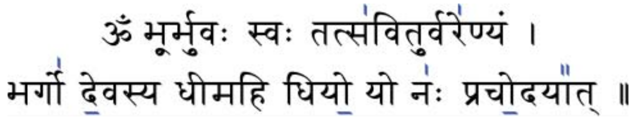
ISBN: 9781119695448

Cover design by Wiley
Cover image: © Audrius J/Shutterstock

Set in 9.5/12.5pt STIXTwoText by Straive, Chennai, India

10 9 8 7 6 5 4 3 2 1

Ṛgvéda 3.62.10:



ॐ भूर्भुवः स्वः तत्स॑वितु॒र्वरे॑ण्यं ।
भर्गो॑ दे॒वस्य धीमहि धियो॒ यो न॑ः प्रचो॒दया᳚त् ॥

Om bhūrbhuvaḥ svaḥ tatsa̍viturvare̍ṇyaṃ;
bhargo̍ de̱vasya dhīmahi dhiyo̱ yo na̍ḥ praco̱dayā̎t.

We meditate on that most adored Supreme Soul, the Creator, whose effulgence illumines all realms. May this divine light illumine our intellect.

Dedicated to our parents:
Late Smt. Dinavahi Sasirekha and Shri. Dinavahi Ramarao
Liyue Xie and Quanyao Lin

Contents

About the Authors *xix*
Preface *xxi*
Acknowledgments *xxv*
List of Acronyms *xxvii*

1 Field Programmable Gate Arrays *1*
1.1 Overview *1*
1.1.1 FPGA Hardware Architecture *2*
1.1.2 Configurable Logic Block *3*
1.1.3 Block RAM *4*
1.1.4 Digital Signal Processing Slice *4*
1.2 Multiprocessing System-on-Chip Architecture *6*
1.3 Communication *7*
1.4 HIL Emulation *9*
1.4.1 Vivado® High-Level Synthesis Tool *9*
1.4.2 Vivado® Top-Level Design *11*
1.4.3 Number Representation and Operations *13*
1.4.4 FPGA Design Schemes *14*
1.4.4.1 Pipeline Design Architecture *14*
1.4.4.2 Parallel Design Architecture *14*
1.4.5 FPGA Experiment *15*
1.5 Summary *16*

2 Hardware Emulation Building Blocks for Power System Components *17*
2.1 Overview *17*
2.2 Concept of HEBB *18*
2.3 Numerical Integration *18*
2.4 Linear Lumped Passive Elements *20*

2.4.1 Model Formulation *20*
2.4.1.1 Resistance *R* *20*
2.4.1.2 Inductance *L* *20*
2.4.1.3 Capacitance *C* *22*
2.4.1.4 *RL* Branch *23*
2.4.1.5 *LC* Branch *23*
2.4.1.6 *RLCG* Branch *24*
2.4.2 Hardware Emulation of Linear Lumped Passive Elements *26*
2.5 Sources *27*
2.5.1 Hardware Emulation of Sources *28*
2.6 Switches *30*
2.6.1 Hardware Emulation of Switches *30*
2.7 Transmission Lines *32*
2.7.1 Traveling Waves *32*
2.7.2 Traveling Wave Model *35*
2.7.2.1 Modal Transformation *36*
2.7.3 Hardware Emulation of the TWM *39*
2.7.3.1 *Transformation Unit* *39*
2.7.3.2 *Update Unit* *39*
2.7.4 Frequency Dependent Line Model *41*
2.7.5 Hardware Emulation of FDLM *46*
2.7.5.1 *Convolution* Unit *46*
2.7.5.2 *Update* Unit *47*
2.7.6 Universal Line Model *48*
2.7.6.1 Frequency-Domain Formulation *48*
2.7.6.2 Time-Domain Formulation *49*
2.7.7 Hardware Emulation of the ULM *51*
2.7.7.1 *Update* $\boldsymbol{x}$ Unit *52*
2.7.7.2 *Convolution* Unit *52*
2.7.7.3 *Interpolation* Unit *54*
2.8 Network Solver *54*
2.8.1 Hardware Emulation of Network Solver *55*
2.8.2 Paralleled EMT Solution Algorithm *55*
2.8.3 *MainControl* Module *58*
2.8.4 Real-Time Emulation Case Study *59*
2.9 Nonlinear Elements: Iterative Real-Time EMT Solver *63*
2.9.1 Compensation Method *64*
2.9.2 Newton–Raphson Method *65*
2.9.3 Hardware Emulation of Nonlinear Solver *67*
2.9.3.1 Nonlinear Function Evaluation *68*
2.9.3.2 Parallel Calculation of $\boldsymbol{J}$ and $F(i_{km})$ *68*

2.9.3.3 Parallel Gauss–Jordan Elimination *71*
2.9.3.4 Computing v_c *71*
2.9.4 Case Studies *71*
2.10 Summary *77*

3 Power Transformers *79*

3.1 Overview *79*
3.2 Nonlinear Admittance-Based Real-Time Transformer Model *80*
3.2.1 Linear Model Formulation *80*
3.2.2 Linear Module Hardware Design *82*
3.2.3 Inode Unit Module *84*
3.2.4 Nonlinear Model Solution *85*
3.2.4.1 Preisach Hysteresis Model *88*
3.2.4.2 Nonlinear Module Hardware Design *89*
3.2.5 Frequency-Dependent Eddy Current Model *90*
3.2.6 Hardware Emulation of Power Transformer *91*
3.2.7 Real-Time Emulation Case Studies *94*
3.2.7.1 Case I *94*
3.2.7.2 Case II *99*
3.3 Nonlinear Magnetic Equivalent Circuit Based Real-time Multi-Winding Transformer Model *100*
3.3.1 Topological ST EMT Model *102*
3.3.1.1 ST Operating Principle *102*
3.3.1.2 Tap-selection Algorithm *102*
3.3.1.3 High-Fidelity Nonlinear MEC-Based ST Model *102*
3.3.1.4 Iron Core Hysteresis and Eddy Currents *107*
3.3.2 High-Fidelity Nonlinear MEC-Based ST Hardware Emulation *109*
3.3.2.1 Network Transient Emulation with Embedded ST *109*
3.3.3 Real-Time Emulation Case Studies *112*
3.3.3.1 Finite Element Modeling and Validation *112*
3.3.3.2 Case Studies *112*
3.4 Real-Time Finite-Element Model of Power Transformer *123*
3.4.1 Magnetodynamic Problem Formulation *123*
3.4.1.1 Refined TLM Solution *126*
3.4.1.2 Field-Circuit Coupling *130*
3.4.2 Hardware Emulation of Finite Element Model *132*
3.4.3 Case Studies *136*
3.4.3.1 Results and Validation *137*
3.4.3.2 Speed-up and Scalability *140*
3.5 Summary *141*

4 Rotating Machines *143*
4.1 Overview *143*
4.2 Lumped Universal Machine (UM) Model *144*
4.2.1 UM Model Formulation *144*
4.2.2 Interfacing UM Model with Network *146*
4.2.3 UM HEBB *148*
4.2.3.1 *Speed & Angle* Unit *149*
4.2.3.2 *FrmTran* Unit *150*
4.2.3.3 $Compi_{dq0}$ Unit *151*
4.2.3.4 *Flux & Torque* Unit *151*
4.2.3.5 *Update & CompVc* Unit *151*
4.2.4 Real-Time Emulation Case Study *152*
4.2.5 Overall Power System HEBB for Real-Time EMT Emulation *154*
4.3 General Framework for State-Space Electrical Machine Emulation *158*
4.3.1 FPGA Design Approaches for Electrical Machine Emulation *159*
4.3.2 State-Space Representation of Machine Models *160*
4.3.3 System Configuration on FPGA *161*
4.3.3.1 Number Representation *161*
4.3.3.2 Floating-Point Implementation by VHDL *162*
4.3.3.3 Fixed-Point Implementation by Schematic *167*
4.3.4 Evaluation of Designed Architectures *170*
4.3.4.1 Real-Time Emulation Accuracy Assessment *170*
4.3.4.2 Off-line Validation *171*
4.3.4.3 Hardware Resource Utilization *172*
4.3.5 Real-Time Emulation Case Studies *174*
4.3.5.1 Case I: Induction Motor Transients *174*
4.3.5.2 Case II: Synchronous Generator Transients *174*
4.3.5.3 Case III: Line Start-Permanent Magnet Synchronous Motor Transients *176*
4.3.5.4 Case IV: DC Motor Transients *177*
4.4 Nonlinear Magnetic Equivalent Circuit Based Induction Machine Model *178*
4.4.1 Magnetic Circuit *179*
4.4.2 Interfacing of Magnetic and Electric Circuits *181*
4.4.3 Electric Circuit *182*
4.4.4 Nonlinear Solution of Detailed MEC *182*
4.4.5 Hardware Emulation of Nonlinear MEC *183*
4.4.5.1 Parallel Gauss–Jordan Elimination Unit *185*
4.4.5.2 Parallel Computational Unit for Residual Vector *187*
4.4.5.3 Nonlinear Evaluation Unit *187*

4.4.6 Evaluation of Real-Time Emulation of Induction Machine *187*
4.5 Summary *190*

5 Protective Relays *193*
5.1 Overview *193*
5.2 Hardware Emulation of Multifunction Protection System *195*
5.2.1 Signal Processing HEBB *196*
5.2.1.1 CORDIC HEBB *196*
5.2.1.2 Symmetrical Components HEBB *198*
5.2.1.3 DFT HEBB *198*
5.2.1.4 Zero-Crossing Detection HEBB *199*
5.2.2 Multifunction Protective System HEBB *203*
5.2.2.1 Fault Detection HEBB *203*
5.2.2.2 Directional Overcurrent Protection HEBB *205*
5.2.2.3 Over/Under Voltage Protection HEBB *205*
5.2.2.4 Distance Protection HEBB *205*
5.2.2.5 Under/Over Frequency Protection HEBB *209*
5.3 Test Setup and Real-Time Results *209*
5.3.1 Case I *210*
5.3.2 Case II *213*
5.4 Summary *214*

6 Adaptive Time-Stepping Based Real-Time EMT Emulation *217*
6.1 Overview *217*
6.2 Nonlinear Solution and Adaptive Time-Stepping Schemes *219*
6.2.1 Nonlinear Element Solution Methods *219*
6.2.1.1 Newton–Raphson Method *219*
6.2.1.2 Piecewise Linearization (PWL) Method *219*
6.2.1.3 Piecewise N-R Method *220*
6.2.2 Adaptive Time-Stepping Schemes *220*
6.2.2.1 Local Truncation Error Method *220*
6.2.2.2 Iteration Count Method *221*
6.2.2.3 DVDT or DIDT Method *221*
6.2.3 Combinations of Adaptive Time-Stepping Schemes *222*
6.2.3.1 Measurements and Restrictions for Real-Time Emulation *222*
6.2.4 Case Studies *223*
6.2.4.1 Diode Full-Bridge Circuit *224*
6.2.4.2 Power Transmission System *225*
6.2.4.3 FPGA Implementation *229*
6.2.4.4 Real-Time Emulation Results *234*

6.3 Adaptive Time-Stepping Universal Line Model and Universal Machine Model for Real-Time Hardware Emulation *236*
6.3.1 Subsystem-Based Adaptive Time-Stepping Scheme *237*
6.3.2 Adaptive Time-Stepping ULM and UM Models *238*
6.3.2.1 ULM Computation *238*
6.3.2.2 Universal Machine Model Computation *242*
6.3.3 Real-Time Emulation Case Study *243*
6.3.3.1 Hardware Implementation *243*
6.3.3.2 Latency and Hardware Resource Utilization *246*
6.3.4 Results and Validation *247*
6.3.4.1 Validation of the ULM Model *247*
6.3.4.2 Real-Time Emulation Results *248*
6.4 Summary *252*

7 Power Electronic Switches *253*
7.1 Overview *253*
7.2 IGBT/Diode Nonlinear Behavioral Model *255*
7.2.1 Power Diode *256*
7.2.1.1 Mathematical Model *256*
7.2.1.2 Hardware Module Architecture *257*
7.2.2 IGBT *259*
7.2.2.1 Model Formulation *259*
7.2.2.2 Hardware Module Architecture *263*
7.2.2.3 Multiple Parallel Devices *265*
7.2.3 Electro-Thermal Network *267*
7.2.4 Hardware Emulation Results *268*
7.3 Physics-Based Nonlinear IGBT/Diode Model *270*
7.3.1 Physics-Based Nonlinear p–i–n Diode Model *271*
7.3.1.1 Model Formulation *271*
7.3.1.2 Model Discretization and Linearization *272*
7.3.1.3 Hardware Emulation on FPGA *274*
7.3.2 Physics-Based Nonlinear IGBT Model *276*
7.3.2.1 Model Formulation *276*
7.3.2.2 Model Discretization and Linearization *279*
7.3.2.3 Hardware Emulation on FPGA *281*
7.3.3 Hardware Emulation Results *285*
7.3.3.1 Test circuit *285*
7.3.3.2 Results and comparison *286*
7.4 IGBT/Diode Curve-Fitting Model *292*
7.4.1 Linear Static Curve-fitting Model *293*
7.4.1.1 Static Characteristics *293*

7.4.1.2 Switching Transients *293*
7.4.2 Nonlinear Dynamic Curve-fitting Model *296*
7.4.3 Hardware Emulation Results *298*
7.5 Summary *300*

8 AC–DC Converters *301*
8.1 Overview *301*
8.2 Detailed Model *303*
8.2.1 Detailed Equivalent Circuit Model *304*
8.3 Equivalenced Device-Level Model *305*
8.3.1 Power Loss Calculation *307*
8.3.2 Thermal Network Calculation *309*
8.3.3 Hardware Emulation of SM Model on FPGA *311*
8.3.4 MMC System Hardware Emulation *314*
8.3.5 Real-Time Emulation Results *316*
8.3.5.1 Test Circuit and Hardware Resource Utilization *316*
8.3.5.2 Results and Comparison for Single-Phase Five-Level MMC *318*
8.3.5.3 Results for Three-Phase Nine-Level MMC *324*
8.4 Virtual-Line-Partitioned Device-Level Models *324*
8.4.1 TLM-Link Partitioning *326*
8.4.2 Hardware Design on FPGA *328*
8.4.2.1 Hardware Platform *329*
8.4.2.2 Controller Emulation *329*
8.4.2.3 MMC Emulation on FPGA *330*
8.4.3 Real-Time Emulation Results *335*
8.4.3.1 MMC *335*
8.4.3.2 Induction Machine Driven by Five-Level MMC *342*
8.5 MMC Partitioned by Coupled Voltage–Current Sources *344*
8.5.1 V–I Coupling *344*
8.5.2 Hardware Emulation Case of NBM-Based MMC *346*
8.5.2.1 Power Converter HIL Emulation *346*
8.5.2.2 HIL Emulation Results and Validation *347*
8.5.2.3 Islanded MMC Performance *348*
8.5.2.4 MMC–MVDC Performance *355*
8.6 Clamped Double Submodule MMC *355*
8.6.1 Operation Principles of CDSM *357*
8.6.2 Device-Level Modeling Scheme *359*
8.6.2.1 Temperature-Dependent Electrical Interface Parameter Calculation *359*
8.6.2.2 Device-Level Linearized Transient Waveform Calculation *361*
8.6.3 SM-Level Modeling Scheme *362*

8.6.4 Converter-Level Modeling Scheme *362*
8.6.5 Case Study and Hardware Implementation *363*
8.6.5.1 Design Partition *365*
8.6.5.2 Latency and Resource Consumption *367*
8.6.6 Real-Time Emulation Results and Analysis *368*
8.6.6.1 Steady-State Results *368*
8.6.6.2 DC Power Flow Control *368*
8.6.6.3 DC Fault Transient Results *371*
8.7 Summary *374*

9 DC-DC Converters *377*
9.1 Overview *377*
9.2 Buck–Boost Converter *379*
9.2.1 System-Level Modeling *379*
9.2.2 Hardware Implementation *380*
9.3 Solid-State Transformer Modeling *381*
9.3.1 MMC Arm Models *382*
9.3.1.1 TLM-Stub Model (TLM-S) *382*
9.3.1.2 Nonlinear Switch-Based Model (NSM) *383*
9.3.1.3 Hybrid Arm Model *384*
9.3.2 Three-Phase Saturable Transformer Model *385*
9.3.3 SST EMT Model *385*
9.3.4 SST HIL Emulation *386*
9.3.5 SST Real-Time HIL Emulation Results *390*
9.3.5.1 Device-Level Behavior *390*
9.3.5.2 Converter Performance *391*
9.3.5.3 System Tests *392*
9.4 Summary *394*

10 DC Circuit Breakers *397*
10.1 Overview *397*
10.2 HHB in MTDC System *399*
10.2.1 MTDC Test System Schematic *399*
10.2.2 DC Line Protection *401*
10.2.2.1 Voltage Derivative Protection *401*
10.2.2.2 Over Current Protection *401*
10.3 Proactive Hybrid HVDC Breaker *402*
10.3.1 HHB EMT Model *403*
10.3.2 Varistor Model *404*
10.3.3 General HHB Unit Model *406*
10.3.4 Two-Node IGBT Models *407*

10.3.5 IGBT Low-Order Nonlinear Behavioral Model *409*
10.3.5.1 IGBT Fourth-Order Behavioral Model *409*
10.3.5.2 Parameters Extraction *409*
10.3.5.3 Sensitivity Analysis *410*
10.3.5.4 Model Parallelization *411*
10.3.6 Electro-Thermal Network *412*
10.3.7 HHB Hardware Implementation on FPGA *412*
10.3.8 HHB HIL Emulation Results *416*
10.3.8.1 Device-Level Performance *416*
10.3.8.2 System-Level Performance *424*
10.4 Ultrafast Mechatronic Circuit Breaker *426*
10.4.1 Nonlinear Device-Level Thyristor Model *426*
10.4.1.1 Basic Device Characteristics *426*
10.4.1.2 Scalable Cascaded Thyristor Model *428*
10.4.2 UFMCB Modeling *431*
10.4.3 Relaxed Scalar Newton–Raphson (RSNR) *433*
10.4.4 UFMCB Hardware Design *435*
10.4.5 UFMCB Real-Time Tests and Validation *438*
10.4.5.1 Four-Terminal DC Grid Test Case *438*
10.4.5.2 UFMCB Design Evaluation by HIL System *438*
10.4.5.3 UFMCB in HVDC Grid *442*
10.5 Summary *444*

11 Large-Scale AC and DC Networks *447*
11.1 Overview *447*
11.2 Spatial Decomposition and Parallelism *449*
11.2.1 Functional Decomposition for Large-Scale Real-Time Emulation *449*
11.2.2 Hardware Module Parallelism *451*
11.3 Multi-FPGA Hardware Design for Real-Time EMT Emulation *453*
11.3.1 Case I: 3-FPGA Hardware Design *454*
11.3.2 Case II: 10-FPGA Hardware Design *457*
11.3.3 Performance and Scalability of the Real-Time EMT Emulator *460*
11.4 CIGRÉ DC Grid Hybrid Modeling Methodology *465*
11.4.1 Network Topology *467*
11.4.2 Control Scheme *467*
11.4.3 Hybrid Modeling Methodology *468*
11.4.3.1 Device-Level Electrothermal Model *469*
11.4.3.2 Equivalent Circuit Model *469*
11.4.3.3 Average Value Model *471*
11.4.3.4 Transmission Line Model *471*
11.4.4 Real-Time MPSoC-FPGA Based DC Grid Emulator *471*

11.4.4.1 System Decomposition *471*
11.4.4.2 Hardware Resource Allocation and Task Partitioning *472*
11.4.4.3 Design and Implementation *474*
11.4.5 Real-Time Emulation Results and Validation *475*
11.4.5.1 Steady-State Operation *475*
11.4.5.2 Power Flow Command Change *477*
11.4.5.3 DC Fault *477*
11.5 Real-Time Co-Emulation Framework for Cyber-Physical Systems *479*
11.5.1 Communication Network Simulation and Co-Simulation *481*
11.5.2 Real-Time Co-Emulation Framework *484*
11.5.2.1 RTCE Hardware Architecture *484*
11.5.3 Hardware Implementation of RTCE *487*
11.5.3.1 Multi-Board EMT Emulation *488*
11.5.3.2 Communication Protocol and Implementation *489*
11.5.4 Real-Time Emulation Results and Verification *491*
11.5.4.1 Processing Delay and Hardware Resource Cost *491*
11.5.4.2 Case Study 1: Over-Current Fault *492*
11.5.4.3 Case Study 2: Communication Link Failure *493*
11.6 Faster-Than-Real-Time Hybrid Dynamic-EMT Emulation of AC–DC Grids *495*
11.6.1 Flexible Time-Stepping Algorithm for Dynamic Emulation *496*
11.6.1.1 Transient Stability Emulation Methodology *496*
11.6.1.2 Local Equipment Based Flexible Time-stepping *497*
11.6.2 AC–DC Grid Component Modeling *498*
11.6.2.1 AC–DC Grid Interface *498*
11.6.2.2 AC Grid Modeling *499*
11.6.2.3 DC Grid Modeling *501*
11.6.3 FTRT Emulation on FPGAs *503*
11.6.4 FTRT Emulation Results and Validation *505*
11.6.4.1 Three-Phase-to-Ground Fault *506*
11.6.4.2 Generator Outage and Sudden Load Change *507*
11.7 Summary *510*

Bibliography *513*

Appendix A Parameters for Case Studies *531*
A.1 Chapter 2 *531*
A.1.1 Case in Section 2.7 *531*
A.1.2 Cases in Section 2.8 *531*
A.2 Chapter 3 *531*
A.2.1 Cases in Section 3.2 *531*

A.2.1.1 Cases Study I *531*
A.2.1.2 Cases Study II *532*
A.2.2 Cases in Section 3.3 *532*
A.2.2.1 Transformer *532*
A.2.2.2 System *532*
A.2.3 Cases in Section 3.4 *532*
A.3 Chapter 4 *533*
A.3.1 UM Case in Section 4.2 *533*
A.3.2 Cases in Section 4.3 *534*
A.3.2.1 State-Space Matrices of Rotating Machines *534*
A.3.2.2 Parameters of Rotating Machines *538*
A.3.3 MEC Case in Section 4.4 *538*
A.4 Chapter 5 *538*
A.5 Chapter 6 *539*
A.5.1 Cases in Section 6.2 *539*
A.5.2 Cases in Section 6.3 *540*
A.6 Chapter 7 *540*
A.7 Chapter 8 *541*
A.7.1 Equivalenced Device-Level Model in Section 8.3 *541*
A.7.2 MMC-IM Case in Section 8.4 *541*
A.7.3 MVDC Case in Section 8.5 *541*
A.7.4 MTDC Case in Section 8.6 *541*
A.8 Chapter 9 *541*
A.9 Chapter 10 *542*
A.9.1 HHB Case *542*
A.9.2 UFMCB Case *542*
A.10 Chapter 11 *543*
A.10.1 CIGRÉ B4 DC Grid Test System *543*

Index *545*

About the Authors

Venkata Dinavahi received the B.Eng. degree in Electrical Engineering from the Visveswaraya National Institute of Technology (VNIT), Nagpur, India, in 1993, the M.Tech. degree in Electrical Engineering from the Indian Institute of Technology (IIT), Kanpur, India, in 1996, and the Ph.D. degree in Electrical and Computer Engineering from the University of Toronto, Ontario, Canada, in 2000. Currently he is a Professor with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, Alberta, Canada. His research interests include real-time simulation of power systems and power electronic systems, electromagnetic transients, device-level modeling, large-scale systems, and parallel and distributed computing. He was the founding chair of the IEEE Power and Energy Society (PES) Task Force on Interfacing Techniques for Simulation Tools from 2006 to 2014. He actively participates in several IEEE PES committees notably in the Working Group on Modeling and Analysis of System Transients. He has published over 150 papers in peer-reviewed international journals and over 60 articles in international conference proceedings. He is a Fellow of IEEE. He was the recipient of the 2018 Outstanding Engineer Award from the IEEE PES/IAS Northern Canada Chapter. He is a member of CIGRÉ (International Council on Large Electric Systems) and a Professional Engineer in the Province of Alberta.

Ning Lin received the B.Sc. and M.Sc. degrees in Electrical Engineering from Zhejiang University, China, in 2008 and 2011, respectively, and the Ph.D. degree in Electrical and Computer Engineering from the University of Alberta, Canada, in 2018. From 2011 to 2014, he worked as an engineer on power system automation, flexible AC transmission system (FACTS), and high-voltage direct current (HVDC). Currently, he is a postdoc assistant researcher at the University of Alberta. His research interests include power electronics, real-time simulation of power systems, and high-performance computing of integrated AC/DC grids.

Preface

Promising advances in high-power electronics and the challenges facing modern power system operation in terms of integration of large-scale renewable generation and energy storage is necessitating the construction of high-voltage direct current (HVDC) transmission worldwide. Meshed multi-terminal DC grids are transporting bulk energy over longer distances, interconnecting far-flung asynchronous AC network, and are being operated with higher redundancy, efficiency, and reliability. Since the conception of real-time analog simulators (known as transient network analyzers (TNAs)) and subsequently real-time digital power system simulators in the 1970s through to the 1990s, one of their principal applications has been for the testing of control and protection functions in a hardware-in-the-loop (HIL) configuration for HVDC systems prior to their commissioning. Currently, real-time digital electromagnetic transient (EMT) simulators are used in every sector of electrical power chain: generation, transmission, distribution, and consumption. Moreover, real-time EMT simulators are also frequently employed in the transportation (automotive and railway traction), aviation, and marine industries, wherein the electrical systems share many structural and functional commonalities with terrestrial AC–DC networks. While the design, testing, and commissioning of local control and protection functions of system equipment is the primary objective of real-time EMT simulation, it is also paramount for global dynamic and interactive studies of large-scale power systems for wide-area control, protection, and system operator training. EMT simulation of large AC–DC grids in real time is a significant challenge due to the need for detailed device-level modeling of system components while simultaneously reproducing the system-level interactions accurately by accommodating large system sizes. These contrasting requirements place an enormous burden on the simulator latency constraints and the hardware selection for implementing the real-time simulation.

EMTs are the consequence of the interplay between the electric and magnetic fields in power system equipment when the system is perturbed from its steady-state operation by an event such as the switching of a line, a fault, or a lightning strike. A widely accepted classification of EMT is into four categories: low-frequency oscillations (0.1 Hz–3 kHz) e.g. temporary overvoltages, slow-front surges (50 Hz–20 kHz) e.g. switching overvoltages, fast-front surges (10 kHz–3 MHz) e.g. lightning overvotages, and very fast-front surges (100 kHz–50 MHz) e.g. circuit breaker restrike overvoltages. The switching on and off of power semiconductor devices such as insulated gate bipolar transistors (IGBTs) also generates transients albeit at the device-level, and they are typically in the 1–20 MHz range. The transients propagate near to the speed of light from their inception point and spread throughout the system causing extensive damage if not interrupted or absorbed. Of all the studies done in power systems, the modeling required to simulate EMT is the most complex. The higher the frequency of the transient, the more complex the modeling of any equipment becomes and the smaller the size of the network it spreads to. Conversely, low-frequency transients entail simpler modeling of equipment and propagate over a wider scale requiring the analysis of a larger network. For a particular EMT case study, the factors that influence the modeling complexity of any equipment are the distributed nature of parameters, frequency-dependency, and the inherent nonlinearities in the device. Accordingly, the extent to which each of these phenomena is accurately modeled for every equipment determines the computational burden experienced by the simulator. The selection of model decomposition strategy, numerical solution algorithm, and time-step also depends on these same factors. All of the above considerations need to be observed to successfully design and implement a real-time EMT simulation.

Of the many digital processors currently available on the market, field-programmable gate arrays (FPGAs) are the sole processor technology capable of meeting the rigorous real-time constraints and large hardware resource capacity required for AC–DC grid emulation with detailed equipment modeling. FPGAs contain numerous configurable logic resources, distributed memory, and inputs/outputs that can provide massive hardware parallelism for emulating detailed power system component models simultaneously. Currently available commercial FPGAs offer millions of logic gates, high-bandwidth on-chip memory, and ultrafast transceivers. The recent development of FPGA technology is not only in terms of improving their timing performance and enlarging their hardware resource capacity but also in terms of streamlining an integrated design tool ecosystem. The high-level synthesis (HLS) design methodology using C/C++ programming language instead of the conventional hardware description language (HDL) is explored as a new means of modularizing the AC–DC grid to reduce the hardware design cycle while maintaining a high synthesis efficiency. The synthesized hardware modules can then be pipelined efficiently with optimized performance regarding the resource usage and latency requirements.

This book intends to provide a detailed exposition of FPGA hardware based real-time EMT emulation for the fundamental components used in AC–DC power systems. Specific focus is afforded to detailed device-level models for their hardware realization in a massively parallel and deeply pipelined manner, and decomposition techniques for emulating large systems. In the various chapters of the book, while the hardware emulation may have been done on FPGAs from different generations or vendors, the underlying principles of model decomposition and parallel solution algorithms are generally applicable on any device. This book is intended for two groups of readers: graduate students in a university and professional research engineers and scientists in the industry. University students pursuing masters and doctoral degrees will find state-of-the-art presentation of the material on real-time EMT simulation of AC–DC grids. Such material can inspire and motivate advanced research ideas for their projects, dissertations, and publications. For industry experts, the book provides relevant academic research developments and implementation knowledge that they can incorporate in their respective product development process. The book is organized as follows: after giving a brief introduction of FPGA architecture and design flow in Chapter 1, Chapter 2 introduces the concepts of hardware emulation building blocks for fundamental power system components necessary for real-time EMT simulation: linear lumped passive elements, transmission lines, and nonlinear elements. Chapters 3 and 4 cover power transformers and rotating electrical machines building from simpler lumped linear models to detailed nonlinear magnetic equivalent circuit based models and finite element models. Chapter 5 describes the hardware emulation techniques for digital protective relays. Chapter 6 addresses the emerging and challenging topic of adaptive time-stepping based real-time EMT simulation. Chapter 7 discusses power semiconductor component models and their hardware emulation varying in complexity from simple system-level switch models to detailed device-level nonlinear behavioral and physics-based electrothermal models. Chapters 8–10 cover the modeling and emulation of various building blocks of DC grids: AC/DC converters, DC/DC converters, and DC circuit breakers. Finally, Chapter 11 culminates in examining the challenge of real-time EMT simulation of large-scale AC and DC grids.

Venkata Dinavahi
Edmonton, Alberta, Canada

Acknowledgments

We would like to express our sincere thanks to the former graduate students and members of the Real-Time Experimental Laboratory (RTX-LAB) at the University of Alberta for allowing us to use material from their publications and theses in this book: Dr. Yuan Chen, Dr. Jiadai Liu, Wentao Wang, Dr. Nariman Roshandel Tavana, Yifan Wang, Dr. Zhuoxuan Shen, Dr. Peng Liu, Dr. Tong Duan, and Shiqi Cao.

We would also like to express our profound gratitude to the Wiley Senior Publishing Team, especially Ms. Mary Hatcher, Ms. Victoria Bradshaw, Ms. Teresa Netzler, and Ms. Amudhapriya Sivamurthy for their timely feedback and for facilitating an efficient and seamless publishing process.

List of Acronyms

AC	alternating current
APU	application processing unit
ASIC	application specific integrated circuit
ATP	alternative transients program
AVM	average value model
AVR	automatic voltage regulator
AXI	advanced eXtensible interface
BJT	bipolar junction transistor
BRAM	block random access memory
CDSM	clamp double submodule
CFM	curve-fitting model
CLB	configurable logic block
CPS	cyber physical system
CPU	central processing unit
DAC	digital to analog converter
DC	direct current
DCFM	dynamic curve-fitting model
DDR4	double data rate fourth-generation
DEM	detailed equivalent model
DMA	direct memory access
DSP	digital signal processing (processor)
DUT	device-under-test
EMT	electro-magnetic transient
FACTS	flexible alternating current transmission system
FBSM	full-bridge submodule
FDLM	frequency dependent line model
FEM	finite element method
FF	flip-flop
FFT	fast Fourier transform

FIFO	first-in first-out
FMC	FPGA mezzanine card
FPGA	field programmable gate array
FPU	floating point unit
FSM	finite state machine
GPIO	general purpose IO
GPU	graphical processing unit
GT	gigabit transceiver
GTH	gigabit transceiver H
GTX	gigabit transceiver X
GTY	gigabit transceiver Y
HBSM	half-bridge submodule
HDL	hardware description language
HEBB	hardware emulation building block
HHB	hybrid HVDC breaker
HIL	hardware-in-the-loop
HLS	high-level synthesis
HVDC	high voltage direct current
I/O	input/output
IGBT	insulated gate bipolar transistor
JTAG	joint test action group
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LCS	load commutation switch
LTE	local truncation error
LUT	look-up table
LVDS	low-voltage differential signaling
lwIP	light weight Internet protocol
MAC	media access layer
MFT	medium frequency transformer
MMC	modular multi-level converter
MMF	magnetomotive force
MOSFET	metal oxide semiconductor field-effect transistor
MOV	metal oxide varistor
MPSoC	multi-processor system-on-chip
MTDC	multi-terminal direct current
MVDC	medium voltage direct current
NBM	nonlinear behavioral model
NLD	nonlinear diode
NPC	neutral-point-clamped
N–R	Newton–Raphson