Design and Development of EFFICIENT ENERGY SYSTEMS

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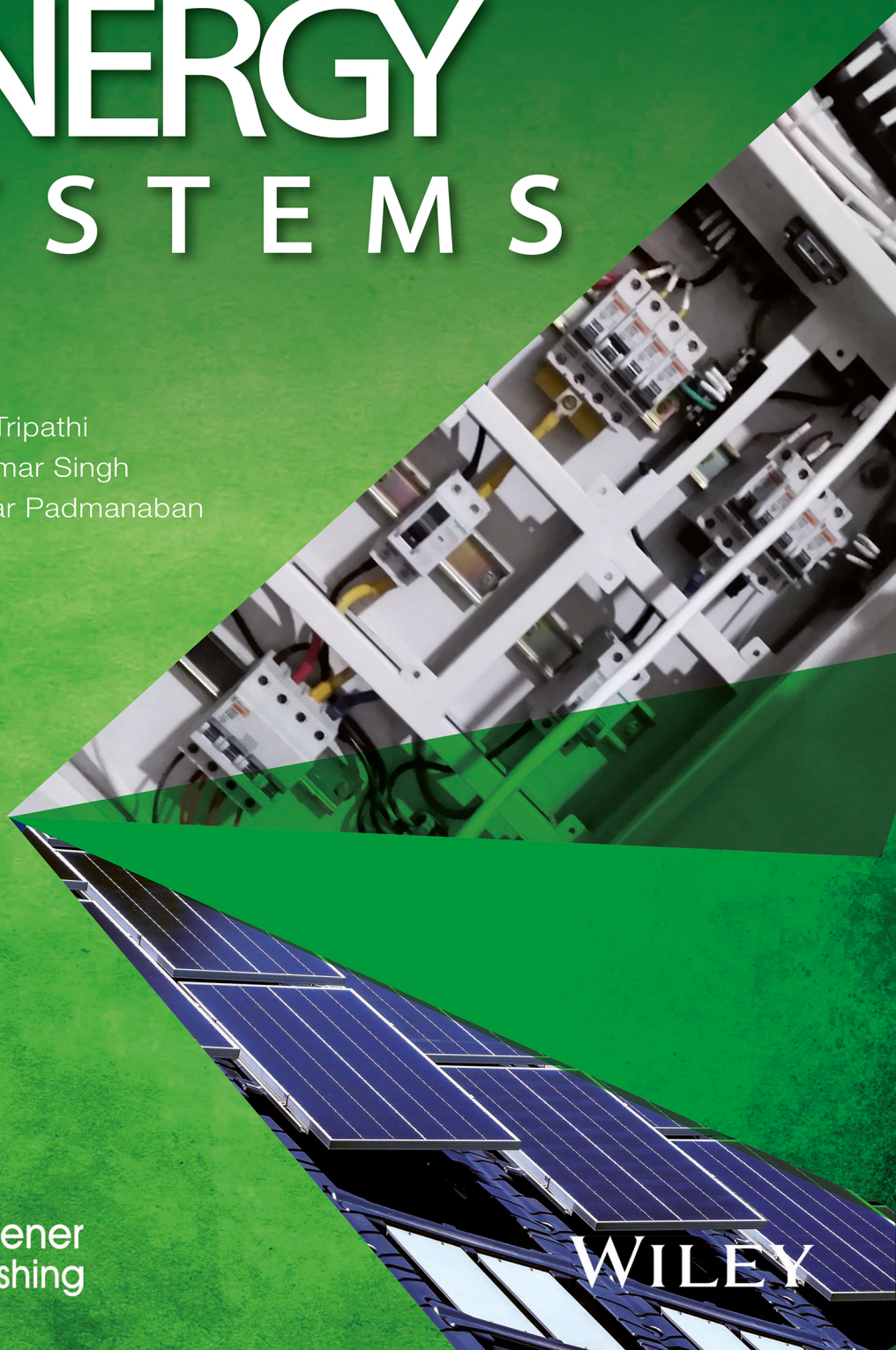

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Contents

Preface

The objective of this edition is to provide a broad view of the fundamental concepts of green energy technology and applications in a concise way for fast and easy understanding. This book provides information regarding almost all the aspects to make it highly beneficial for all students, researchers and teachers of this field. Fundamental principles of green energy technology with the latest developments are discussed in a clear and detailed manner with explanatory diagrams wherever necessary. The book focuses on the basic concepts of Internet of Things (IoT) in power conversion, IoT in renewable energy, and adoption of machine learning, low-power device and circuit design including the latest research available depending upon the technological changes based upon their application.

Chapter Organization

Chapter 1 deals with prefabrication low-power device design and analysis on Visual TCAD device simulator with graphical and programming interfaces. Also, the chapter discusses the design of device-based low-power memory and biomedical applications.

Chapter 2 mainly describes Vedic multiplication based on the compressor block that is focused on the reduction of interconnect wire. The multiplier is implemented using Verilog HDL with cadence NC SIM and the constrain areas, power and delay optimize using underlying block.

Chapter 3 deals with gas leakage detection from drainage to offer safety for sanitary workers from gases such as Carbon monoxide (CO), Hydrogen sulphide (H2S), and Methane (CH4), which are some of the hazardous gases present in underground drainage systems.

Chapter 4 presents a smart healthcare system development with machine learning, which is energy efficient, with reduced network latency and minimum bandwidth.

Chapter 5 This chapter presents some of the solutions in literature for implementing security. The chapter also covers different types of attacks such as goal-oriented attack, performer-oriented attack and layer-oriented attack.

Chapter 6 addresses the energy-saving component and the application of digital technology and Internet of Things (IoT) in large-scale process industries.

Chapter 7 discuss the method deployed relay node in such a way that the network will behave like a sensor network with the help of K-Means clustering approach.

Chapter 8 analyzes an MLI fed Induction Motor Drive by considering Solar Energy as a source. The effects of employing various types of MLI for a PV source-based drive, and methods of deriving maximum drive efficiency are elaborated in this chapter with sufficient simulation results.

Chapter 9 describes energy storage systems using a universal controller that can work for a wide range of voltage to both DC and AC loads with high power rating and low power loss.

Chapter 10 explores energy arrangement producers, energy financial analysts, and directors with a review of the job of IoT in enhancement of energy frameworks.

Chapter 11 focuses on integration of photovoltaic cell, wind energy and other forms of renewable energy. It also covers microgrid systems with high reliability, less transmission losses and improved power system efficiency.

Chapter 12 describes state-of-the-art renewable energy systems and highlights the global efforts being made to increase their efficiency.

Chapter 13 is dedicated to Internet of Things (IoT) technologies with best solutions, ease of the task of monitoring and analysis that opens up a wide range of prospects for making better future decisions.

Chapter 14 examines new security challenges in the Internet of Things (IoT) using machine learning algorithm and the system of interrelated computing devices for its quick development and distribution that are essential for internet and smart device users.

Chapter 15 presents a working and solution process, an illustrative fuzzily defined mathematical framework for optimizing food quality. Here, the emphasis is not only on ensuring fruit safety but also avoiding foodborne diseases.

Chapter 16 is an overview of the various requirements for Internet of Things (IoT) systems and architectures, highlighting different research challenges and security issues connected with IoT.

Chapter 17 presents a state-of-the-art of FinFET technology with low power consumption and their application in a low-power VLSI circuit.

Chapter 18 proposes a single-source high step-up switched-capacitor-based 19-level inverter topology with enhanced power quality that can be extended by addition of switched-capacitor units. The extended topology can produce larger gain and voltage steps.

1

Design of Low Power Junction-Less Double-Gate MOSFET

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Abstract

The requirement of low power consumption and higher IC packing density leads the designer to explore new MOSFET architectures with low leakage current and operating voltages. Multi-gate MOSFET architectures are a promising candidate with increased gate-control over the channel region. Double-gate MOSFET is one of the advanced MOSFETs with a thin-channel region sandwiched into the top and bottom gate. The changes in the position of the top and bottom gate overlap and also have a significant effect on the electrical characteristics of transistors. The higher number of gates increases the drive current capability of the transistor with enhanced gate control that is desired for low-power and high-speed operations of digital circuit and bulk memories. The junction-less feature future improves switching characteristics of multi-gate MOSFETs with more drive current and high I_{ON}/I_{OFF} current ratio. These prefabrication low-power design and analysis can be done on a Visual TCAD device simulator with graphical and programming interfaces that reduce fabrication cost and improve overall throughput.

Keywords: Low power, junction-less, DGMOSFET, TCAD, leakage current, etc.

1.1 Introduction

The size of semiconductor devices is being continuously reduced and has entered into the nanoscale range. Every two years the number of transistors doubles because the size of the MOSFET is reduced. Reducing the size of the MOSFET reduces the size of the channel, which causes short-channel effects and it increases the leakage current. Reduction in the size of semiconductor devices has given rise to short-channel effects (SCEs). The various SCEs are parasitic capacitances, drain field effect on channel field, degraded subthreshold region of operation, mobility degradation, hot carrier effects, etc. To overcome these effects the devices need to be engineered using different techniques like gate or channel engineering. The cause of the SCEs is when the width of the drain barrier extends into the drain and source region barrier lowering. Many MOSFET structures like DG-MOSFET, GAA (Gate-all-around) MOSFET, TG (Triple-gate) MOSFET, SOI (Silicon-on-insulator)

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MOSFET, double-step buried-oxide including junction-less properties have been designed to overcome SCEs [1–6].

MOSFETs are used for analog and RF applications to handle the radio frequency signals that are high in power from devices like televisions, radio transmitters, and amplifiers. MOSFETs are used for biomedical applications [7]. It is used as a biosensor to detect biomolecules. It is useful in detecting molecules like enzymes, nucleotide, protein and antibodies. Using MOSFETs as a biosensor has benefits over other methods as it has more sensitivity, compatibility, mass production and miniaturization. MOSFET is also used to store memory. It is used in the construction of SRAM cells for storing data. MOSFETs were also adopted by NASA to detect interplanetary magnetic fields and interplanetary plasma. MOSFETs are used in digital applications for switching which prevents DC to flow supply and ground that lead to reduced power consumption and providing high input impedance.

1.2 MOSFET Performance Parameters

The MOSFET performance mainly depends on ON and OFF state conditions depending on the different applied bias voltage. The performance analysis is categorized as:

a) DC Analysis

In DC analysis, subthreshold parameters are mainly calculated such as I_{OFF}, DIBL, SS, and threshold voltage (V_{th}). These parameters can be defined as:

i) I_{OFF}: It is OFF-state current when the applied gate voltage (V_{gs}) is less than the threshold voltage (V_{th}).

ii) V_{th}: It the required minimum value of the gate voltage to establish channel inversion.

iii) Subthreshold Slope (SS): It is one of SCE that can be derived from the equation:

$$\mathrm{SS} = \frac{dV_{gs}}{d(logI_d)}\mathrm{mV/decade} \tag{1.1}$$

iv) Drain induced barrier lowering (DIBL): DIBL is another important parameter of SCE which is a measure of threshold voltage variations with the variation in drain voltage for constant drain current. It can be derived from the equation:

$$\mathrm{DIBL} = \frac{dV_{gs}}{dV_{ds}}(\mathrm{mV/V}) \tag{1.2}$$

b) AC analysis

AC analysis is dependent on frequency of applied bias voltages. The important ac parameters are:

i) Transistor Capacitance (Cg): There are several inherent capacitances such as gate to source, the gate to drain and gate to body capacitances.

Transistor capacitances are important for desired switching behavior from OFF to ON state.

ii) Transconductance (g_m): It is a measure of drain current with the variation in gate voltage for constant drain current. It plays an important role to achieve high value of transistor amplifier gain. It can be derived from the equation:

$$g_m = \frac{di_d}{dv_{gs}} \tag{1.3}$$

c) Electrostatic Characteristics

There are a few other important parameters that also have significant importance of MOSFET behavior during ON/OFF state. Energy band diagram, channel potential, electric field distribution and electron-hole density are important electrostatic properties that need to be analysed while designing any MOSFET architecture.

1.3 Comparison of Existing MOSFET Architectures

Table 1.1 shows a comparison of existing MOSFET structures based on their performance and suitable applications.

1.4 Proposed Heavily Doped Junction-Less Double Gate MOSFET (AJ-DGMOSFET)

An AJ-DGMOSFET shown in Figure 1.1 has top and bottom gates arranged asymmetrically with an overlap region of 10nm. An n+ pocket region is added to the source side with heavy doping of donor atoms. p+ polysilicon is used as gate contact material with Hfas an oxide region of high-k dielectric constant. The body thickness is kept very low (6nm). The gate (L_{gate}) is 20 nm, with overlap region ($L_{overlap}$) of 10 nm. The body thickness ($T_{silicon}$) is 6 nm source /drain length ($L_{source} = L_{drain}$) of 8 nm. The oxide thickness (T_{oxide}) is 1 nm. A thin pocket region (n+ doping) is doped with $1x10^{22}$ cm^{-3} with channel region II doping (n+ doping) of $1x10^{19}$ cm^{-3}. Including channel region I + and channel region II, the overall channel length becomes 30 nm.

The high doping concentration of the source drain region with heavy doping of n+ pocket region improves the ON-state current transistor. The drain region doping is slightly less than the source to achieve a low value of leakage current, therefore enhanced current ratio (I_{ON}/ I_{OFF}). Here channel length is also dependent on bias condition. In ON-state the effective channel length is equal to the length of overlap region of top and bottom gates. In OFF-state, the effective channel length is the length excluding overlap region between top and bottom gate.

Figure 1.2 shows a comparison between ON-state and OFF-state of the transistor. Different characteristics have been drawn with and without pocket region. The proposed AJ-DGMOSFET with heavily doped pocket region shows better ratio in comparison to AJ-DGMOSFET without a doped pocket region.

Table 1.1 Comparison of existing MOSFET structures.

Ref.	Existing MOSFET structure and methodology	Electrical performance and applications
[2]	Ge pockets are inserted in SOI JLT	Reduces the lattice temperature. The channel length is 20 nm.
[3]	Gate all around junctionless MOSFET with source and drain extension	The highly doped regions have also led to an increase in I-ON current magnitude by 70%.
[4]	Gate engineering using double-gate MOSFET	The sub-threshold slope is decreased by 1.61% and ON/OFF current ratio is increased by 17.08% and DIBL is decreased by 4.52%. The channel length is 20 nm.
[5]	Gate material engineering and drain/source Extensions	Improves the RF and analog performance. The figure of merit is also increased compared to the conventional double-gate junctionless MOSFET. The channel length is 100 nm.
[6]	Inducing source and drain extensions electrically	Suppresses short-channel effects for the channel length less than 50 nm and also suppresses hot electron effects.
[7]	Nanogap cavity is formed by the process of etching gate oxide in the channel from both the sides of source and drain	Detecting biomolecules such as DNA, enzymes, cells etc using dielectric modulation technique. The channel length is 100 nm.
[8]	Graded channel dual material gate junctionless (GC-DMGJL) MOSFET	The GC-DMGJL MOSFET gives high drain current and transconductance and also reduces short-channel effects. The channel length is 30 nm.
[9]	Black phosphorus is integrated with the junctionless recessed MOSFET	Structure drain current increases up to 0.3 mA. The off current reduces, improvement in subthreshold slope. The channel length is 44 nm.
[10]	Fully depleted tri material double-gate MOSFET is used	Improvement in the RF performance, linearity and analog performance compared to the DM-DG MOSFET and single material DG MOSFET. The channel length is 35 nm.
[11]	Pocket region is constructed near the source and drain region and is heavily doped	Good immunity from short-channel effects and can meet the specifications of OFF-state current and ON-state current. The channel length is 100 nm.

(*Continued*)

Table 1.1 Comparison of existing MOSFET structures. (*Continued*)

Ref.	Existing MOSFET structure and methodology	Electrical performance and applications
[12]	A transparent gate recessed channel is used	Enhancement of cut-off frequency by 42% and oscillator frequency is increased by 32%. The channel length is 30nm.
[13]	MOSFET with asymmetrical gate to improve the functioning of the device	Decrease in subthreshold slope (68 mV/dec) and drain induced barrier lowering (65 mV/V). The channel length is 20 nm.
[14]	6-T SRAM cell using silicon on insulator	The area of the junctionless transistor-based 6-T SRAM cell using silicon on inductor is 6.9 μm-cube and that of the conventional structure is 11.3 μm -cube.
[15]	Short-channel dual metal gate with recessed source and drain SOI MOSFET	This device provides high on current, low DIBL value. The channel length is 30 nm -300nm.
[16]	Dual Material Surrounding Gate MOSFET to suppress short-channel effects	DMSG MOSFET (SCEs) more efficient as compared to a conventional SMSG MOSFET
[17]	Misalignment effect introduced by the asymmetrical source and drain	The region which is non-overlapped produces extra series resistance and weak control over the channel, while the additional overlapped region produces extra overlap capacitance and supply to ground leakage current through gate
[18]	Optimized the design of the gate all around MOSFET and compared it with the double gate MOSFET	GAA structure reduced the DIBL value to 81.44 mV/V when compared to the double-gate MOSFET. The ON-state current is increased and OFF-state current is reduced.
[19]	The deviation in the oxide thickness between the two gates is considered small. A surface potential solution is used for symmetric double-gate MOSFET for initial trial approximation for approaching surface potential solution for asymmetric double-gate MOSFET.	Different parameters of MOSFET like drain current, 5channel current, transconductance, gate capacitances and the effect of oxide thickness on these parameters are determined.
[20]	Performance analysis of junctionless double-gate MOSFET based 6T SRAM with gate stack configuration	The use of high k dielectric material in the junctionless DG-MOSFET shows improvement in static noise margin. Scaling down of gate length degrades the stability.

(*Continued*)

Table 1.1 Comparison of existing MOSFET structures. (*Continued*)

Ref.	Existing MOSFET structure and methodology	Electrical performance and applications
[21]	Simulation of junctionless double-gate MOSFET with symmetrical side gates. With the presence of side gates the channel present under the front gate, is electrically insulated from the drain voltage resulting to electron shielding.	The DIBL and SS values improved using the side gates. The drain voltage effect on the channel is reduced so it becomes easy for the gate to have more control over the channel.
[22]	A structure of double-gate MOSFET with symmetrical insulator packets for improving the SCEs. In this, insulator packets were inserted between the channel junction and source/drain ends	Hot electron reliability improves. There is an improvement in the DIBL value and ON/OFF-state current ratio.

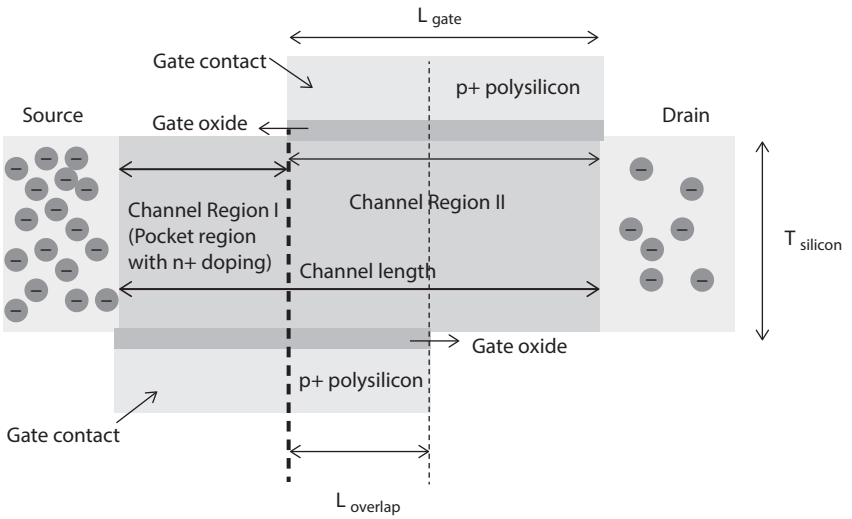

Figure 1.1 2D view of AJ-DGMOSFET.

Figure 1.4 shows the performance of MOSFET when different gate contacts are used like aluminium, polysilicon and copper. MOSFET shows better performance when polysilicon is used as a gate contact. Metal gates like Aluminium and copper operate at voltages 3V to 5V. The lowering of operating voltages leads to the use of polysilicon gate contact. From the graph we can observe at lower operating voltages polysilicon gate contact gives better performance because the OFF-state current is low.

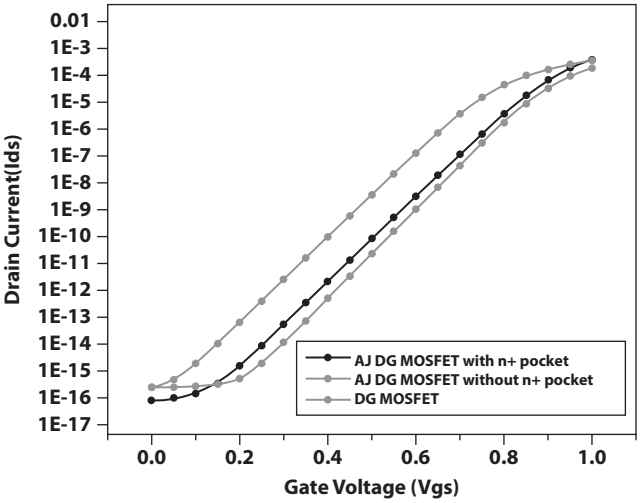

Figure 1.2 I_d versus V_{gs} plot of AJ-DGMOSFET.

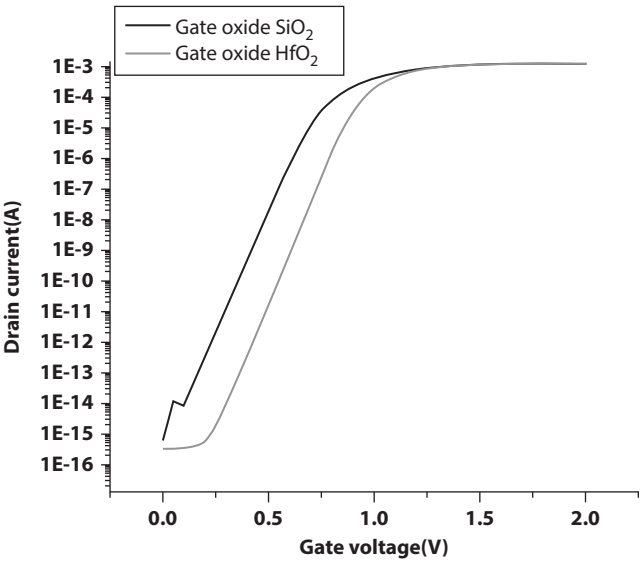

Figure 1.3 Id Versus Vgs plot with different oxide region material.

The proposed JL-DG MOSFET has ratio of 10^{13} which is higher than other existing structures. The calculation of SCE parameters like SS and DIBL is also a deciding factor for device performance. The proposed device show SS value of 59 mV/ decade and DIBL of 13.4 mV/V. Both SS and DIBL values are less than other existing transistors. Therefore, heavily doped AJ-DG MOSFET has superior ON/OFF performances.

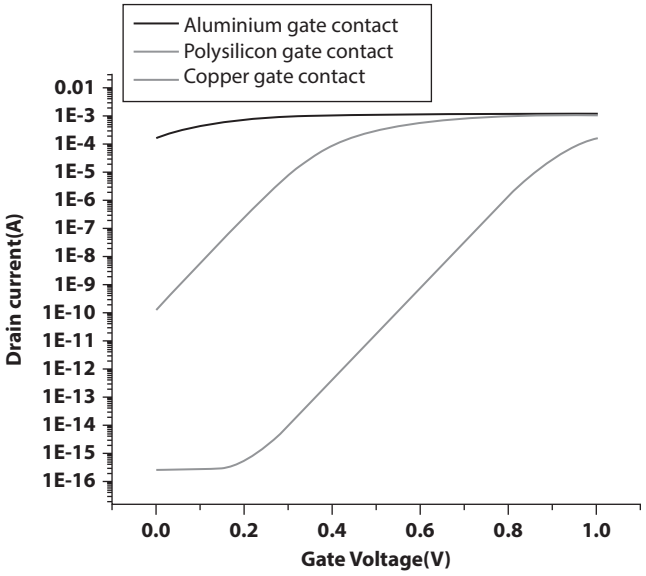

Figure 1.4 I_d versus V_{gs} Plot of different gate contact material.

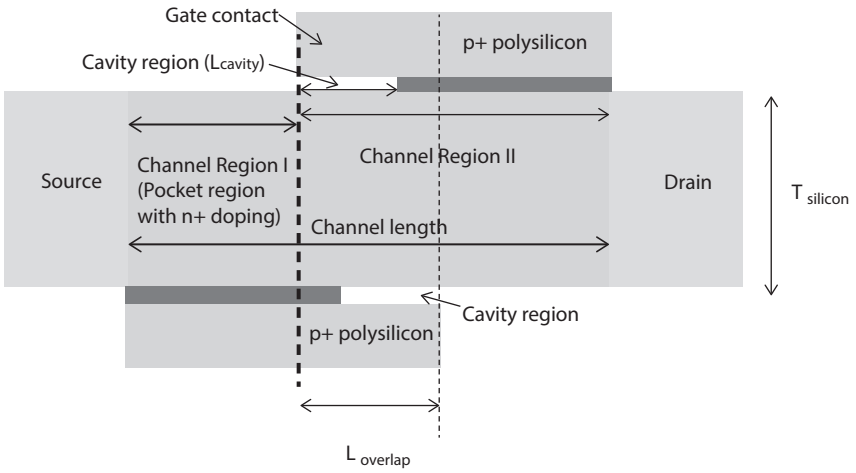

Figure 1.5 JL-DG MOSFET with cavity region.

1.5 Heavily Doped JL-DG MOSFET for Biomedical Application

DG MOSFETs were designed with a nanogap cavity region as bio-sensor that can sense the bio-molecule present in the nanogap cavity [23, 24]. These bio-sensors work on the principle of dielectric modulation with the variation in bio-species present in the air (nanogap cavity) that further varies the electrical parameters of the device.

Figure 1.5 shows the 2-D view of JL-DG MOSFET with a cavity region. Here the cavity plays an important role to sense the bio-species present in air. The presence of bio-species

and their concentration affect the dielectric constant of the cavity region that further affects the electrical parameters of transistor. The cavity region with different length (L_{cavity}) and height (H_{cavity}) shows varied device sensitivity towards the presences of biomolecules. This effect has been studied through varying dielectric constant with different materials such as air, SiO_2, HfO_2 and S_3N_4.

Figure 1.5 shows AJ-DG MOSFET with the nanogap cavity region. A thin SiO_2 layer used for binding the molecules entering the cavity region by restricting the movements of bio-molecules. For the presented device the cavity region height (H_{cavity}) is 2.7 nm and SiO_2 layer thickness is 0.3 nm. Another way to analyze device sensitivity is by introducing different types of charged particles in the cavity region.

In Figure 1.6 a sharp change is observed in the threshold voltages with the different dielectric constant of the material added in the cavity region. The longer cavity region length shows more variations in threshold voltage that results in the shifting of channel inversion threshold level. Therefore with a higher value of dielectric constant, the threshold voltage lowers. This shows that the device is highly sensitive towards the change in dielectric material constant depending on biomolecule presence resulting in electrical parameter variations.

A significant variation in threshold voltage is observed with a change in oxide thickness. The changing oxide thickness results in a change in the cavity region thickness that also affects the electrical parameter variations.

1.6 Conclusion

The AJ-DG MOSFET is a suitable choice for low-power applications such as bulk memories that are integral parts of many IoT-enabled systems. The performance of AJ-DG MOSFET can also be varied by adjusting the position of the top and bottom gate overlapping regions. High ON/OFF current ratio and low leakage current are the key features of the AJ-DG MOSFET with low static power consumption and enhanced speed of circuit operation. Another application of JL-DG MOSFET is as biosensor by introducing cavity region

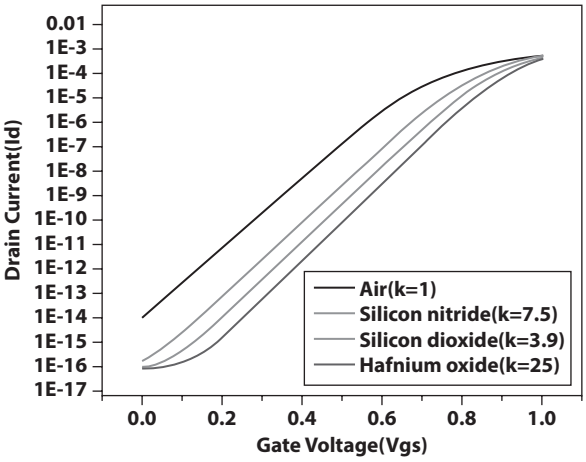

Figure 1.6 I_d Versus V_{gs} of AJ-DG MOSFET with varying dielectric constant (L_{cavity} = 7nm).

between gate and channel. These cavity regions are sensitive to the bio species present in the environment. The variation in biomolecule changes the dielectric constant of the medium that results in the variation in electrical parameters of a device that can be easily measured to detect the presence of bio-species.

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