

Lecture Notes in Networks and Systems 147

Nikhil Ranjan Das
Santu Sarkar *Editors*

Computers and Devices for Communication

Proceedings of CODEC 2019

 Springer

Lecture Notes in Networks and Systems

Volume 147

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Editors

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ISSN 2367-3370

ISSN 2367-3389 (electronic)

Lecture Notes in Networks and Systems

ISBN 978-981-15-8365-0

ISBN 978-981-15-8366-7 (eBook)

<https://doi.org/10.1007/978-981-15-8366-7>

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Preface

The world is witnessing a tremendous progress in science and technology through significant transformation in industrial manufacturing, which has resulted in the emergence of the Fourth Industrial Revolution (Industry 4.0). Now, we talk about materials, structures and devices with prefix ‘smart’, and we wish to see ourselves in smart home, in smart cities. This vision is being fulfilled due to the advances in high-speed communication, optimized computation, artificial intelligence, machine-to-machine communication, material science, novel devices, data science and several other areas of science and technology.

To discuss such advances and recent trends in industry and research, the Seventh International Conference on Computers and Devices for Communication (CODEC) was organized on 19–20 December in Kolkata, India, by bringing together researchers from different parts of the world to exchange their views. CODEC was initiated in 1998 to begin the golden jubilee year celebration of the Institute of Radio Physics and Electronics (IRPE), a department of the University of Calcutta. The IRPE (estd.1949) is the first university department in India to begin teaching and research in electronics, devices, communication, control and all areas covered by radio science. CODEC is organized by the IRPE, and since 2014, it has become a triennial event, though the seventh CODEC was held after a 4-year gap due to some unavoidable reasons. All CODECs were participated by international delegates from different parts of the world and at different times were technically sponsored by several IEEE societies (EDS, PS, APS, MTTS), IET, SPIE, etc. The deliberations from experts were in the form of keynote address, plenary talks, invited lectures and contributory research papers.

Selected contributory research papers of CODEC-19, after peer review (minimum two reviewers) and plagiarism checks, have been considered for publication in Springer Lecture Notes in Networks and Systems (LNNS). In this book, each paper has appeared as a chapter. The chapters cover almost all important areas of electronics and communication and are grouped into four broad categories as follows:

- Computer Applications and Control (CAC)
- Communication and Space Science (CSS)

- Microwave and Lightwave Technology (MLT)
- Nanoscale Materials and Devices (NMD)

It was a hard task to arrange peer reviews and plagiarism checks for all the contributory papers to comply with the publication requirement of Springer LNNS. The editors are thankful to their colleagues and staff in the department, who made a meticulous effort to complete the task towards the final selection of papers for publication. The editors are grateful to the reviewers for their time and efforts towards critical review of the submitted contributory research papers. Full credit goes to them for their evaluation to ensure the high quality and standard of the papers for the Springer Lecture Notes. It is a pleasure to acknowledge the help received from the Springer publication/production team, including G. Ayyasamy, S. Ravivarman, P. Thirumani, to name a few, and especially, Mr. Aninda Bose, Senior Editor of Springer Nature (Research Publishing).

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About the Editors

Dr. Nikhil Ranjan Das is a Professor in the Department of Radio Physics and Electronics, University of Calcutta. He served as the Head of the Department, and the Dean of Engineering & Technology, and the Director of the Centre for Research in Nanoscience and Nanotechnology, the University of Calcutta. He was a Postdoctoral Fellow and later a Postdoctoral Research Associate at McMaster University, Canada, from 1999 to 2002. He was a Senior Guest Scientist in Trieste (Italy), and Visiting Professor at McMaster University (Canada), the University of Sheffield (UK), and Pohang University of Science and Technology (POSTECH, South Korea). He was also a Visiting Scientist at the Technical University Dresden, Germany, in 2018 as a recipient of the INSA-DFG award. His research focuses on design, simulation, and optimization of optoelectronic and photonic devices, including semiconductor nanostructures. He has been a reviewer for several IEEE, IET, and other journals. He is a Fellow of IETE and IE(I) and senior member of the IEEE. He was the founder and Chairman of the IEEE Photonics Society Calcutta Chapter, and has been the Branch Counselor of IEEE Calcutta University Student Branch. He completed international collaborative programs such as UKIERI with the University of Sheffield and was the key person from the University of Calcutta for Erasmus Mundus 'LEADERS' program.

Dr. Santu Sarkar received his B.Sc. (Hons.) degree in Physics from the University of Calcutta, in 1995, and B.Tech., M.Tech., and Ph.D. degrees in Radio Physics and Electronics from the University of Calcutta, in 1998, 2000, and 2011, respectively. From 2000 to 2004, he was a Lecturer at Asansol Engineering College, University of Technology, West Bengal. From 2004 to 2016, he was an Associate Professor and Head of the Electronics and Communication Engineering Department, Academy of Technology. He is currently an Assistant Professor in the Department of Radio Physics and Electronics, University of Calcutta.

Computer Applications and Control (CAC)



IEEE 754 Floating Point Pipelined Multiplier with Karatsuba for Mitigations of Area and Power

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Abstract. The proposed architecture implements IEEE 754 floating point pipelined multiplier merge single and double precision using Karatsuba. This paper is presented in order to reduce power and area expenditures to fast the process of the adder and reduce delay. To achieve, the design Verilog language is used and targeted on Xilinx Virtex-5 (XC5VLX155FF1760-3) and Cadence on TSMC-180 nm CMOS technology. The architecture reduces the processing block as it uses exception block as replacement, whereas in the Karatsuba multiplier, the adders are replaced with different adder to obtain reduce results of area and power. Karatsuba is used in placing the mantissa in the multiplier, and in the Karatsuba architecture, the previous design is replaced in order to reduce the numbers of operations in block processing; here, left shifting is in the $27 * 27$ bits multiplier. By implementation of various adders, better results are obtained when compared to the previous work in terms of DSP 6 (4%), LUTs 1367 (1%), frequency 168.741 MHz, dynamic power 123.61 mW.

Keywords: Xilinx Virtex-5 · Cadence · Verilog · Karatsuba · Floating point pipelined multiplier

1 Introduction

In recent years, there are fabulous developments in computation of results in field of adders, subtractors, multipliers, divisions and other operations. IEEE 754 plays all the function in it as floating point multiplier. There are different types of precisions; for instance, two types of precisions are used in this as single precision and double precision.

2 System-level Architecture

We purposed an exception processing block replacing three processing blocks of multiplicand processing, exponent processing and sign processing, and there are two blocks in stage of 1–5 where $27 * 27$ bits multipliers are show in Fig. 1.

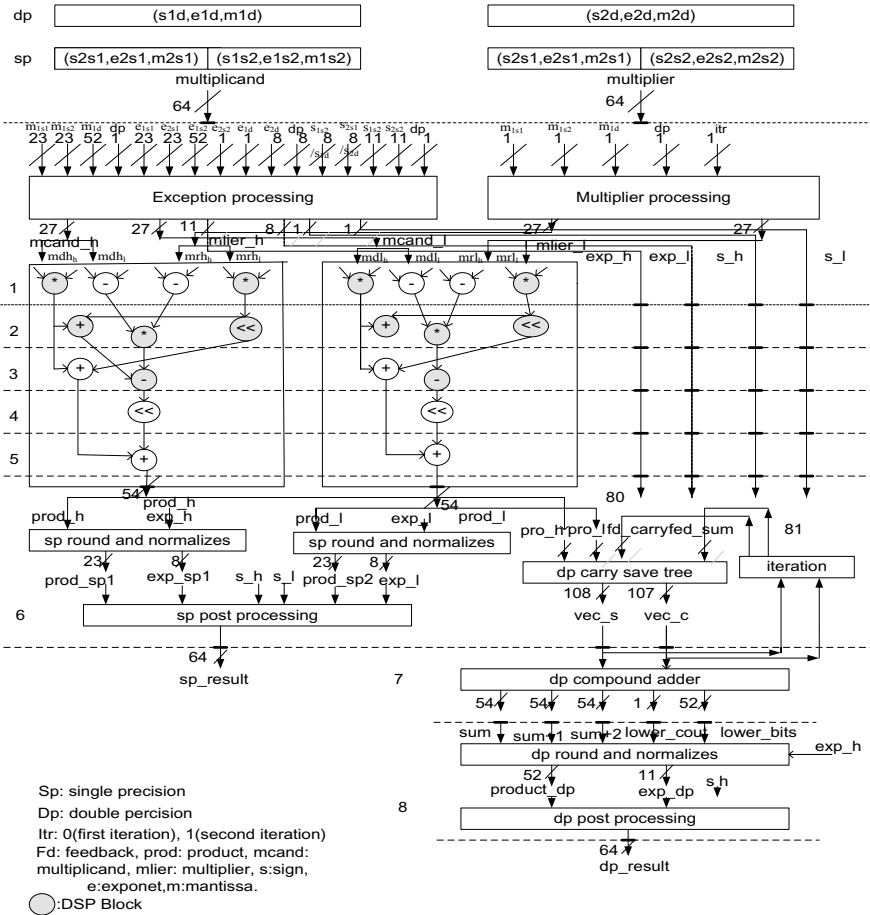


Fig. 1 Data path of the proposed single- and double precision floating point

3 Simulation Results Obtained in Xilinx ISE Software

Simulation results of IEEE 754 floating point pipeline multiplier merged single precision and double precision using Karatsuba with various adder is showed in Figs. 2, 3 and 4.

3.1 Carry Propagate Adder

Inputs: $A_{in} [7:0] = 36$; $B_{in} [7:0] = 129$; $C_{in} = 1$; Width $[31:0] = 8$.

Output: $SUM [7:0] = 166$; Carry out = 0.

3.2 Kogge–Stone Adder

Inputs: $Clk = 1$; $dp = 0$; $itr = x$; Multiplicand $[63:0] = e2ca4ec5f4007ae8$; Multiplier $[63:0] = de8e28bd2e584...$; **Outputs:** SP Result $[63:0] = 90a7fa5380000000$.

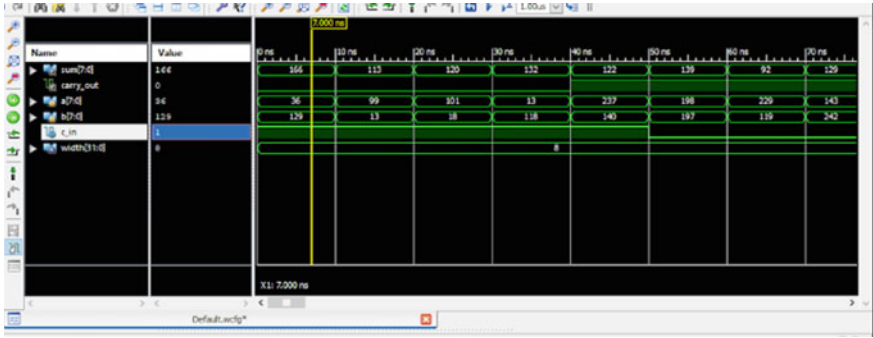


Fig. 2 Simulation result of carry propagated adder

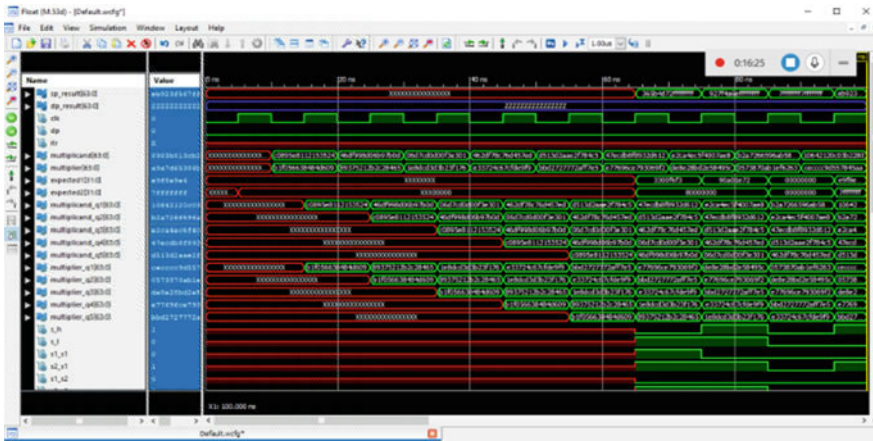


Fig. 3 Simulation result of Kogge–Stone adder

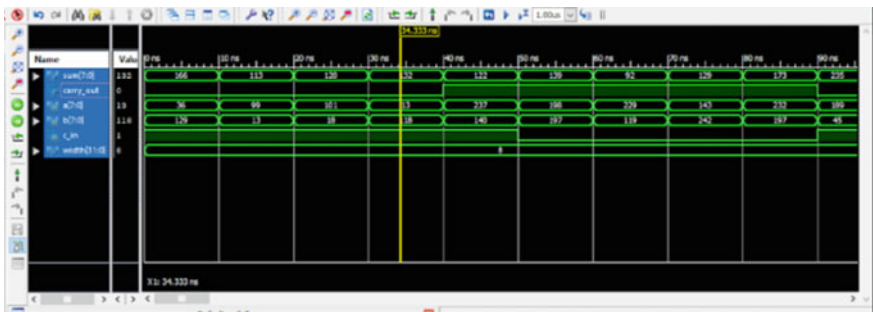


Fig. 4 Simulation result of carry look ahead adder

3.3 Carry Look Ahead Adder

Inputs: $A_{in} [7:0] = 13$; $B_{in} [7:0] = 118$; $C_{in} = 1$; Width $[31:0] = 8$.

Outputs: SUM [7:0] = 132; Carry out = 0.

4 Schematic of Floating Point Multiplier in Cadence

Figure 5 is the structure view of compiler RC 14.28 this is implemented in Cadence in TSMC-180 nm CMOS technology.

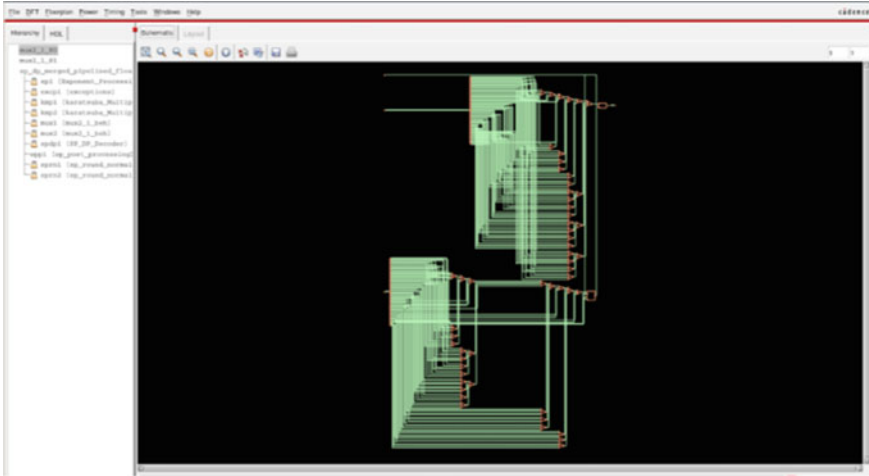


Fig. 5 Schematic of floating point multiplier

5 Simulation Results Obtained in Cadence Simulator Software

See Fig. 6.

a Dynamic power = 17,928,133.149 nW; **b** Area = 17,226.

6 Comparison Results

See Table 1.

7 Conclusion

The multiplier is implemented in Xilinx on Virtex-5 (XC5VLX155FF1760-3) and Cadence, for high-performance Kogge–Stone adder is best in terms as it obtained better results as less power as per the desired specifications by implementation of the floating point multiplier. The adder is implemented successfully with Karatsuba in Xilinx and Cadence, with less area and power consumptions achieved as compare to previous work [1]. This work can be further increased in by using Cadence with different multipliers [2], Alteria-7 [3].

(a) Dynamic Power Report of adder.

The screenshot shows a dynamic power report with columns for Instance, Gate Area, Gate Count, and Power (mW). It lists various adder components such as add_00_00, add_00_01, and add_00_02, along with their respective power consumption values.

(b) Area Report of adder

The screenshot displays an area report with columns for Instance, LUTs, Registers, and Logic Elements. It provides a detailed breakdown of the hardware resources used by the adder components, including the total number of LUTs and registers consumed.

Fig. 6 a Dynamic power report and b area report for adder

Table 1 Comparison results of various adders

Device	DSP	LUT's	Frequency (MHz)	Dynamic power (mW)
Virtex-5 adder	6 (4%)	1565 (1%)	156.33	168.7
Virtex-5 carry look ahead adder	6 (4%)	1759 (1%)	125.142	170.37
Virtex-5 carry propagate adder	6 (4%)	1434 (1%)	117.542	170.10
Virtex-5 Kogge–Stone adder	6 (4%)	1367 (1%)	168.741	123.61
Virtex-5 [1]	6 (4%)	1117 (1%)	348.19	247.70

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Digital Fault Detection Techniques: A Review

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Abstract. The testing and detection of faults in digital circuits has become extremely relevant to both industry as well as academia in recent years. Effective and cheap testing procedures and algorithms help to decrease the manufacturing costs for digital circuits to a significant extent. The present work discusses state-of-the-art digital fault detection techniques. Specific emphasis is laid on a relatively new class of techniques that employ machine learning techniques to classify and detect faults in digital circuits and systems, especially focusing on Bayesian networks and support vector machines (SVMs). The work is concluded by the proposal of a machine learning-based fault probability estimation technique and brief deliberations on the enhancements that can be made in future to the technique.

Keywords: Testing · Digital faults · Machine learning · Bayesian network · Support vector machines

1 Introduction

Digital systems currently define the way the majority of humans interact and remain connected to each other as well as the natural world. The advent of digital circuits has brought about new possibilities in terms of computation, control and design of electronic systems. Digital circuits have revolutionized many domains of engineering in direct or indirect ways. However, certain critical issues still remain in the field of digital circuits and systems. One such issue is the testing of digital circuits for the possibility of occurrence of faults. Since a fault in a critical digital circuit or system can have far-reaching effects resulting in malfunctioning, researchers have proposed various methods for detection of digital faults. However, due to the ever-increasing complexity of digital systems, new methods need to be regularly investigated to keep up with the increase in number and complexity of digital circuits.

Researchers have outlined extensive testing procedures and principles for the testing of digital circuits. Many tools and algorithms have been designed to ensure the functional integrity of digital circuits and systems. However, new tools are constantly being proposed and investigated by scholars for the possible applicability to the domain of

digital circuit and system testing. Consequently, some of the important state-of-the-art techniques are reviewed in this work.

The paper is organized in the following manner. Section 2 contains the survey of research papers outlining novel techniques for determining digital faults. This section lays special emphasis on machine learning-based techniques, which have gained in prominence over the recent few years. Section 3 elucidates the proposed machine learning-based scheme for detection and classification of digital faults. Section 4 concludes the paper with a brief discussion on the avenues of research expected to stem from the present work.

2 Literature Survey

Digital circuits have been tested using various techniques since their inception. Parameters such as the number of states have been studied for identifying fluctuations in their numbers and estimating fault coverage [1]. The tests used by researchers have at times been singular; however, in recent years, adaptive testing has gained prominence due to the highly accurate results available using such testing procedures [2]. Binary decision diagrams have also been used by some scholars to identify conditional digital faults [3]. Among the classes of digital faults, delay faults can cause massive depreciation in circuit performance. Such delay faults have been studied by certain researchers in order to reduce their testing time [4].

Automated design flows have been put forward by authors in a bid to apply triple modular redundancy in such digital circuits [5]. The patterns generated for testing a digital circuit have also been validated by some researchers using automatic test pattern generator (ATPG) [6]. Research has also been carried out to reduce testing time related to test pattern generation [7, 8]. Reseeding of the linear feedback shift register (LFSR) has been employed by the scholars to that end [7].

Extensive research has also been done in the domain of detection and elimination of hidden faults [9]. The evolution of hidden faults has been examined in conjunction with their proposed solutions [10]. Injection of faults has been employed for the purpose of diagnosis of digital faults in FPGA-based systems [11]. Power supply glitch-based faults have also been investigated, and appropriate solutions based on fast clock modulation have been proved to be applicable in such cases [12]. Other state-of-the-art approaches to digital fault detection include quantum-based test generation methods [13]. Nowadays, the utilization of novel digital VLSI circuits is increasing exponentially, and the design trends are to decrease the node capacitance and power supply requirements. This results in huge susceptibility to transient faults to increase in the nano-range digital CMOS designs [14].

In recent times, machine learning has gained importance in the domain of digital fault testing, diagnosis and mitigation. Classification and recommendation-based algorithms involving neural networks (NNs) and support vector machines (SVMs) have been studied and developed for digital fault localization in object-oriented paradigms [15]. Digital fault identification and mitigation has been carried out for vehicular systems connected by wireless networks through the application of NNs [16].

Among the machine learning techniques popularly employed, Bayesian techniques have been used frequently by researchers in recent years due to their comparative simplicity, as well as their accuracy. Bayesian networks have been extensively examined by some researchers in the context of their applicability to the testing and fault identification of digital systems of varying specifications [17]. The detection of data faults in wireless sensor networks has, for example, been accomplished through a distributed Bayesian network technique, which allows for rapid detection and classification of faults [18]. Minimal risk Bayesian decision theory has been used in conjunction with other techniques to diagnose faults [19]. Principal component analysis (PCA) has been employed by some researchers to determine faults even in situations with missing information [20].

The present work therefore proposes a Bayesian method of prediction of probability of occurrence of a fault in any particular type of digital circuit or system, as discussed in the following section.

3 Proposed Technique

Multiple parameters may influence the occurrence of faults in digital circuits. These include but are not limited to physical parameters such as aging of the circuit, power supply noise, sudden drops in voltage at certain points in the circuit and crosstalk effect between connecting wires [1]. These factors may or may not cause faults in digital circuits at any given instance of their occurrence. Consequently, it is possible to design a probabilistic Bayesian model for estimation of the probability of occurrence of a fault in a digital circuit in the presence of these parameters. The only assumption used to formulate such a model is the fact that the parameters used are independent of each other.

A frequency table containing the instances where faults occur or do not occur in the presence of each of the above-mentioned parameters is constructed. The instances are represented by suitable variables. The number of times faults do not occur despite aging of circuit is represented by A_{nf} , and the number of times faults occur in an aged circuit is represented as A_{of} . In a similar manner, where fault does not occur despite power supply noise being present, S_{nf} represents such instances, with corresponding number of faulty instances being represented by S_{of} . The corresponding variables for voltage drops are V_{nf} and V_{of} , respectively, and for crosstalk, C_{nf} and C_{of} , respectively. Table 1 is presented as follows.

From Table 1, the corresponding probabilities can be found. The overall probability of a fault not occurring in presence of these parameters is represented by P_{FF} and the corresponding probability of occurrence of a fault by P_{TF} . The total number of instances that each parameter is present in circuits is determined by the sum of the number of times faults occur and do not occur in circuits, for each parameter. The corresponding number of instances for aging, power supply noise, sudden voltage drops and connector crosstalk is represented by A , S , V and C , respectively.

$$A_{nf} + A_{of} = A \quad (1)$$

$$S_{nf} + S_{of} = S \quad (2)$$

Table 1 Digital faults occurring in the presence of various parameters

Parameter	Fault not occurring	Fault occurring
Aging of circuit	A_{nf}	A_{of}
Power supply noise	S_{nf}	S_{of}
Sudden voltage drops	V_{nf}	V_{of}
Connector crosstalk	C_{nf}	C_{of}

$$V_{nf} + V_{of} = V \quad (3)$$

$$C_{nf} + C_{of} = C \quad (4)$$

$$P_{FF} = (A_{nf} + S_{nf} + V_{nf} + C_{nf}) / (A + S + V + C) \quad (5)$$

$$P_{TF} = (A_{of} + S_{of} + V_{of} + C_{of}) / (A + S + V + C) \quad (6)$$

The total probabilities of occurrence of faults for each of the parameters are also determined through the following equations. The probability that an aging circuit will experience a fault is given by OF_A , while the probability of no occurrence of a fault of an aging circuit is given by NF_A . Similarly, for power supply noise, the variables are OF_S and NF_S , while for sudden voltage drops, they are OF_V and NF_V , respectively, and for crosstalk, the parameters are OF_C and NF_C . The corresponding equations are given as follows.

$$OF_A = A_{of} / (A + S + V + C) \quad (7)$$

$$NF_A = A_{nf} / (A + S + V + C) \quad (8)$$

$$OF_S = S_{of} / (A + S + V + C) \quad (9)$$

$$NF_S = S_{nf} / (A + S + V + C) \quad (10)$$

$$OF_V = V_{of} / (A + S + V + C) \quad (11)$$

$$NF_V = V_{nf} / (A + S + V + C) \quad (12)$$

$$OF_C = C_{of} / (A + S + V + C) \quad (13)$$

$$NF_C = C_{nf}/(A + S + V + C) \quad (14)$$

Now, the following Bayes' theorem, $\text{Prob}(x|y)$ is the probability of event x occurring provided event y has occurred, $\text{Prob}(y|x)$ is the probability of event y occurring provided event x has occurred, $\text{Prob}(y)$ is the total probability of event y occurring, and $\text{Prob}(x)$ is consequently the total probability of event x occurring. By Bayes rule, the equation governing these probabilities is given by

$$\text{Prob}(x|y) = \text{Prob}(y|x) * \text{Prob}(x)/\text{Prob}(y) \quad (15)$$

Using the previous Eqs. (1)–(14) with Eq. (15), we can determine the probability of a fault occurring in the presence of any parameter. As an example, the numbers of faults occurring or not occurring at various instances in the presence of the parameters are simulated. The simulation results are shown in Table 2.

Table 2 Digital fault simulated to occur in presence of parameters

Parameter	Fault not occurring	Fault occurring
Aging of circuit	13	112
Power supply noise	66	57
Sudden voltage drops	58	43
Connector crosstalk	80	113

Using Eqs. (1)–(15), the probabilities of faults occurring due to each of the factors can be calculated, as shown in Table 3.

Table 3 Probabilistic estimates for occurrence of digital faults

Parameter	Probability of fault not occurring	Probability of fault occurring
Aging of circuit	0.02	0.21
Power supply noise	0.12	0.1
Sudden voltage drops	0.11	0.08
Connector crosstalk	0.15	0.21
Total probabilities	0.4	0.6

It can be seen from Table 3 that the proposed Bayes estimation model can estimate individual fault occurrence probabilities as well as joint probabilities, for example, the probability of a fault occurring in the presence of both power supply noise as well